



ST7735P3

**132RGB x 162dot 262K Color with Frame Memory
Single-Chip TFT Controller/Driver**

Datasheet

Version P0.1

2021/08

Sitronix Technology Corporation

Sitronix Technology Corp. reserves the right to change the contents in this document without prior notice.

LIST OF CONTENT

1	GENERAL DESCRIPTION	9
2	FEATURES	9
3	PAD ARRANGEMENT	11
	3.1 Output Bump Dimension	11
	3.2 Input Bump Dimension	12
	3.3 Alignment Mark Dimension	13
	3.4 Chip Information	14
4	PAD CENTER COORDINATES	15
5	BLOCK DIAGRAM	21
6	PIN DESCRIPTION	22
	6.1 Power Supply Pin	22
	6.2 Interface Logic Pin	22
	6.3 Mode Selection Pin	24
	6.4 Driver Output pins	25
	6.5 Test Pins	26
7	DRIVER ELECTRICAL CHARACTERISTICS	27
	7.1 Absolute Operation Range	27
	7.2 DC Characteristic	28
	7.3 Power Consumption	29
8	Timing chart	30
	8.1 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (8080 Series MCU Interface)	30
	8.2 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (6800 Series MCU Interface)	32
	8.3 Serial Interface Characteristics (3-line Serial)	34
	8.4 Serial Interface Characteristics (4-line Serial)	35
9	Function Description	36
	9.1 Interface Type Selection	36
	9.2 8080-series MCU Parallel Interface (P68 = '0')	37
	9.2.1 Write Cycle Sequence	38
	9.2.2 Read Cycle Sequence	39
	9.3 6800-series MCU Parallel Interface (P68 = '1')	40
	9.3.1 Write Cycle Sequence	41
	9.3.2 Read Cycle Sequence	42
	9.4 Serial Interface	43
	9.4.1 Command Write Mode	43
	9.4.2 Read Functions	45
	9.4.3 3-line Serial Protocol	45
	9.4.4 4-line Serial Protocol	46

9.5 Data Transfer Break and Recovery.....	47
9.6 Data Transfer Pause.....	49
9.6.1 Serial Interface Pause.....	49
9.6.2 Parallel Interface Pause.....	49
9.7 Data Transfer Modes.....	50
9.7.1 Method 1.....	50
9.7.2 Method 2.....	50
9.8 Data Color Coding.....	51
9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= "100").....	51
9.8.2 8-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= "03h".....	51
9.8.3 8-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= "05h".....	52
9.8.4 8-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= "06h".....	53
9.8.5 16-Bit Parallel Interface (IM2,IM1, IM0= "101").....	54
9.8.6 16-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= "03h".....	54
9.8.7 16-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= "05h".....	55
9.8.8 16-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= "06h".....	56
9.8.9 9-Bit Parallel Interface (IM2, IM1, IM0="110").....	57
9.8.10 Write 9-bit Data for RGB 6-6-6-bit Input (262k-color).....	57
9.8.11 18-Bit Parallel Interface (IM2, IM1, IM0="111").....	58
9.8.12 18-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h".....	58
9.8.13 18-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h".....	59
9.8.14 18-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h".....	60
9.8.15 3-line Serial Interface.....	61
9.8.16 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h".....	61
9.8.17 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h".....	62
9.8.18 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h".....	63
9.8.19 4-line Serial Interface.....	64
9.8.20 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h".....	64
9.8.21 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h".....	65
9.8.22 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h".....	65
9.9 Display Data RAM.....	66
9.9.1 Configuration (GM[1:0] = "00").....	66
9.9.2 Memory to Display Address Mapping.....	67
9.9.3 When using 128RGB x 160 resolution (GM[1:0] = "11", SMX=SMY=SRGB= '0').....	67
9.9.4 When using 132RGB x 132resolution (GM[1:0] = "01", SMX=SMY=SRGB= '0').....	68
9.9.5 When using 132RGB x 162 resolution (GM[1:0] = "00", SMX=SMY=SRGB= '0').....	69
9.9.6 Normal Display On or Partial Mode On.....	70
9.9.7 When using 128RGB x 160 resolution (GM[1:0] = "11").....	70

9.9.8 When using 128RGB x 160 resolution (GM[1:0] = "01")	71
9.9.9 When using 132RGB x 162 resolution (GM[1:0] = "00")	72
9.10 Address Counter	73
9.11 Memory Data Write/ Read Direction	74
9.11.1 When 128RGBx160 (GM= "11")	74
9.11.2 When 132RGBx132 (GM= "01")	74
9.11.3 When 132RGBx162 (GM= "00")	75
9.11.4 Frame Data Write Direction According to the MADCTL Parameters (MV, MX and MY)	76
9.11.5 Scroll Address Circuit.....	77
9.11.6 Vertical Scroll Mode	77
9.11.7 Vertical Scroll Example	78
9.11.8 Case 1: TFA + VSA + BFA<162	78
9.11.9 Case 2: TFA + VSA + BFA=162 (Rolling Scrolling)	79
9.12 Tearing Effect Output Line	80
9.12.1 Tearing Effect Line Modes	80
9.12.2 Tearing Effect Line Timings	81
9.12.3 Example 1: MPU Write is faster than panel read	82
9.12.4 Example 2: MPU Write is slower than panel read.....	83
9.13 Power ON/OFF Sequence	84
9.13.1 Uncontrolled Power Off	85
9.14 Power Level Definition	86
9.14.1 Power Level.....	86
9.14.2 Power Flow Chart.....	87
9.15 Reset Table	88
9.15.1 Reset Table(Default Value, GM[1:0]="11", 128RGB x 160).....	88
9.15.2 Reset Table (GM[1:0]= "01", 132RGB x 132)	89
9.15.3 Reset Table (GM[1:0]= "00", 132RGB x 162)	90
9.16 Module Input/Output Pins	91
9.16.1 Output or Bi-directional (I/O) Pins	91
9.17 Reset Timing.....	92
9.18 Color Depth Conversion Look Up Tables.....	93
9.18.1 65536 Color to 262,144 Color	93
9.18.2 4096 Color to 262,144 Color	97
9.19 Sleep Out-Command and Self-Diagnostic Functions of the Display Module	99
9.19.1 Register Loading Detection.....	99
9.19.2 Functionality Detection.....	100
9.19.3 Chip Attachment Detection (Optional)	101
9.19.4 Display Glass Break Detection (Optional).....	102

10	COMMAND.....	103
10.1	System Function Command List and Description	103
10.1.1	NOP (00h)	106
10.1.2	SWRESET (01h): Software Reset	107
10.1.3	RDDID (04h): Read Display ID	108
10.1.4	RDDST (09h): Read Display Status.....	109
10.1.5	RDDPM (0Ah): Read Display Power Mode	111
10.1.6	RDDMADCTL (0Bh): Read Display MADCTL	112
10.1.7	RDDCOLMOD (0Ch): Read Display Pixel Format.....	113
10.1.8	RDDIM (0Dh): Read Display Image Mode.....	114
10.1.9	RDDSM (0Eh): Read Display Signal Mode.....	115
10.1.10	RDDSDR (0Fh): Read Display Self-Diagnostic Result	117
10.1.11	SLPIN (10h): Sleep In	118
10.1.12	SLPOUT (11h): Sleep Out	119
10.1.13	PTLON (12h): Partial Display Mode On	120
10.1.14	NORON (13h): Normal Display Mode On	121
10.1.15	INVOFF (20h): Display Inversion Off	122
10.1.16	INVON (21h): Display Inversion On	123
10.1.17	GAMSET (26h): Gamma Set	124
10.1.18	DISPOFF (28h): Display Off.....	125
10.1.19	DISPON (29h): Display On	126
10.1.20	CASET (2Ah): Column Address Set	127
10.1.21	RASET (2Bh): Row Address Set	129
10.1.22	RAMWR (2Ch): Memory Write.....	131
10.1.23	RGBSET (2Dh): Color Setting for 4K, 65K and 262K	132
10.1.24	RAMRD (2Eh): Memory Read	133
10.1.25	PTLAR (30h): Partial Area	134
10.1.26	SCRLAR (33h): Scroll Area Set	136
10.1.27	TEOFF (34h): Tearing Effect Line OFF	138
10.1.28	TEON (35h): Tearing Effect Line ON	139
10.1.29	MADCTL (36h): Memory Data Access Control	141
10.1.30	VSCSAD (37h): Vertical Scroll Start Address of RAM	144
10.1.31	IDMOFF (38h): Idle Mode Off	146
10.1.32	IDMON (39h) : Idle Mode On	147
10.1.33	COLMOD (3Ah): Interface Pixel Format	149
10.1.34	RDID1 (Dah): Read ID1 Value	150
10.1.35	RDID2 (DBh): Read ID2 Value.....	151
10.1.36	RDID3 (DCh): Read ID3 Value	152

10.2 Panel Function Command List and Description	153
10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)	157
10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)	158
10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)	159
10.2.4 INVCTR (B4h): Display Inversion Control	160
10.2.5 PWCTR1 (C0h): Power Control 1	161
10.2.6 PWCTR2 (C1h): Power Control 2	163
10.2.7 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors).....	165
10.2.8 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)	167
10.2.9 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)	169
10.2.10 VMCTR (C5h): VCOM Control	171
10.2.11 VMOFCTR (C7h): VCOM Offset Control	173
10.2.12 NVFCTR1 (D7h): NVM Enable Command.....	175
10.2.13 NVFCTR2 (D8h): Set Address for NVM.....	176
10.2.14 NVFCTR3 (D9h): Set Data for NVM	177
10.2.15 NVFCTR4 (DFh): NVM Write Command	178
10.2.16 NVFCTR5 (FDh): Custom Mode Enable Command	179
10.2.17 GMCTRP (E0h): Gamma ('+'polarity) Correction Characteristics Setting	180
10.2.18 GMCTRN (E1h): Gamma '-'polarity Correction Characteristics Setting	182
10.2.19 GCV(FCh): Gate Pump Clock Frequency Variable	184
11 Power Structure	185
11.1 Driver IC Operating Voltage Specification.....	185
11.2 Power Booster Circuit	186
12 Gamma Structure.....	187
12.1 Structure of Grayscale Amplifier	187
12.2 Gamma Voltage Formula (Positive/ Negative Polarity)	188
13 Example Connection with Panel Direction and Different Resolution	190
13.1 Application of Connection with Panel Direction.....	190
13.2 Application of Connection with Different Resolution.....	192
13.3 Microprocessor Interface Applications	195
13.3.1 8080-Series MCU Interface for 8-bit Data Bus (P68=0, IM2, IM1, IM0="100").....	195
13.3.2 8080-Series MCU Interface for 16-bit Data Bus (P68=0, IM2, IM1, IM0="101").....	195
13.3.3 8080-Series MCU Interface for 9-bit Data Bus (P68=0, IM2, IM1, IM0="110").....	195
13.3.4 8080-Series MCU Interface for 18-bit Data Bus (P68=0, IM2, IM1, IM0="111").....	196
13.3.5 3-Line Serial MCU Interface (IM2, IM1, IM0="000", SPI4W=0)	196
13.3.6 4-Line Serial MCU Interface (IM2, IM1, IM0="000", SPI4W=1)	196
14 Revision History	197

LIST OF FIGURES

Figure 1 Parallel Interface Timing Characteristics (8080 Series MCU Interface)	30
Figure 2 Rising And Falling Timing for Input And Output Signal	31
Figure 3 Chip Selection (CSX) Timing.....	31
Figure 4 Write-to-Read And Read-to-Write Timing	31
Figure 5 Parallel Interface Timing Characteristics (6800-Series MCU Interface)	32
Figure 6 3-line Serial Interface Timing.....	34
Figure 7 4-line Serial Interface Timing.....	35
Figure 8 8080-series WRX Protocol	38
Figure 9 8080-series Parallel Bus Protocol, Write to Register or Display RAM	38
Figure 10 8080-series RDX Protocol.....	39
Figure 11 8080-series Parallel Bus Protocol, Read Data from Register or Display RAM	39
Figure 12 6800-series Write Protocol	41
Figure 13 6800-series Parallel Bus Protocol, Write to Register or Display RAM	41
Figure 14 6800-series Read Protocol.....	42
Figure 15 6800-series Parallel Bus Protocol, Read Data form Register or Display RAM	42
Figure 16 Serial Interface Data Stream Format	43
Figure 17 3-line Serial Interface Write Protocol (Write to Register with Control Bit in Transmission).....	44
Figure 18 4-line Serial Interface Write Protocol (Write to Register with Control Bit in Transmission).....	44
Figure 19 3-line Serial Interface Read Protocol	45
Figure 20 4-line Serial Interface Read Protocol	46
Figure 21 Serial Bus Protocol, Write Mode–Interrupted by RESX	47
Figure 22 Serial Bus Protocol, Write Mode–Interrupted by CSX	47
Figure 23 Write Interrupts Recovery (Serial Interface).....	48
Figure 24 Write Interrupts Recovery (Both Serial and Parallel Interface)	48
Figure 25 Serial Interface Pause Protocol (Pause by CSX).....	49
Figure 26 Parallel Bus Pause Protocol (Paused by CSX).....	49
Figure 27 Display Data RAM Organization.....	66
Figure 28 Data Streaming order	74

LIST OF TABLES

Table 1 Absolute Operation Range	27
Table 2 DC Characteristic.....	28
Table 3 Power Consumption	29
Table 4 8080 Parallel Interface Characteristics.....	31
Table 5 6800 Parallel Interface Characteristics.....	33
Table 6 3-line Serial Interface Characteristics.....	34
Table 7 4-line Serial Interface Characteristics.....	35
Table 8 Interface Type Selection	36
Table 9 Pin Connection According to Various MCU Interface.....	36
Table 10 The Function of 8080-series Parallel Interface.....	37
Table 11 The Function of 6800-series Parallel Interface.....	40
Table 12 Selection of Serial Interface.....	43
Table 13 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C).....	81
Table 14 Reset Timing.....	92
Table 15 System Function Command List (1)	103
Table 16 System Function Command List (2)	104
Table 17 System Function command List (3).....	105
Table 18 Panel Function Command List (1).....	153
Table 19 Panel Function Command List (2).....	154
Table 20 Panel Function Command List (3).....	155
Table 21 Panel Function Command List (4).....	156

1 GENERAL DESCRIPTION

The ST7735P3 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 396 source line and 162 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bit/9-bit/16-bit/18-bit parallel interface. Display data can be stored in the on-chip display data RAM of 132 x 162 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

2 FEATURES

Single Chip TFT-LCD Controller/Driver with RAM On-chip Display Data RAM (i.e. Frame Memory)

132 (H) x RGB x 162 (V) Bits

LCD Driver Output Circuits:

Source Outputs: 132 RGB Channels

Gate Outputs: 162 Channels

Common Electrode Output

Display Colors (Color Mode)

Full Color: 262K, RGB=(666) Max., Idle Mode OFF

Color Reduce: 8-color, RGB=(111), Idle Mode ON

Programmable Pixel Color Format (Color Depth) for Various Display Data input Format

12-bit/pixel: RGB=(444) Using the 384k-bit Frame Memory and LUT

16-bit/pixel: RGB=(565) Using the 384k-bit Frame Memory and LUT

18-bit/pixel: RGB=(666) Using the 384k-bit Frame Memory and LUT

Various Interfaces

Parallel 8080-series MCU Interface

(8-bit, 9-bit, 16-bit & 18-bit)

Parallel 6800-series MCU Interface

(8-bit, 9-bit, 16-bit & 18-bit)

3-line Serial Interface

4-line Serial Interface

Display Features

Support Both Normal-black & Normal-white LC

Software Programmable Color Depth Mode

Partial Window Moving & Data Scrolling

Built-in Circuits

DC/DC Converter

Adjustable VCOM Generation

Non-volatile (NV) Memory to Store Initial Register Setting

Oscillator for Display Clock Generation

Factory default value (module ID, module version, etc.) are stored in NV memory.

Timing Controller

Built-in NV Memory for LCD Initial Register Setting

8-bits for ID1

8-bits for ID2

8-bits for ID3

5-bits for VCOM Offset Adjustment

Wide Supply Voltage Range

I/O Voltage (VDDI to DGND): 1.65V~3.7V ($VDDI \leq VDD$)

Analog Voltage (VDD to AGND): 2.5V~3.7V

On-Chip Power System

Source Voltage (GVDD to AGND): 3.15 V to 4.7 V

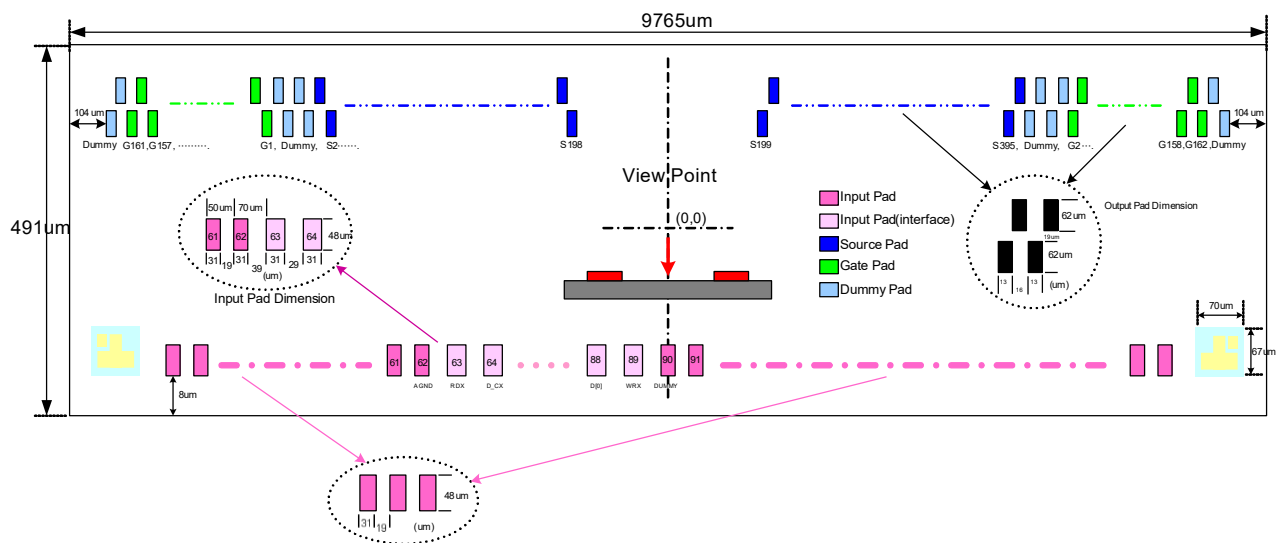
VCOM level (VCOM to AGND): -0.425 V to -2 V

Gate Driver HIGH Level (VGH to AGND): +10.0V to +15V

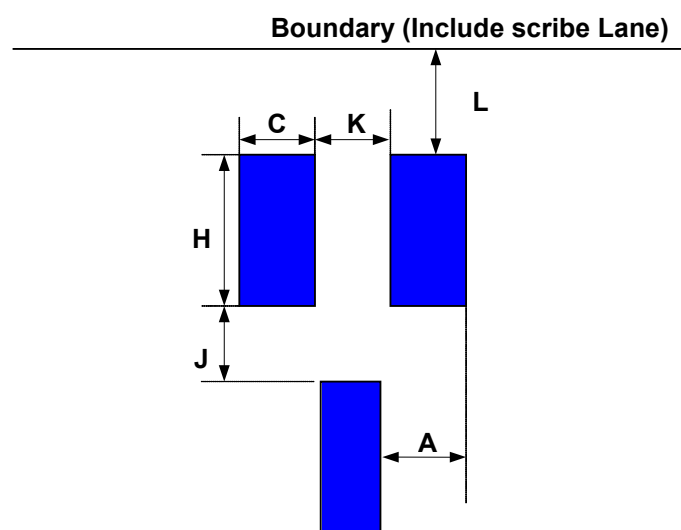
Gate Driver LOW Level (VGL to AGND): -13V to -7.5V

Operating Temperature: -30°C to +85°C

3 PAD ARRANGEMENT

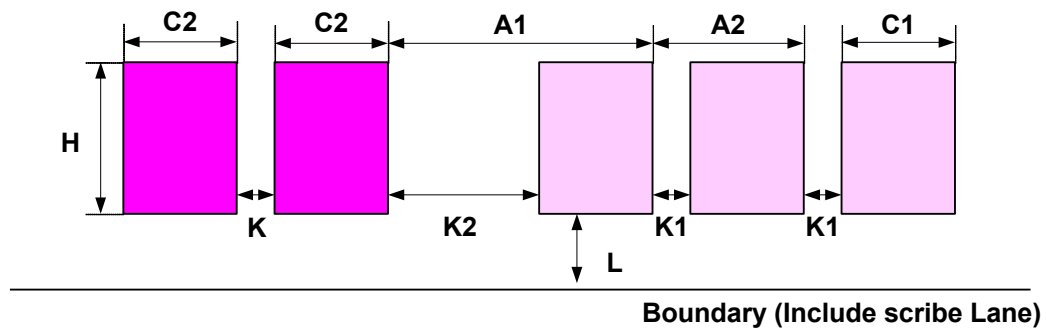


3.1 Output Bump Dimension



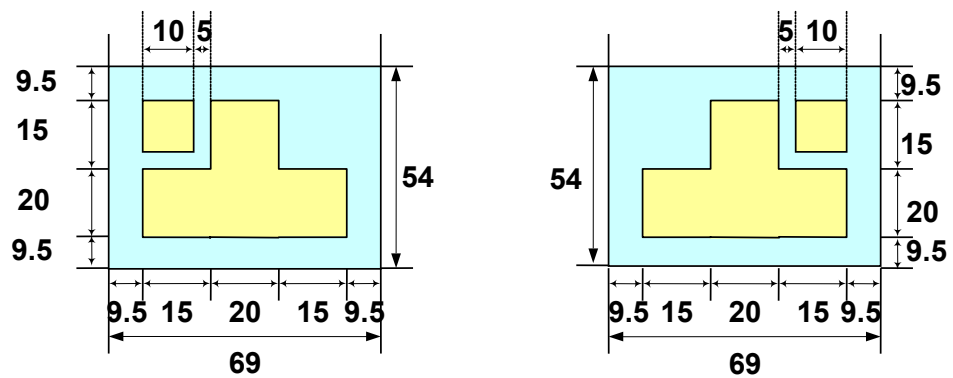
Item	Symbol	Size
Bump Pitch	A	16 um
Bump Width	C	13 um
Bump Height	H	62 um
Bump Gap1 (Vertical)	J	19 um
Bump Gap2 (Horizontal)	K	19 um
Bump Area	C x H	806 um ²
Chip Boundary (Include Scribe Lane)	L	7 um

3.2 Input Bump Dimension

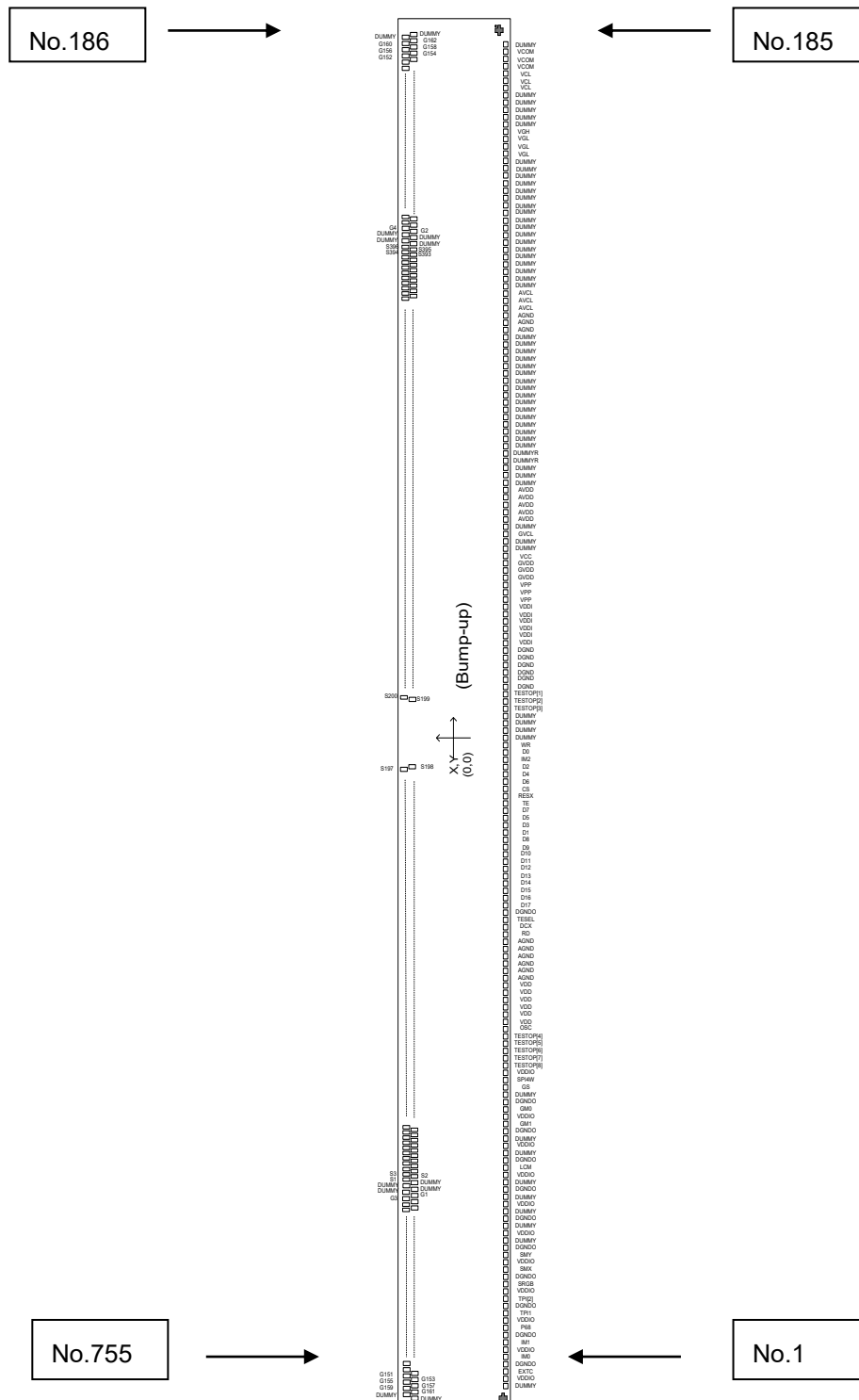


Item	Symbol	Size
Bump Pitch 1	A1	70 um
Bump Pitch 2	A2	60 um
Bump Width 1	C1	31 um
Bump Width 2	C2	31 um
Bump Height	H	48 um
Bump Gap	K	19 um
Bump Gap1	K1	29 um
Bump Gap2	K2	39 um
Bump Area 1	C1 X H	1488 um ²
Bump Area 2	C2 X H	1488 um ²
Chip Boundary(Include Scribe Lane)	L	8 um

3.3 Alignment Mark Dimension



Bump Hardness (HV): 90(TYP)



4 PAD CENTER COORDINATES

No.	PAD Name	X	Y
1	Dummy	-4750	-213.5
2	VDDIO	-4700	-213.5
3	EXTC	-4650	-213.5
4	DGNDO	-4600	-213.5
5	IM0	-4550	-213.5
6	VDDIO	-4500	-213.5
7	IM1	-4450	-213.5
8	DGNDO	-4400	-213.5
9	P68	-4350	-213.5
10	VDDIO	-4300	-213.5
11	TEST1P	-4250	-213.5
12	DGNDO	-4200	-213.5
13	TEST2P	-4150	-213.5
14	VDDIO	-4100	-213.5
15	SRGB	-4050	-213.5
16	DGNDO	-4000	-213.5
17	SMX	-3950	-213.5
18	VDDIO	-3900	-213.5
19	SMY	-3850	-213.5
20	DGNDO	-3800	-213.5
21	Dummy	-3750	-213.5
22	VDDIO	-3700	-213.5
23	Dummy	-3650	-213.5
24	DGNDO	-3600	-213.5
25	Dummy	-3550	-213.5
26	VDDIO	-3500	-213.5
27	Dummy	-3450	-213.5
28	DGNDO	-3400	-213.5
29	Dummy	-3350	-213.5
30	VDDIO	-3300	-213.5
31	LCM	-3250	-213.5
32	DGNDO	-3200	-213.5
33	DUMMY	-3150	-213.5
34	VDDIO	-3100	-213.5
35	Dummy	-3050	-213.5
36	DGNDO	-3000	-213.5
37	GM1	-2950	-213.5
38	VDDIO	-2900	-213.5
39	GM0	-2850	-213.5
40	DGNDO	-2800	-213.5
41	Dummy	-2750	-213.5
42	GS	-2700	-213.5
43	SPI4W	-2650	-213.5
44	VDDIO	-2600	-213.5
45	TESTOP[8]	-2550	-213.5
46	TESTOP[7]	-2500	-213.5
47	TESTOP[6]	-2450	-213.5
48	TESTOP[5]	-2400	-213.5
49	TESTOP[4]	-2350	-213.5
50	OSCP	-2300	-213.5

No.	PAD Name	X	Y
51	VDD	-2250	-213.5
52	VDD	-2200	-213.5
53	VDD	-2150	-213.5
54	VDD	-2100	-213.5
55	VDD	-2050	-213.5
56	VDD	-2000	-213.5
57	AGND	-1950	-213.5
58	AGND	-1900	-213.5
59	AGND	-1850	-213.5
60	AGND	-1800	-213.5
61	AGND	-1750	-213.5
62	AGND	-1700	-213.5
63	RDX	-1630	-213.5
64	D_CX	-1570	-213.5
65	TESEL	-1510	-213.5
66	DGNDO	-1450	-213.5
67	D17	-1390	-213.5
68	D16	-1330	-213.5
69	D15	-1270	-213.5
70	D14	-1210	-213.5
71	D13	-1150	-213.5
72	D12	-1090	-213.5
73	D11	-1030	-213.5
74	D10	-970	-213.5
75	D9	-910	-213.5
76	D8	-850	-213.5
77	D1	-790	-213.5
78	D3	-730	-213.5
79	D5	-670	-213.5
80	D7	-610	-213.5
81	TE	-550	-213.5
82	RESX	-490	-213.5
83	CSX	-430	-213.5
84	D6	-370	-213.5
85	D4	-310	-213.5
86	D2	-250	-213.5
87	IM2	-190	-213.5
88	D0	-130	-213.5
89	WRX	-70	-213.5
90	Dummy	0	-213.5
91	Dummy	50	-213.5
92	Dummy	100	-213.5
93	Dummy	150	-213.5
94	TESTOP[3]	200	-213.5
95	TESTOP[2]	250	-213.5
96	TESTOP[1]	300	-213.5
97	DGND	350	-213.5
98	DGND	400	-213.5
99	DGND	450	-213.5
100	DGND	500	-213.5

No.	PAD Name	X	Y
101	DGND	550	-213.5
102	DGND	600	-213.5
103	VDDI	650	-213.5
104	VDDI	700	-213.5
105	VDDI	750	-213.5
106	VDDI	800	-213.5
107	VDDI	850	-213.5
108	VDDI	900	-213.5
109	VPP	950	-213.5
110	VPP	1000	-213.5
111	VPP	1050	-213.5
112	GVDD	1100	-213.5
113	GVDD	1150	-213.5
114	GVDD	1200	-213.5
115	VCC	1250	-213.5
116	VCC	1300	-213.5
117	VCC	1350	-213.5
118	GVCL	1400	-213.5
119	Dummy	1450	-213.5
120	AVDD	1500	-213.5
121	AVDD	1550	-213.5
122	AVDD	1600	-213.5
123	AVDD	1650	-213.5
124	AVDD	1700	-213.5
125	Dummy	1750	-213.5
126	Dummy	1800	-213.5
127	Dummy	1850	-213.5
128	DummyR	1900	-213.5
129	DummyR	1950	-213.5
130	Dummy	2000	-213.5
131	Dummy	2050	-213.5
132	Dummy	2100	-213.5
133	Dummy	2150	-213.5
134	Dummy	2200	-213.5
135	Dummy	2250	-213.5
136	Dummy	2300	-213.5
137	Dummy	2350	-213.5
138	Dummy	2400	-213.5
139	Dummy	2450	-213.5
140	Dummy	2500	-213.5
141	Dummy	2550	-213.5
142	Dummy	2600	-213.5
143	Dummy	2650	-213.5
144	Dummy	2700	-213.5
145	Dummy	2750	-213.5
146	AGND	2800	-213.5
147	AGND	2850	-213.5
148	AGND	2900	-213.5
149	AVCL	2950	-213.5
150	AVCL	3000	-213.5

No.	PAD Name	X	Y
151	AVCL	3050	-213.5
152	Dummy	3100	-213.5
153	Dummy	3150	-213.5
154	Dummy	3200	-213.5
155	Dummy	3250	-213.5
156	Dummy	3300	-213.5
157	Dummy	3350	-213.5
158	Dummy	3400	-213.5
159	Dummy	3450	-213.5
160	Dummy	3500	-213.5
161	Dummy	3550	-213.5
162	Dummy	3600	-213.5
163	Dummy	3650	-213.5
164	Dummy	3700	-213.5
165	Dummy	3750	-213.5
166	Dummy	3800	-213.5
167	Dummy	3850	-213.5
168	Dummy	3900	-213.5
169	Dummy	3950	-213.5
170	VGL	4000	-213.5
171	VGL	4050	-213.5
172	VGL	4100	-213.5
173	VGH	4150	-213.5
174	Dummy	4200	-213.5
175	Dummy	4250	-213.5
176	Dummy	4300	-213.5
177	Dummy	4350	-213.5
178	Dummy	4400	-213.5
179	VCL	4450	-213.5
180	VCL	4500	-213.5
181	VCL	4550	-213.5
182	VCOM	4600	-213.5
183	VCOM	4650	-213.5
184	VCOM	4700	-213.5
185	Dummy	4750	-213.5
186	Dummy	4772	126.5
187	Dummy	4756	207.5
188	G162	4740	126.5
189	G160	4724	207.5
190	G158	4708	126.5
191	G156	4692	207.5
192	G154	4676	126.5
193	G152	4660	207.5
194	G150	4644	126.5
195	G148	4628	207.5
196	G146	4612	126.5
197	G144	4596	207.5
198	G142	4580	126.5
199	G140	4564	207.5
200	G138	4548	126.5

No.	PAD Name	X	Y
201	G136	4532	207.5
202	G134	4516	126.5
203	G132	4500	207.5
204	G130	4484	126.5
205	G128	4468	207.5
206	G126	4452	126.5
207	G124	4436	207.5
208	G122	4420	126.5
209	G120	4404	207.5
210	G118	4388	126.5
211	G116	4372	207.5
212	G114	4356	126.5
213	G112	4340	207.5
214	G110	4324	126.5
215	G108	4308	207.5
216	G106	4292	126.5
217	G104	4276	207.5
218	G102	4260	126.5
219	G100	4244	207.5
220	G98	4228	126.5
221	G96	4212	207.5
222	G94	4196	126.5
223	G92	4180	207.5
224	G90	4164	126.5
225	G88	4148	207.5
226	G86	4132	126.5
227	G84	4116	207.5
228	G82	4100	126.5
229	G80	4084	207.5
230	G78	4068	126.5
231	G76	4052	207.5
232	G74	4036	126.5
233	G72	4020	207.5
234	G70	4004	126.5
235	G68	3988	207.5
236	G66	3972	126.5
237	G64	3956	207.5
238	G62	3940	126.5
239	G60	3924	207.5
240	G58	3908	126.5
241	G56	3892	207.5
242	G54	3876	126.5
243	G52	3860	207.5
244	G50	3844	126.5
245	G48	3828	207.5
246	G46	3812	126.5
247	G44	3796	207.5
248	G42	3780	126.5
249	G40	3764	207.5
250	G38	3748	126.5

No.	PAD Name	X	Y
251	G36	3732	207.5
252	G34	3716	126.5
253	G32	3700	207.5
254	G30	3684	126.5
255	G28	3668	207.5
256	G26	3652	126.5
257	G24	3636	207.5
258	G22	3620	126.5
259	G20	3604	207.5
260	G18	3588	126.5
261	G16	3572	207.5
262	G14	3556	126.5
263	G12	3540	207.5
264	G10	3524	126.5
265	G8	3508	207.5
266	G6	3492	126.5
267	G4	3476	207.5
268	G2	3460	126.5
269	Dummy	3444	207.5
270	Dummy	3428	126.5
271	Dummy	3412	207.5
272	Dummy	3396	126.5
273	S396	3380	207.5
274	S395	3364	126.5
275	S394	3348	207.5
276	S393	3332	126.5
277	S392	3316	207.5
278	S391	3300	126.5
279	S390	3284	207.5
280	S389	3268	126.5
281	S388	3252	207.5
282	S387	3236	126.5
283	S386	3220	207.5
284	S385	3204	126.5
285	S384	3188	207.5
286	S383	3172	126.5
287	S382	3156	207.5
288	S381	3140	126.5
289	S380	3124	207.5
290	S379	3108	126.5
291	S378	3092	207.5
292	S377	3076	126.5
293	S376	3060	207.5
294	S375	3044	126.5
295	S374	3028	207.5
296	S373	3012	126.5
297	S372	2996	207.5
298	S371	2980	126.5
299	S370	2964	207.5
300	S369	2948	126.5

No.	PAD Name	X	Y
301	S368	2932	207.5
302	S367	2916	126.5
303	S366	2900	207.5
304	S365	2884	126.5
305	S364	2868	207.5
306	S363	2852	126.5
307	S362	2836	207.5
308	S361	2820	126.5
309	S360	2804	207.5
310	S359	2788	126.5
311	S358	2772	207.5
312	S357	2756	126.5
313	S356	2740	207.5
314	S355	2724	126.5
315	S354	2708	207.5
316	S353	2692	126.5
317	S352	2676	207.5
318	S351	2660	126.5
319	S350	2644	207.5
320	S349	2628	126.5
321	S348	2612	207.5
322	S347	2596	126.5
323	S346	2580	207.5
324	S345	2564	126.5
325	S344	2548	207.5
326	S343	2532	126.5
327	S342	2516	207.5
328	S341	2500	126.5
329	S340	2484	207.5
330	S339	2468	126.5
331	S338	2452	207.5
332	S337	2436	126.5
333	S336	2420	207.5
334	S335	2404	126.5
335	S334	2388	207.5
336	S333	2372	126.5
337	S332	2356	207.5
338	S331	2340	126.5
339	S330	2324	207.5
340	S329	2308	126.5
341	S328	2292	207.5
342	S327	2276	126.5
343	S326	2260	207.5
344	S325	2244	126.5
345	S324	2228	207.5
346	S323	2212	126.5
347	S322	2196	207.5
348	S321	2180	126.5
349	S320	2164	207.5
350	S319	2148	126.5

No.	PAD Name	X	Y
351	S318	2132	207.5
352	S317	2116	126.5
353	S316	2100	207.5
354	S315	2084	126.5
355	S314	2068	207.5
356	S313	2052	126.5
357	S312	2036	207.5
358	S311	2020	126.5
359	S310	2004	207.5
360	S309	1988	126.5
361	S308	1972	207.5
362	S307	1956	126.5
363	S306	1940	207.5
364	S305	1924	126.5
365	S304	1908	207.5
366	S303	1892	126.5
367	S302	1876	207.5
368	S301	1860	126.5
369	S300	1844	207.5
370	S299	1828	126.5
371	S298	1812	207.5
372	S297	1796	126.5
373	S296	1780	207.5
374	S295	1764	126.5
375	S294	1748	207.5
376	S293	1732	126.5
377	S292	1716	207.5
378	S291	1700	126.5
379	S290	1684	207.5
380	S289	1668	126.5
381	S288	1652	207.5
382	S287	1636	126.5
383	S286	1620	207.5
384	S285	1604	126.5
385	S284	1588	207.5
386	S283	1572	126.5
387	S282	1556	207.5
388	S281	1540	126.5
389	S280	1524	207.5
390	S279	1508	126.5
391	S278	1492	207.5
392	S277	1476	126.5
393	S276	1460	207.5
394	S275	1444	126.5
395	S274	1428	207.5
396	S273	1412	126.5
397	S272	1396	207.5
398	S271	1380	126.5
399	S270	1364	207.5
400	S269	1348	126.5

No.	PAD Name	X	Y
401	S268	1332	207.5
402	S267	1316	126.5
403	S266	1300	207.5
404	S265	1284	126.5
405	S264	1268	207.5
406	S263	1252	126.5
407	S262	1236	207.5
408	S261	1220	126.5
409	S260	1204	207.5
410	S259	1188	126.5
411	S258	1172	207.5
412	S257	1156	126.5
413	S256	1140	207.5
414	S255	1124	126.5
415	S254	1108	207.5
416	S253	1092	126.5
417	S252	1076	207.5
418	S251	1060	126.5
419	S250	1044	207.5
420	S249	1028	126.5
421	S248	1012	207.5
422	S247	996	126.5
423	S246	980	207.5
424	S245	964	126.5
425	S244	948	207.5
426	S243	932	126.5
427	S242	916	207.5
428	S241	900	126.5
429	S240	884	207.5
430	S239	868	126.5
431	S238	852	207.5
432	S237	836	126.5
433	S236	820	207.5
434	S235	804	126.5
435	S234	788	207.5
436	S233	772	126.5
437	S232	756	207.5
438	S231	740	126.5
439	S230	724	207.5
440	S229	708	126.5
441	S228	692	207.5
442	S227	676	126.5
443	S226	660	207.5
444	S225	644	126.5
445	S224	628	207.5
446	S223	612	126.5
447	S222	596	207.5
448	S221	580	126.5
449	S220	564	207.5
450	S219	548	126.5

No.	PAD Name	X	Y
451	S218	532	207.5
452	S217	516	126.5
453	S216	500	207.5
454	S215	484	126.5
455	S214	468	207.5
456	S213	452	126.5
457	S212	436	207.5
458	S211	420	126.5
459	S210	404	207.5
460	S209	388	126.5
461	S208	372	207.5
462	S207	356	126.5
463	S206	340	207.5
464	S205	324	126.5
465	S204	308	207.5
466	S203	292	126.5
467	S202	276	207.5
468	S201	260	126.5
469	S200	244	207.5
470	S199	228	126.5
471	S198	-228	126.5
472	S197	-244	207.5
473	S196	-260	126.5
474	S195	-276	207.5
475	S194	-292	126.5
476	S193	-308	207.5
477	S192	-324	126.5
478	S191	-340	207.5
479	S190	-356	126.5
480	S189	-372	207.5
481	S188	-388	126.5
482	S187	-404	207.5
483	S186	-420	126.5
484	S185	-436	207.5
485	S184	-452	126.5
486	S183	-468	207.5
487	S182	-484	126.5
488	S181	-500	207.5
489	S180	-516	126.5
490	S179	-532	207.5
491	S178	-548	126.5
492	S177	-564	207.5
493	S176	-580	126.5
494	S175	-596	207.5
495	S174	-612	126.5
496	S173	-628	207.5
497	S172	-644	126.5
498	S171	-660	207.5
499	S170	-676	126.5
500	S169	-692	207.5

No.	PAD Name	X	Y
501	S168	-708	126.5
502	S167	-724	207.5
503	S166	-740	126.5
504	S165	-756	207.5
505	S164	-772	126.5
506	S163	-788	207.5
507	S162	-804	126.5
508	S161	-820	207.5
509	S160	-836	126.5
510	S159	-852	207.5
511	S158	-868	126.5
512	S157	-884	207.5
513	S156	-900	126.5
514	S155	-916	207.5
515	S154	-932	126.5
516	S153	-948	207.5
517	S152	-964	126.5
518	S151	-980	207.5
519	S150	-996	126.5
520	S149	-1012	207.5
521	S148	-1028	126.5
522	S147	-1044	207.5
523	S146	-1060	126.5
524	S145	-1076	207.5
525	S144	-1092	126.5
526	S143	-1108	207.5
527	S142	-1124	126.5
528	S141	-1140	207.5
529	S140	-1156	126.5
530	S139	-1172	207.5
531	S138	-1188	126.5
532	S137	-1204	207.5
533	S136	-1220	126.5
534	S135	-1236	207.5
535	S134	-1252	126.5
536	S133	-1268	207.5
537	S132	-1284	126.5
538	S131	-1300	207.5
539	S130	-1316	126.5
540	S129	-1332	207.5
541	S128	-1348	126.5
542	S127	-1364	207.5
543	S126	-1380	126.5
544	S125	-1396	207.5
545	S124	-1412	126.5
546	S123	-1428	207.5
547	S122	-1444	126.5
548	S121	-1460	207.5
549	S120	-1476	126.5
550	S119	-1492	207.5

No.	PAD Name	X	Y
551	S118	-1508	126.5
552	S117	-1524	207.5
553	S116	-1540	126.5
554	S115	-1556	207.5
555	S114	-1572	126.5
556	S113	-1588	207.5
557	S112	-1604	126.5
558	S111	-1620	207.5
559	S110	-1636	126.5
560	S109	-1652	207.5
561	S108	-1668	126.5
562	S107	-1684	207.5
563	S106	-1700	126.5
564	S105	-1716	207.5
565	S104	-1732	126.5
566	S103	-1748	207.5
567	S102	-1764	126.5
568	S101	-1780	207.5
569	S100	-1796	126.5
570	S99	-1812	207.5
571	S98	-1828	126.5
572	S97	-1844	207.5
573	S96	-1860	126.5
574	S95	-1876	207.5
575	S94	-1892	126.5
576	S93	-1908	207.5
577	S92	-1924	126.5
578	S91	-1940	207.5
579	S90	-1956	126.5
580	S89	-1972	207.5
581	S88	-1988	126.5
582	S87	-2004	207.5
583	S86	-2020	126.5
584	S85	-2036	207.5
585	S84	-2052	126.5
586	S83	-2068	207.5
587	S82	-2084	126.5
588	S81	-2100	207.5
589	S80	-2116	126.5
590	S79	-2132	207.5
591	S78	-2148	126.5
592	S77	-2164	207.5
593	S76	-2180	126.5
594	S75	-2196	207.5
595	S74	-2212	126.5
596	S73	-2228	207.5
597	S72	-2244	126.5
598	S71	-2260	207.5
599	S70	-2276	126.5
600	S69	-2292	207.5

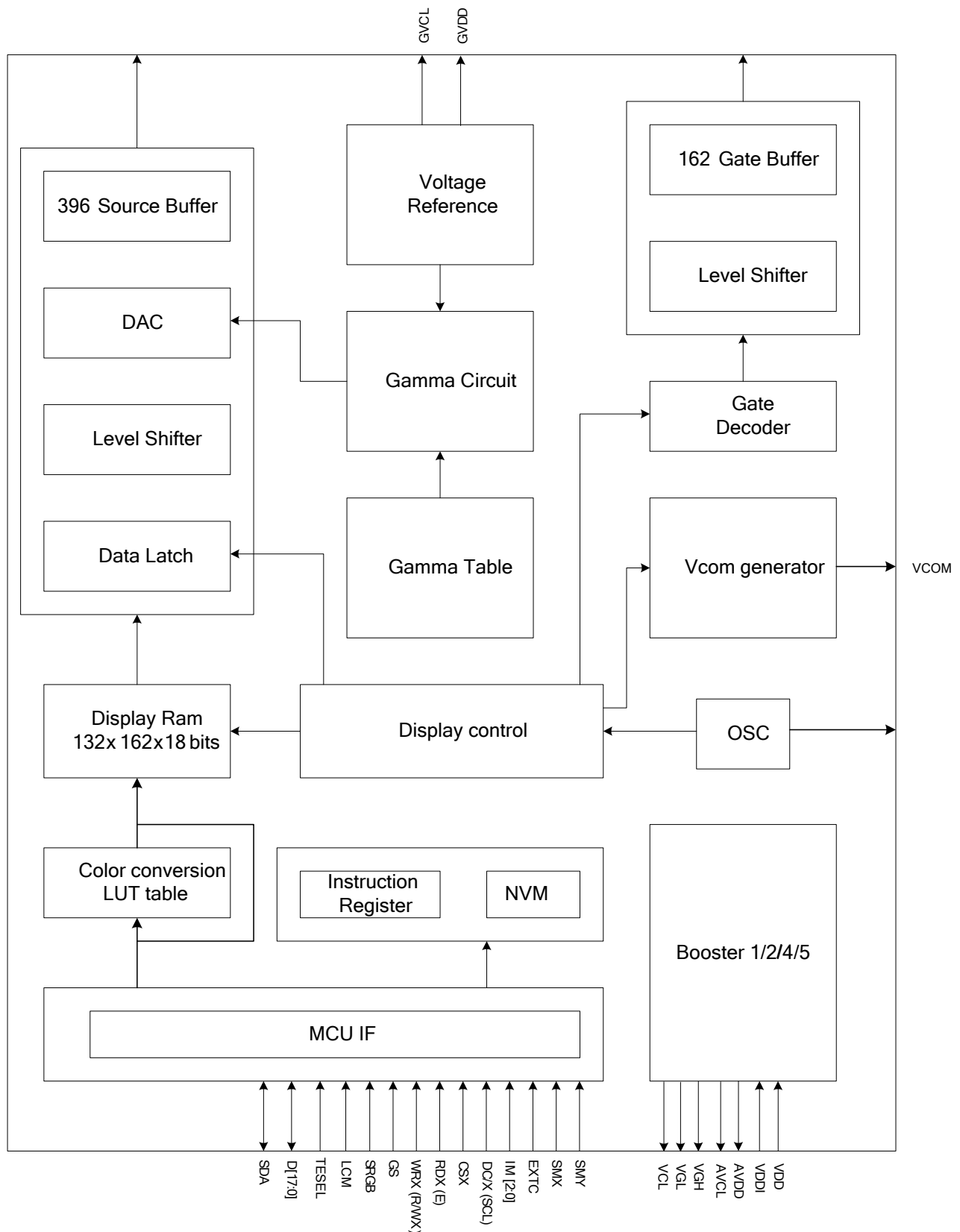
No.	PAD Name	X	Y
601	S68	-2308	126.5
602	S67	-2324	207.5
603	S66	-2340	126.5
604	S65	-2356	207.5
605	S64	-2372	126.5
606	S63	-2388	207.5
607	S62	-2404	126.5
608	S61	-2420	207.5
609	S60	-2436	126.5
610	S59	-2452	207.5
611	S58	-2468	126.5
612	S57	-2484	207.5
613	S56	-2500	126.5
614	S55	-2516	207.5
615	S54	-2532	126.5
616	S53	-2548	207.5
617	S52	-2564	126.5
618	S51	-2580	207.5
619	S50	-2596	126.5
620	S49	-2612	207.5
621	S48	-2628	126.5
622	S47	-2644	207.5
623	S46	-2660	126.5
624	S45	-2676	207.5
625	S44	-2692	126.5
626	S43	-2708	207.5
627	S42	-2724	126.5
628	S41	-2740	207.5
629	S40	-2756	126.5
630	S39	-2772	207.5
631	S38	-2788	126.5
632	S37	-2804	207.5
633	S36	-2820	126.5
634	S35	-2836	207.5
635	S34	-2852	126.5
636	S33	-2868	207.5
637	S32	-2884	126.5
638	S31	-2900	207.5
639	S30	-2916	126.5
640	S29	-2932	207.5
641	S28	-2948	126.5
642	S27	-2964	207.5
643	S26	-2980	126.5
644	S25	-2996	207.5
645	S24	-3012	126.5
646	S23	-3028	207.5
647	S22	-3044	126.5
648	S21	-3060	207.5
649	S20	-3076	126.5
650	S19	-3092	207.5

No.	PAD Name	X	Y
651	S18	-3108	126.5
652	S17	-3124	207.5
653	S16	-3140	126.5
654	S15	-3156	207.5
655	S14	-3172	126.5
656	S13	-3188	207.5
657	S12	-3204	126.5
658	S11	-3220	207.5
659	S10	-3236	126.5
660	S9	-3252	207.5
661	S8	-3268	126.5
662	S7	-3284	207.5
663	S6	-3300	126.5
664	S5	-3316	207.5
665	S4	-3332	126.5
666	S3	-3348	207.5
667	S2	-3364	126.5
668	S1	-3380	207.5
669	Dummy	-3396	126.5
670	Dummy	-3412	207.5
671	Dummy	-3428	126.5
672	Dummy	-3444	207.5
673	G1	-3460	126.5
674	G3	-3476	207.5
675	G5	-3492	126.5
676	G7	-3508	207.5
677	G9	-3524	126.5
678	G11	-3540	207.5
679	G13	-3556	126.5
680	G15	-3572	207.5
681	G17	-3588	126.5
682	G19	-3604	207.5
683	G21	-3620	126.5
684	G23	-3636	207.5
685	G25	-3652	126.5
686	G27	-3668	207.5
687	G29	-3684	126.5
688	G31	-3700	207.5
689	G33	-3716	126.5
690	G35	-3732	207.5
691	G37	-3748	126.5
692	G39	-3764	207.5
693	G41	-3780	126.5
694	G43	-3796	207.5
695	G45	-3812	126.5
696	G47	-3828	207.5
697	G49	-3844	126.5
698	G51	-3860	207.5
699	G53	-3876	126.5
700	G55	-3892	207.5

No.	PAD Name	X	Y
701	G57	-3908	126.5
702	G59	-3924	207.5
703	G61	-3940	126.5
704	G63	-3956	207.5
705	G65	-3972	126.5
706	G67	-3988	207.5
707	G69	-4004	126.5
708	G71	-4020	207.5
709	G73	-4036	126.5
710	G75	-4052	207.5
711	G77	-4068	126.5
712	G79	-4084	207.5
713	G81	-4100	126.5
714	G83	-4116	207.5
715	G85	-4132	126.5
716	G87	-4148	207.5
717	G89	-4164	126.5
718	G91	-4180	207.5
719	G93	-4196	126.5
720	G95	-4212	207.5
721	G97	-4228	126.5
722	G99	-4244	207.5
723	G101	-4260	126.5
724	G103	-4276	207.5
725	G105	-4292	126.5
726	G107	-4308	207.5
727	G109	-4324	126.5
728	G111	-4340	207.5
729	G113	-4356	126.5
730	G115	-4372	207.5
731	G117	-4388	126.5
732	G119	-4404	207.5
733	G121	-4420	126.5
734	G123	-4436	207.5
735	G125	-4452	126.5
736	G127	-4468	207.5
737	G129	-4484	126.5
738	G131	-4500	207.5
739	G133	-4516	126.5
740	G135	-4532	207.5
741	G137	-4548	126.5
742	G139	-4564	207.5
743	G141	-4580	126.5
744	G143	-4596	207.5
745	G145	-4612	126.5
746	G147	-4628	207.5
747	G149	-4644	126.5
748	G151	-4660	207.5
749	G153	-4676	126.5
750	G155	-4692	207.5

2021-08

5 BLOCK DIAGRAM



6 PIN DESCRIPTION

6.1 Power Supply Pin

Name	I/O	Description	Connect Pin
VDD	I	Power Supply for Analog, Digital System and Booster Circuit.	VDD
VDDI	I	Power Supply for I/O system.	VDDI
AGND	I	System Ground for Analog System and Booster Circuit.	GND
DGND	I	System Ground for I/O System and Digital System.	GND

6.2 Interface Logic Pin

Name	I/O	Description	Connect pin															
P68	I	-8080/6800 MCU Interface Mode Select. -P68='1', Select 6800 MCU Parallel Interface. -P68='0', Select 8080 MCU Parallel Interface. -If not used, Please Fix this Pin at DGND Level.	DGND/VDDI															
IM2	I	MCU Parallel Interface Bus and Serial Interface select IM2='1', Parallel Interface IM2='0', Serial Interface	DGND/VDDI															
IM1,IM0	I	- MCU Parallel Interface Type Selection -If Not Used, Please Fix this Pin at VDDI or DGND Level. <table border="1"><thead><tr><th>IM1</th><th>IM0</th><th>Parallel Interface</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>MCU 8-bit Parallel</td></tr><tr><td>0</td><td>1</td><td>MCU 16-bit Parallel</td></tr><tr><td>1</td><td>0</td><td>MCU 9-bit Parallel</td></tr><tr><td>1</td><td>1</td><td>MCU 18-bit Parallel</td></tr></tbody></table>	IM1	IM0	Parallel Interface	0	0	MCU 8-bit Parallel	0	1	MCU 16-bit Parallel	1	0	MCU 9-bit Parallel	1	1	MCU 18-bit Parallel	DGND/VDDI
IM1	IM0	Parallel Interface																
0	0	MCU 8-bit Parallel																
0	1	MCU 16-bit Parallel																
1	0	MCU 9-bit Parallel																
1	1	MCU 18-bit Parallel																
SPI4W	I	- SPI4W='0', 3-line SPI Enable. - SPI4W='1', 4-line SPI Enable. -If Not Used, Please fix this Pin at DGND Level.	DGND/VDDI															
RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	MCU															
CSX	I	-Chip Selection Pin -Low Enable.	MCU															

D/CX (SCL)	I	-Display data/command Selection Pin in MCU Interface. -D/CX='1': Display Data or Parameter. -D/CX='0': Command Data. -In Serial Interface, this is used as SCL. -If not used, please fix this pin at VDDI or DGND level.	MCU
RDX	I	-Read Enable in 8080 MCU Parallel Interface. -If not used, please fix this pin at VDDI or DGND level.	MCU
WRX (D/CX)	I	-Write Enable in MCU Parallel Interface. -In 4-line SPI, this pin is used as D/CX (data/ command selection). -If not used, please fix this pin at VDDI or DGND level.	MCU
D[17:0]	I/O	-D[17:0] are used as MCU parallel interface data bus. -D0 is the serial input/output signal in serial interface mode. -In serial interface, D[17:1] are not used and should be fixed at VDDI or DGND level.	MCU
TE	O	-Tearing effect output pin to synchronies MCU to frame rate, activated by S/W command. -If not used, please open this pin.	MCU
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. -When this pin is inactive (function OFF), this pin is DGND level. -If not used, please open this pin.	-

Note1. When in parallel mode, no use data pin must be connected to "1" or "0".

Note2. When CSX="1", there is no influence to the parallel and serial interface.

6.3 Mode Selection Pin

Name	I/O	Description	Connect Pin																
EXTC	I	- During normal operation, please connect to VDDI.. <table><tr><td>EXTC</td><td colspan="3">Enable/disable Modification of Extend Command</td></tr><tr><td>0</td><td colspan="3">Panel Function Commands Disable.</td></tr><tr><td>1</td><td colspan="3">Panel Function Commands Enable.</td></tr></table>	EXTC	Enable/disable Modification of Extend Command			0	Panel Function Commands Disable.			1	Panel Function Commands Enable.			VDDI/DGND				
EXTC	Enable/disable Modification of Extend Command																		
0	Panel Function Commands Disable.																		
1	Panel Function Commands Enable.																		
GM1, GM0	I	-Panel Resolution Selection Pins. <table><tr><td>GM1</td><td>GM0</td><td colspan="2">Selection of panel resolution</td></tr><tr><td>0</td><td>0</td><td colspan="2">132RGB x 162 (S1~S396 & G1~G162 output)</td></tr><tr><td>0</td><td>1</td><td colspan="2">132RGB x 132 (S1~S396 & G1~G132 Output)</td></tr><tr><td>1</td><td>1</td><td colspan="2">128RGB x 160 (S7~S390 & G2~G161 output)</td></tr></table>	GM1	GM0	Selection of panel resolution		0	0	132RGB x 162 (S1~S396 & G1~G162 output)		0	1	132RGB x 132 (S1~S396 & G1~G132 Output)		1	1	128RGB x 160 (S7~S390 & G2~G161 output)		VDDI/DGND
GM1	GM0	Selection of panel resolution																	
0	0	132RGB x 162 (S1~S396 & G1~G162 output)																	
0	1	132RGB x 132 (S1~S396 & G1~G132 Output)																	
1	1	128RGB x 160 (S7~S390 & G2~G161 output)																	
SRGB	I	-RGB Direction Select H/W Pin for Color Filter Setting. <table><tr><td>SRGB</td><td colspan="3">RGB Arrangement</td></tr><tr><td>0</td><td colspan="3">S1, S2, S3 Filter Order = 'R', 'G', 'B'</td></tr><tr><td>1</td><td colspan="3">S1, S2, S3 Filter Order = 'B', 'G', 'R'</td></tr></table>	SRGB	RGB Arrangement			0	S1, S2, S3 Filter Order = 'R', 'G', 'B'			1	S1, S2, S3 Filter Order = 'B', 'G', 'R'			VDDI/DGND				
SRGB	RGB Arrangement																		
0	S1, S2, S3 Filter Order = 'R', 'G', 'B'																		
1	S1, S2, S3 Filter Order = 'B', 'G', 'R'																		
SMX	I	-Module Source Output Direction H/W Selection Pin. <table><tr><td>SMX</td><td colspan="3">Scanning direction of source output</td></tr><tr><td></td><td>GM= '00'</td><td>GM= '01'</td><td>GM= '11'</td></tr><tr><td>0</td><td>S1 -> S396</td><td>S1 -> S396</td><td>S7 -> S390</td></tr><tr><td>1</td><td>S396 -> S1</td><td>S396 -> S1</td><td>S390 -> S7</td></tr></table>	SMX	Scanning direction of source output				GM= '00'	GM= '01'	GM= '11'	0	S1 -> S396	S1 -> S396	S7 -> S390	1	S396 -> S1	S396 -> S1	S390 -> S7	VDDI/DGND
SMX	Scanning direction of source output																		
	GM= '00'	GM= '01'	GM= '11'																
0	S1 -> S396	S1 -> S396	S7 -> S390																
1	S396 -> S1	S396 -> S1	S390 -> S7																
SMY	I	-Module Gate Output Direction H/W Selection Pin. <table><tr><td>SMY</td><td colspan="3">Scanning direction of gate output</td></tr><tr><td></td><td>GM= '00'</td><td>GM= '01'</td><td>GM= '11'</td></tr><tr><td>0</td><td>G1 -> G162</td><td>G1 -> G132</td><td>G2 -> G161</td></tr><tr><td>1</td><td>G162 -> G1</td><td>G132 -> G1</td><td>G161 -> G2</td></tr></table>	SMY	Scanning direction of gate output				GM= '00'	GM= '01'	GM= '11'	0	G1 -> G162	G1 -> G132	G2 -> G161	1	G162 -> G1	G132 -> G1	G161 -> G2	VDDI/DGND
SMY	Scanning direction of gate output																		
	GM= '00'	GM= '01'	GM= '11'																
0	G1 -> G162	G1 -> G132	G2 -> G161																
1	G162 -> G1	G132 -> G1	G161 -> G2																
LCM	I	-Liquid Crystal (LC) Type Selection Pins. <table><tr><td>LCM</td><td colspan="3">Selection of LC Type</td></tr><tr><td>0</td><td colspan="3">Normally White LC Type</td></tr><tr><td>1</td><td colspan="3">Normally Black LC Type</td></tr></table>	LCM	Selection of LC Type			0	Normally White LC Type			1	Normally Black LC Type			VDDI/DGND				
LCM	Selection of LC Type																		
0	Normally White LC Type																		
1	Normally Black LC Type																		
GS	I	-Gamma Curve Selection Pin. <table><tr><td>GS</td><td colspan="3">Selection of Gamma Curve</td></tr><tr><td>0</td><td colspan="3">GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8</td></tr><tr><td>1</td><td colspan="3">GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0</td></tr></table>	GS	Selection of Gamma Curve			0	GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8			1	GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0			VDDI/DGND				
GS	Selection of Gamma Curve																		
0	GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8																		
1	GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0																		

VPP	I	When writing NVM, it needs external power supply voltage (7.5V).							
TESEL	I	Input pin to select horizontal line number in TE signal. This pin is internally pull low. <table><tr><td>TESEL</td><td>Selection of gamma curve</td></tr><tr><td>0</td><td>TE output 162 lines</td></tr><tr><td>1</td><td>TE output 160 lines</td></tr></table>	TESEL	Selection of gamma curve	0	TE output 162 lines	1	TE output 160 lines	DGND
TESEL	Selection of gamma curve								
0	TE output 162 lines								
1	TE output 160 lines								

6.4 Driver Output pins

Name	I/O	Description	Connect Pin
S1 to S396	O	- Source Driver Output Pins.	-
G1 to G162	O	- Gate Driver Output Pins.	-
AVDD	O	- Power Pin for Analog Circuits.	-
AVCL	O	- A power Supply Pin for Generating GVCL.	-
VGH	O	- Power Output Pin for Gate Driver	-
VGL	O	- Power Output (Negative) Pin for Gate Driver	-
GVDD	O	- A power Output of Grayscale Voltage Generator. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	-
GVCL	O	- A power Output (Negative) of Grayscale Voltage Generator. - When internal GVCL generator is not used, connect an external power supply (AVCL+0.5V) to this pin.	-
VCOM	O	- A Power Supply for the TFT-LCD Common Electrode.	Common Electrode
VCC	O	- Monitoring Pin of Internal Digital Reference Voltage. - Please Open These Pins.	
VCL	O	- A power output of VCOM voltage (Negative) generator.	
VDDIO	O	- VDDI Voltage Output Level for Monitoring.	-
DGND0	O	- DGND Voltage Output Level for Monitoring.	-

6.5 Test Pins

Name	I/O	Description	Connect Pin
TEST2P TEST1P	I	-These test pins for driver vender test used. -Please connect these pins to DGND.	DGND
TESTOP[8] TESTOP[7] TESTOP[6] TESTOP[5] TESTOP[4] TESTOP[3] TESTOP[2] TESTOP[1]	O	-These test pins for driver vender test used. -Please open these pins.	Open
DummyR	-	-These pins are dummy (have no function inside). -Pad128 DummyR internal short to pad 129 DummyR.	Open
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass. -Please open these pins.	Open

7 DRIVER ELECTRICAL CHARACTERISTICS

7.1 Absolute Operation Range

Item	Symbol	Rating	Unit
Supply Voltage	VDD	- 0.3 ~ +4.6	V
Supply Voltage (Logic)	VDDI	- 0.3 ~ +4.6	V
Supply Voltage (Digital)	VCC	-0.3 ~ +1.95	V
Driver Supply Voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Input Voltage Range	VO	-0.3 ~ VDDI + 0.3	V
Operating Temperature Range	TOPR	-30 ~ +85	°C
Storage Temperature Range	TSTG	-40 ~ +125	°C

Table 1 Absolute Operation Range

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC Characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	Typ	Max		
Power & Operation Voltage							
System Voltage	VDD	Operating Voltage	2.5	2.75	3.7	V	
Interface Operation Voltage	VDDI	I/O Supply Voltage	1.65	1.8	3.7	V	
Gate Driver High Voltage	VGH		11		16	V	Note 4
Gate Driver Low Voltage	VGL		-13		-7.5	V	
Gate Driver Supply Voltage		VGH-VGL	18.5		29	V	Note 4
Input / Output							
Logic-High Input Voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-Low Input Voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-High Output Voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-Low Output Voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-High Input Current	IIH	VIN = VDDI			1	uA	Note 1
Logic-Low Input Current	IIL	VIN = VSS	-1			uA	Note 1
Input Leakage Current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM Voltage							
VCOM Amplitude	VCOM		-2		-0.425	V	
Source driver							
Source Output Range	Vsout		0.1		GVDD	V	
Gamma Reference Voltage	GVDD		3.15		4.7	V	
Source Output Settling Time	Tr	Below with 99% precision			20	us	Note 2
Output Offset Voltage	Voffset				35	mV	Note 3

Table 2 DC Characteristic

Notes:

1. TA= -30 to 85℃.
2. Source channel loading= 2KΩ+12pF/channel, Gate channel loading=5KΩ+40pF/channel.
3. The Max. value is between measured point of source output and gamma setting value.
4. VGH setting condition is AVDD=4.7V, the Max and Min VGH voltage depend on AVDD setting, VGH-VGL can not large than 30V.

7.3 Power Consumption

Ta=25°C, Frame rate = 60Hz, Bare die, the registers setting are IC default setting.

Operation Mode	Image	Current Consumption			
		Typical		Maximum	
		IDD (mA)	IDD (mA)	IDD (mA)	IDD (mA)
Normal Mode	Note 1	0.01	1.5	0.02	3
	Note 2	0.01	1.5	0.02	3
Partial + Idle Mode (40 lines)	Note 1	0.01	1.5	0.02	3
	Note 2	0.01	1.5	0.02	3
Sleep-In Mode	N/A	0.005	0.020	0.01	0.03

Table 3 Power Consumption

Notes:

1. All pixels black.
2. All pixels white.
3. The Current Consumption is DC characteristics of ST7735P3
4. Typical: VDDI=1.8V, VDD=2.75V; Maximum: VDDI=1.65 to 3.7V, VDD=2.5 to 3.7V

8 Timing chart

8.1 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (8080 Series MCU Interface)

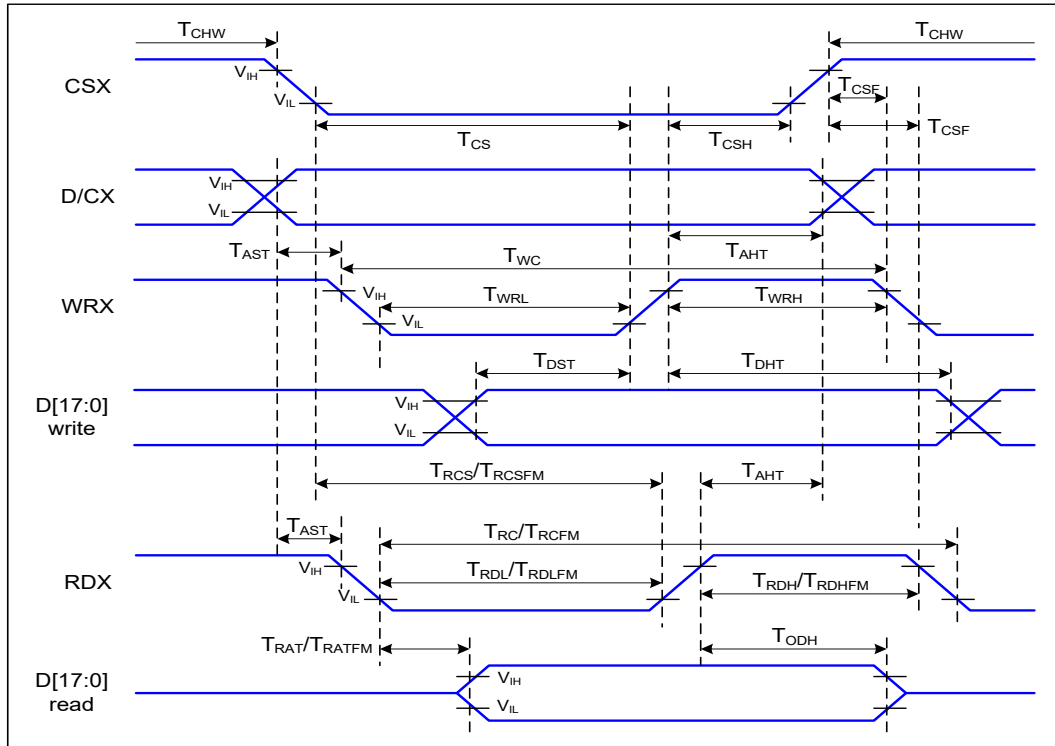


Figure 1 Parallel Interface Timing Characteristics (8080 Series MCU Interface)

T_a=25 °C, V_{DDI}=1.65~3.7V, V_{DD}=2.5~3.7V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	TAST	Address Setup Time	0		ns	-
	®	Address Hold Time (Write/Read)	10		ns	
CSX	TCHW	Chip Select "H" Pulse Width	0		ns	-
	TCS	Chip Select Setup Time (Write)	15		ns	
	TRCS	Chip Select Setup Time (Read ID)	45		ns	
	TRCSFM	Chip Select Setup time (Read FM)	355		ns	
	TCSF	Chip Select Wait Time (Write/Read)	10		ns	
	TCSH	Chip Select Hold Time	10		ns	
WRX	TWC	Write Cycle	66		ns	
	TWRH	Control Pulse "H" Duration	15		ns	
	TWRL	Control Pulse "L" Duration	15		ns	
RDX (ID)	TRC	Read Cycle (ID)	160		ns	When Read ID Data
	TRDH	Control Pulse "H" Duration (ID)	90		ns	
	TRDL	Control Pulse "L" Duration (ID)	45		ns	

RDX (FM)	TRCFM	Read Cycle (FM)	450		ns	When Read from Frame Memory
	TRDHFM	Control Pulse "H" Duration (FM)	90		ns	
	TRDLFM	Control Pulse "L" Duration (FM)	355		ns	
D[17:0]	TDST	Data Setup Time	10		ns	For CL=30pF
	TDHT	Data Hold Time	10		ns	
	TRAT	Read Access Time (ID)		40	ns	
	TRATFM	Read Access Time (FM)		340	ns	
	TODH	Output Disable Time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

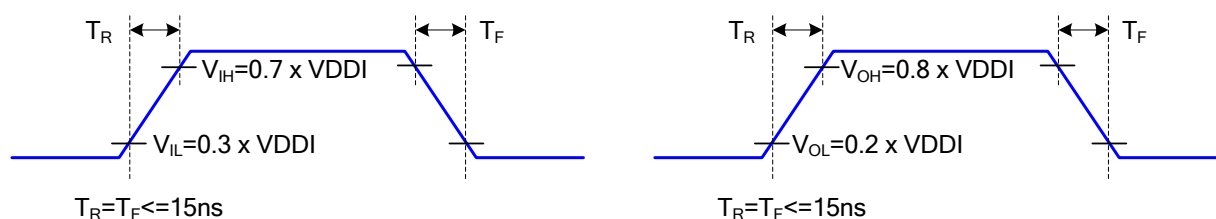


Figure 2 Rising And Falling Timing for Input And Output Signal

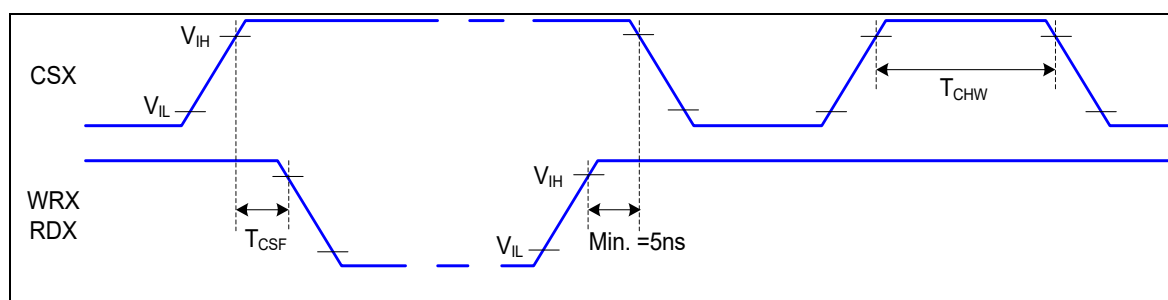


Figure 3 Chip Selection (CSX) Timing

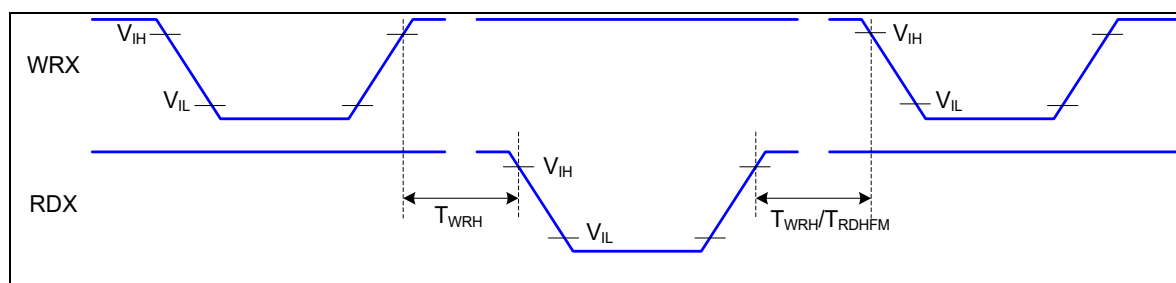


Figure 4 Write-to-Read And Read-to-Write Timing

Note: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.2 Parallel Interface Characteristics: 18, 16, 9 or 8-bit Bus (6800 Series MCU Interface)

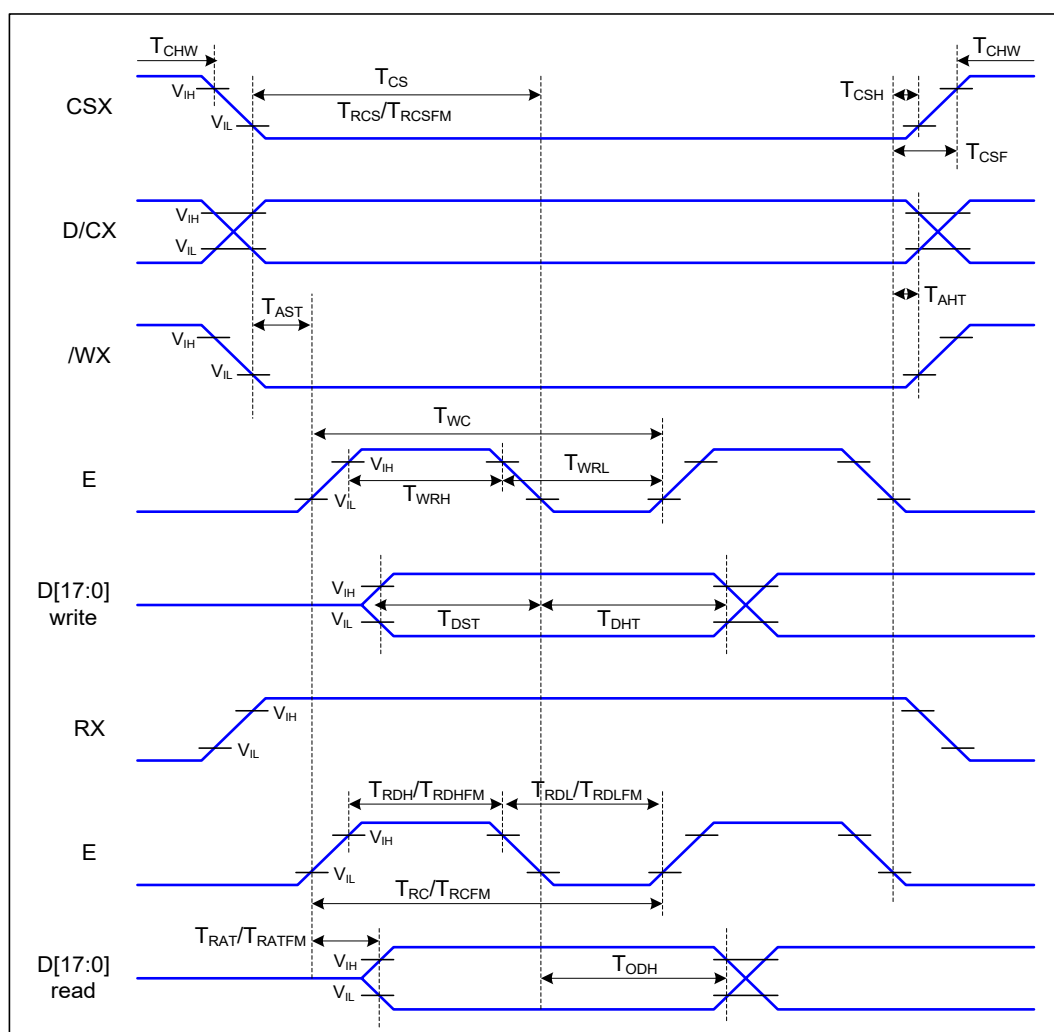


Figure 5 Parallel Interface Timing Characteristics (6800-Series MCU Interface)

Ta=25 °C, VDDI=1.65~3.7V, VDD=2.5~3.7V

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T _{AST}	Address Setup Time	0		ns	-
	Ⓜ	Address Hold Time (Write/Read)	10		ns	
CSX	T _{CHW}	Chip Select "H" Pulse Width	0		ns	-
	T _{CS}	Chip Select Setup Time (Write)	15		ns	
	T _{RCS}	Chip Select Setup Time (Read ID)	45		ns	
	T _{RCSFM}	Chip Select Setup Time (Read FM)	355		ns	
	T _{CSF}	Chip Select wait Time (Write/Read)	10		ns	
	T _{CSH}	Chip Select Hold Time	10		ns	
WRX	T _{WC}	Write Cycle	66		ns	-
	T _{WRH}	Control Pulse "H" Duration	15		ns	
	T _{WRL}	Control Pulse "L" Duration	15		ns	

RDX (ID)	T _{RC}	Read Cycle (ID)	160		ns	When Read ID Data
	T _{RDH}	Control Pulse "H" Duration (ID)	90		ns	
	T _{RDL}	Control Pulse "L" Duration (ID)	45		ns	
RDX (FM)	T _{RCFM}	Read Cycle (FM)	450		ns	When Read From Frame Memory
	T _{RDHFM}	Control Pulse "H" Duration (FM)	90		ns	
	T _{RDLFM}	Control Pulse "L" Duration (FM)	355		ns	
D[17:0]	T _{DST}	Data Setup Time	10		ns	For Maximum
	T _{DHT}	Data Hold Time	10		ns	CL=30pF
	T _{ODH}	Output Disable Time	20	80	ns	For Minimum CL=8pF

Table 5 6800 Parallel Interface Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

8.3 Serial Interface Characteristics (3-line Serial)

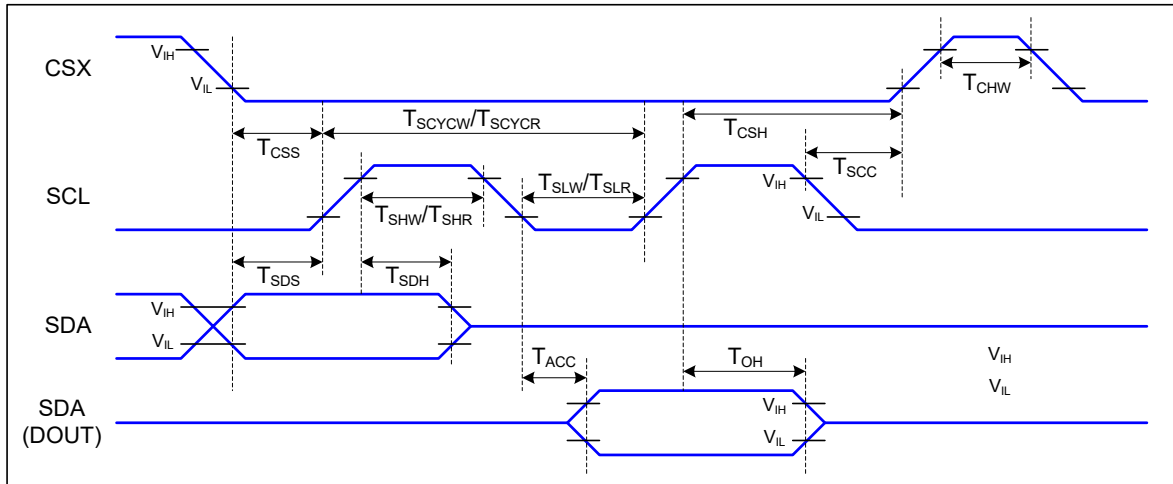


Figure 6 3-line Serial Interface Timing

Ta=25 °C, VDDI=1.65~3.7V, VDD=2.5~3.7V

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSS	Chip Select Setup Time (Write)	15		ns	
	TCSH	Chip Select Hold Time (Write)	15		ns	
	TCSS	Chip Select Setup Time (Read)	60		ns	
	TSCC	Chip Select Hold Time (Read)	65		ns	
	TCHW	Chip Select "H" pulse width	40		ns	
SCL	TSCYCW	Serial Clock Cycle (Write)	20		ns	
	TSHW	SCL "H" Pulse Width (Write)	10		ns	
	TSLW	SCL "L" Pulse Width (Write)	10		ns	
	TSCYCR	Serial Clock Cycle (Read)	150		ns	
	TSHR	SCL "H" Pulse Width (Read)	60		ns	
	TS LR	SCL "L" Pulse Width (Read)	60		ns	
SDA (DIN) (DOUT)	TSDS	Data Setup Time	10		ns	For Maximum CL=30pF For Minimum CL=8pF
	TSDH	Data Hold Time	10		ns	
	TACC	Access Time	10	50	ns	
	TOH	Output Disable Time	15	50	ns	

Table 6 3-line Serial Interface Characteristics

Note : The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.4 Serial Interface Characteristics (4-line Serial)

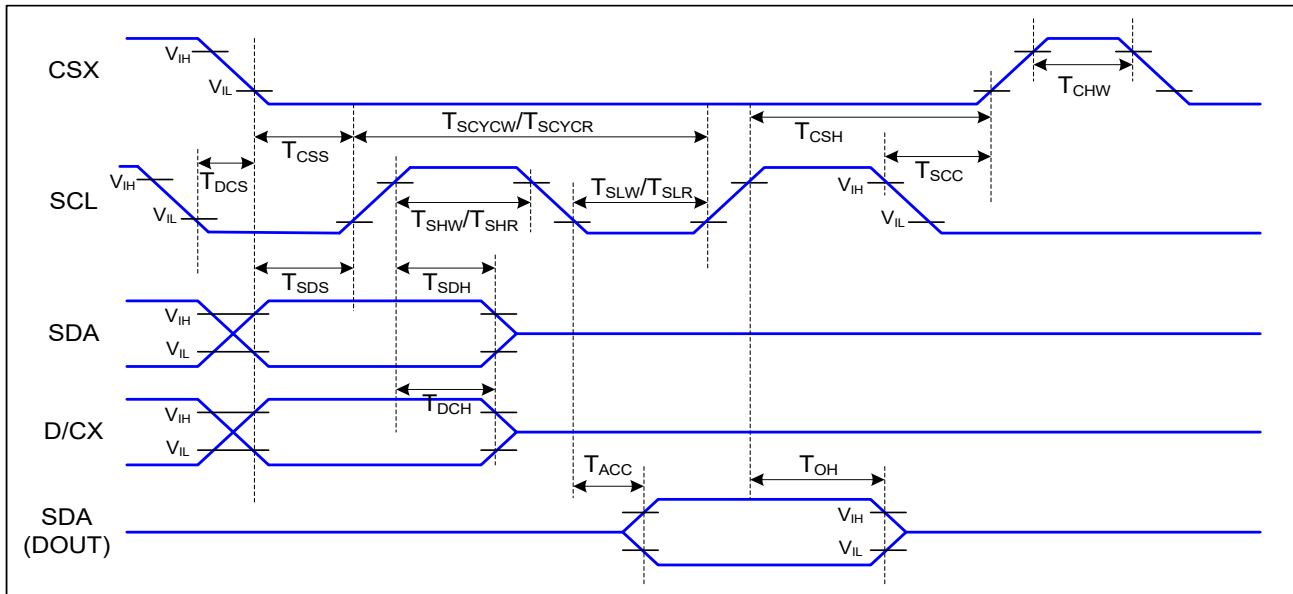


Figure 7 4-line Serial Interface Timing

T_a=25 °C, V_{DDI}=1.65~3.7V, V_{DD}=2.5~3.7V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip Select Setup Time (Write)	45		ns	
	TCSH	Chip Select Hold Time (Write)	45		ns	
	TCSS	Chip Select Setup Time (Read)	60		ns	
	TSCC	Chip Select Hold Time (Read)	65		ns	
	TCHW	Chip Select "H" Pulse Width	40		ns	
SCL	TSCYCW	Serial Clock Cycle (Write)	20		ns	-Write Command & Data Ram
	TSHW	SCL "H" Pulse Width (Write)	10		ns	
	TSLW	SCL "L" Pulse Width (Write)	10		ns	
	TSCYCR	Serial Clock Cycle (Read)	150		ns	-Read Command & Data Ram
	TSHR	SCL "H" Pulse Width (Read)	60		ns	
	TSLR	SCL "L" Pulse Width (Read)	60		ns	
D/CX	TDCS	D/CX Setup Time	10		ns	
	TDCH	D/CX Hold Time	10		ns	
SDA (DIN) (DOUT)	TSDS	Data Setup Time	10		ns	For Maximum CL=30pF For Minimum CL=8pF
	TSDH	Data Hold Time	10		ns	
	TACC	Access Time	10	50	ns	
	TOH	Output Disable Time	15	50	ns	

Table 7 4-line Serial Interface Characteristics

Note : The rising time and falling time (T_r, T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

9 Function Description

9.1 Interface Type Selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

P68	IM2	IM1	IM0	Interface	Read Back Selection
-	0	-	-	3-line Serial Interface	Via the Read Instruction
0	1	0	0	8080 MCU 8-bit Parallel	RDX Strobe (8-bit Read Data and 8-bit Read Parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX Strobe (16-bit Read Data and 8-bit Read Parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX Strobe (9-bit Read Data and 8-bit Read Parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX Strobe (18-bit Read Data and 8-bit Read Parameter)
-	0	-	-	3-line Serial Interface	Via the Read Instruction
1	1	0	0	6800 MCU 8-bit Parallel	E Strobe (8-bit Read Data and 8-bit Read Parameter)
1	1	0	1	6800 MCU 16-bit Parallel	E Strobe (16-bit Read Data and 8-bit Read Parameter)
1	1	1	0	6800 MCU 9-bit Parallel	E Strobe (9-bit Read Data and 8-bit Read Parameter)
1	1	1	1	6800 MCU 18-bit Parallel	E Strobe (18-bit Read Data and 8-bit Read Parameter)

Table 8 Interface Type Selection

P68	IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
-	0	-	-	3-line Serial	Note1	Note1	SCL	D[17:1]: Unused, D0: SDA
0	1	0	0	8080 8-bit Parallel	RDX	WRX	D/CX	D[17:8]: Unused, D7-D0: 8-bit Data
0	1	0	1	8080 16-bit Parallel	RDX	WRX	D/CX	D[17:16]: Unused, D15-D0: 16-bit Data
0	1	1	0	8080 9-bit Parallel	RDX	WRX	D/CX	D[17:9]: Unused, D8-D0: 9-bit Data
0	1	1	1	8080 18-bit Parallel	RDX	WRX	D/CX	D17-D0: 18-bit Data
-	0	-	-	4-line Serial	Note1	D/CX	SCL	D[17:1]: Unused, D0: SDA
1	1	0	0	6800 8-bit Parallel	E	WRX	RS	D[17:8]: Unused, D7-D0: 8-bit Data
1	1	0	1	6800 16-bit Parallel	E	WRX	RS	D[17:16]: Unused, D15-D0: 16-bit Data
1	1	1	0	6800 9-bit Parallel	E	WRX	RS	D[17:9]: Unused, D8-D0: 9-bit Data
1	1	1	1	6800 18-bit Parallel	E	WRX	RS	D17-D0: 18-bit Data

Table 9 Pin Connection According to Various MCU Interface

Note: Unused pins can be open, or connected to DGND or VDDI.

9.2 8080-series MCU Parallel Interface (P68 = '0')

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table..

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read Back Selection
1	0	0	8-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 8-bit Display Data or 8-bit Parameter (D7 to D0)
				1	↑	1	Read 8-bit Display Data (D7 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)
1	0	1	16-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 16-bit Display Data or 8-bit Parameter (D15 to D0)
				1	↑	1	Read 16-bit Display Data (D15 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)
1	1	0	9-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 9-bit Display Data or 8-bit Parameter (D8 to D0)
				1	↑	1	Read 9-bit Display Data (D8 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)
1	1	1	18-bit Parallel	0	1	↑	Write 8-bit Command (D7 to D0)
				1	1	↑	Write 18-bit Display Data or 8-bit Parameter (D17 to D0)
				1	↑	1	Read 18-bit Display Data (D17 to D0)
				1	↑	1	Read 8-bit Parameter or Status (D7 to D0)

Table 10 The Function of 8080-series Parallel Interface

Note: applied for command code: Dah, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

9.2.1 Write Cycle Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (= '0') and vice versa it is data (= '1').

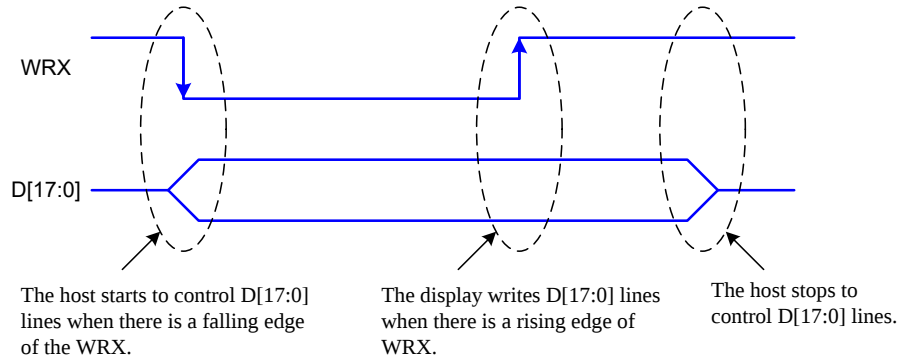


Figure 8 8080-series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

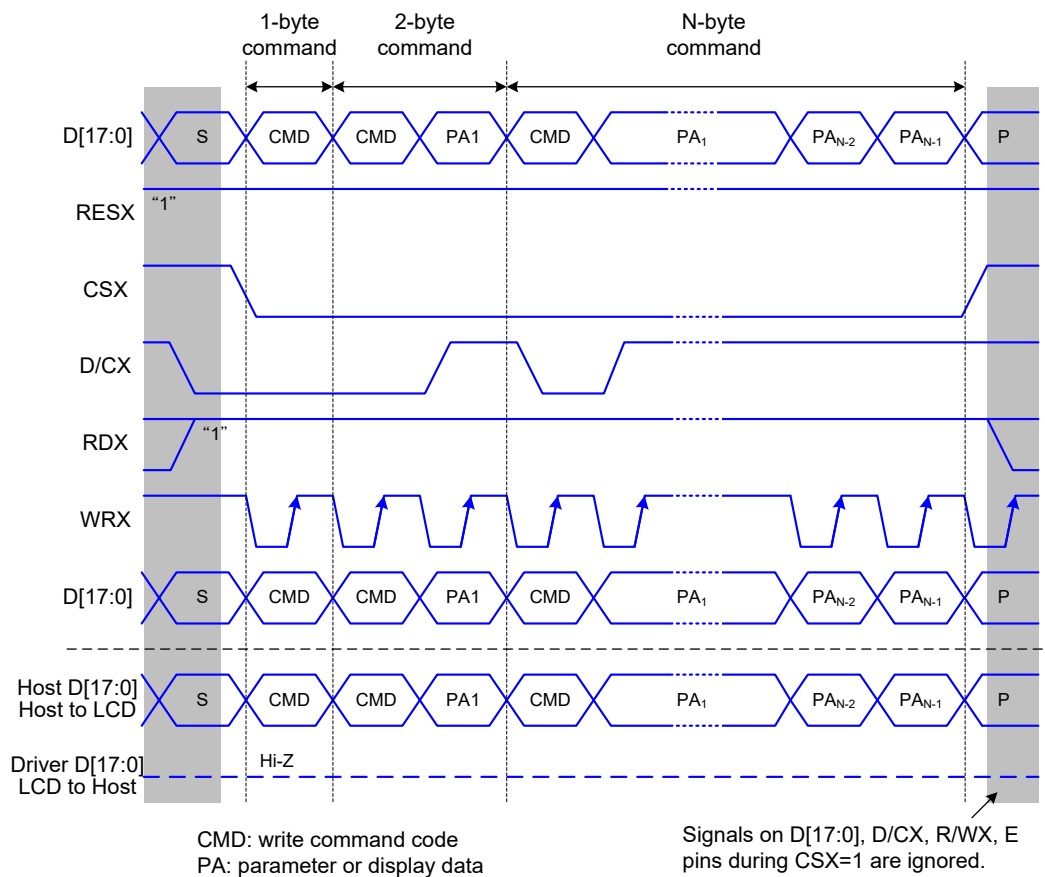


Figure 9 8080-series Parallel Bus Protocol, Write to Register or Display RAM

9.2.2 Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

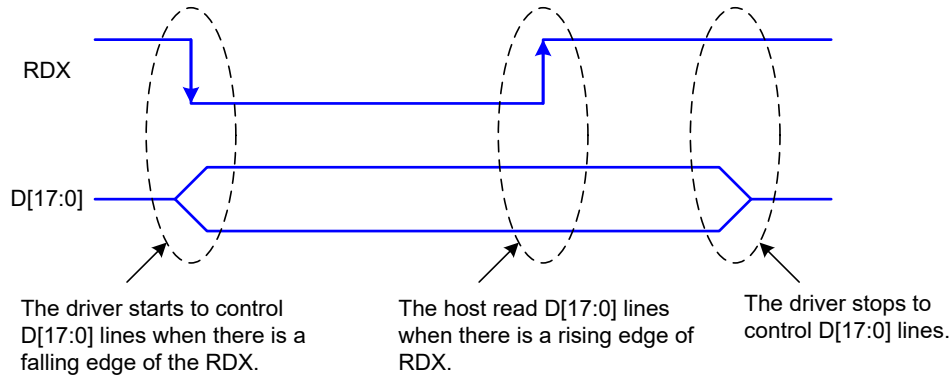


Figure 10 8080-series RDX Protocol

Note: RDX is an unsynchronized signal (It can be stopped).

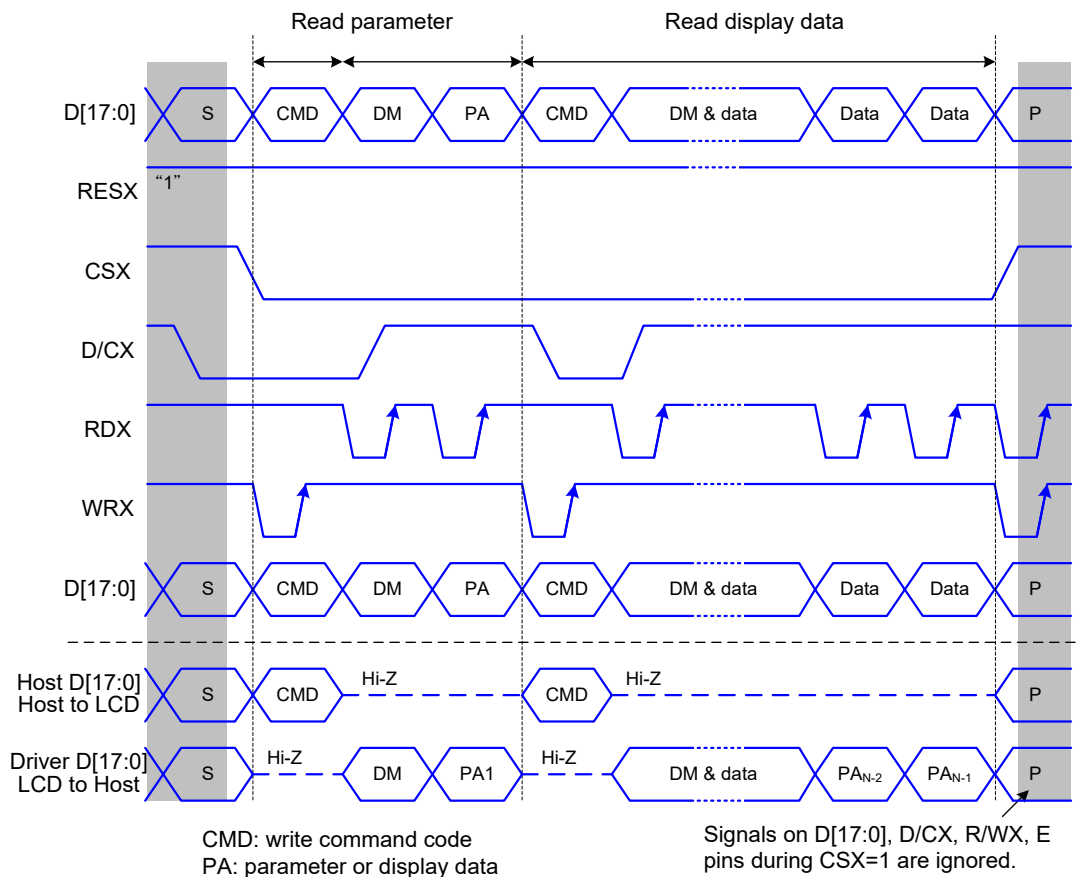


Figure 11 8080-series Parallel Bus Protocol, Read Data from Register or Display RAM

9.3 6800-series MCU Parallel Interface (P68 = '1')

The MCU uses one of following interface: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface, or 21-lines with 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data bus.

The LCD driver reads the data at the falling edge of E signal when R/WX= '1' and Writes the data at the falling of the E signal when R/WX='0'. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C= '0', D[17:0] bits are commands.

The 6800-series bi-directional interface can be used for communication between the micro controller and LCD driver. The selection of this interface is done when P68 pin is high state (VDDI). Interface bus width can be selected with IM2, IM1 and IM0. The interface functions of 6800-series parallel interface are given in Table11.

P68	IM2	IM1	IM0	Interface	D/CX	R/WX	E	Function
1	1	0	0	8-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 8-bit Display Data or 8-bit Parameter (D7 to D0)
					1	1	↓	Read 8-bit Display Data (D7 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)
1	1	0	1	16-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 16-bit Display Data or 8-bit Parameter (D15 to D0)
					1	1	↓	Read 16-bit Display Data (D15 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)
1	1	1	0	9-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 9-bit Display Data or 8-bit Parameter (D8 to D0)
					1	1	↓	Read 9-bit Display Data (D8 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)
1	1	1	1	18-bit Parallel	0	0	↓	Write 8-bit Command (D7 to D0)
					1	0	↓	Write 18-bit Display Data or 8-bit Parameter (D17 to D0)
					1	1	↓	Read 18-bit Display Data (D17 to D0)
					1	1	↓	Read 8-bit Parameter or Status (D7 to D0)

Table 11 The Function of 6800-series Parallel Interface

Note: applied for command code: Dah, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh.

9.3.1 Write Cycle Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (E low-high-low sequence) consists of 3 control signals (D/CX, E, R/WX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (= '0') and vice versa it is data (= '1').

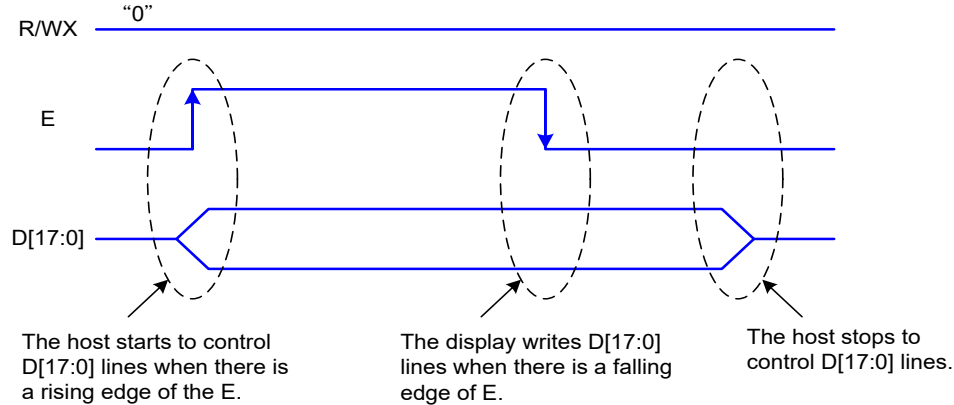


Figure 12 6800-series Write Protocol

Note: E is an unsynchronized signal (It can be stopped)

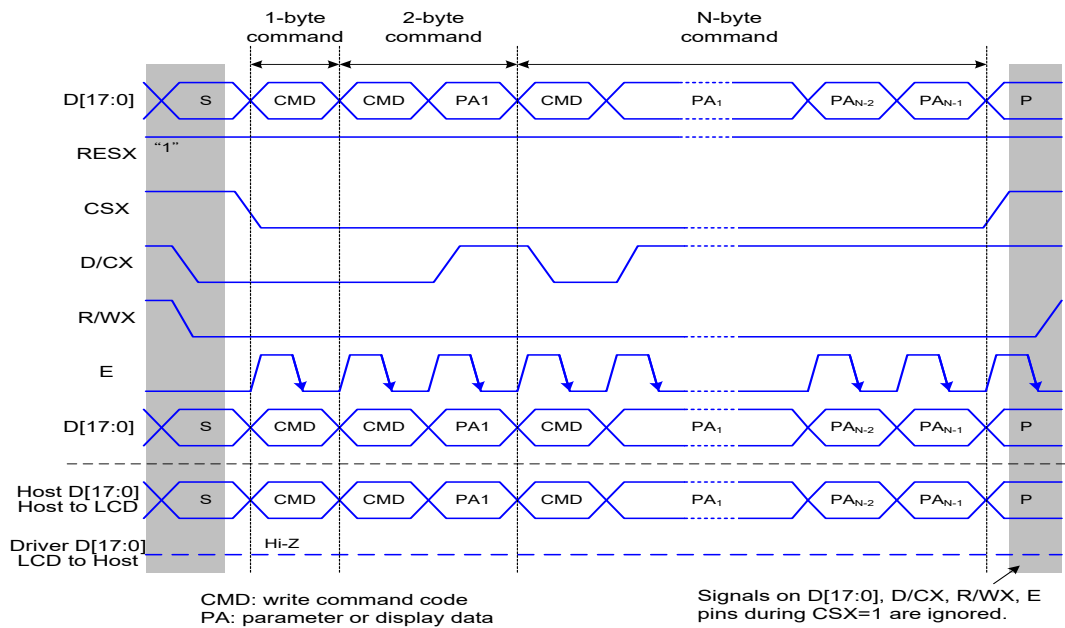


Figure 13 6800-series Parallel Bus Protocol, Write to Register or Display RAM

9.3.2 Read Cycle Sequence

The read cycle (E low-high-low sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a rising edge of E and the host reads data when there is a falling edge of E.

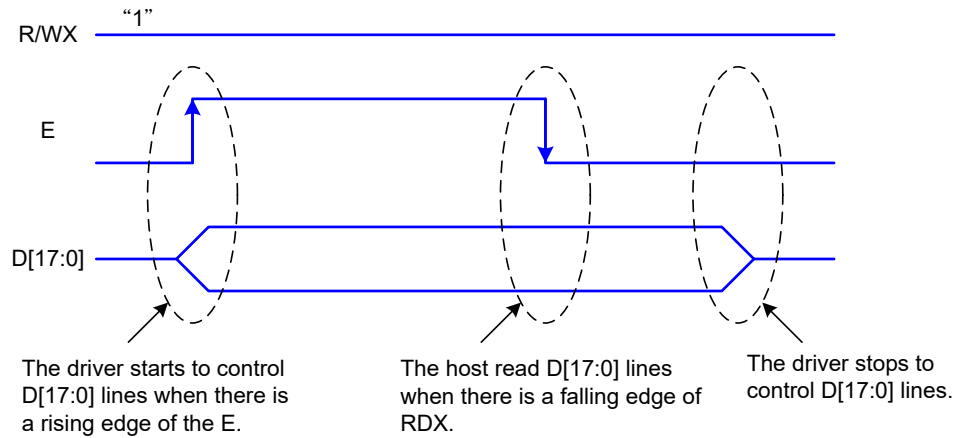


Figure 14 6800-series Read Protocol

Note: E is an unsynchronized signal (It can be stopped)

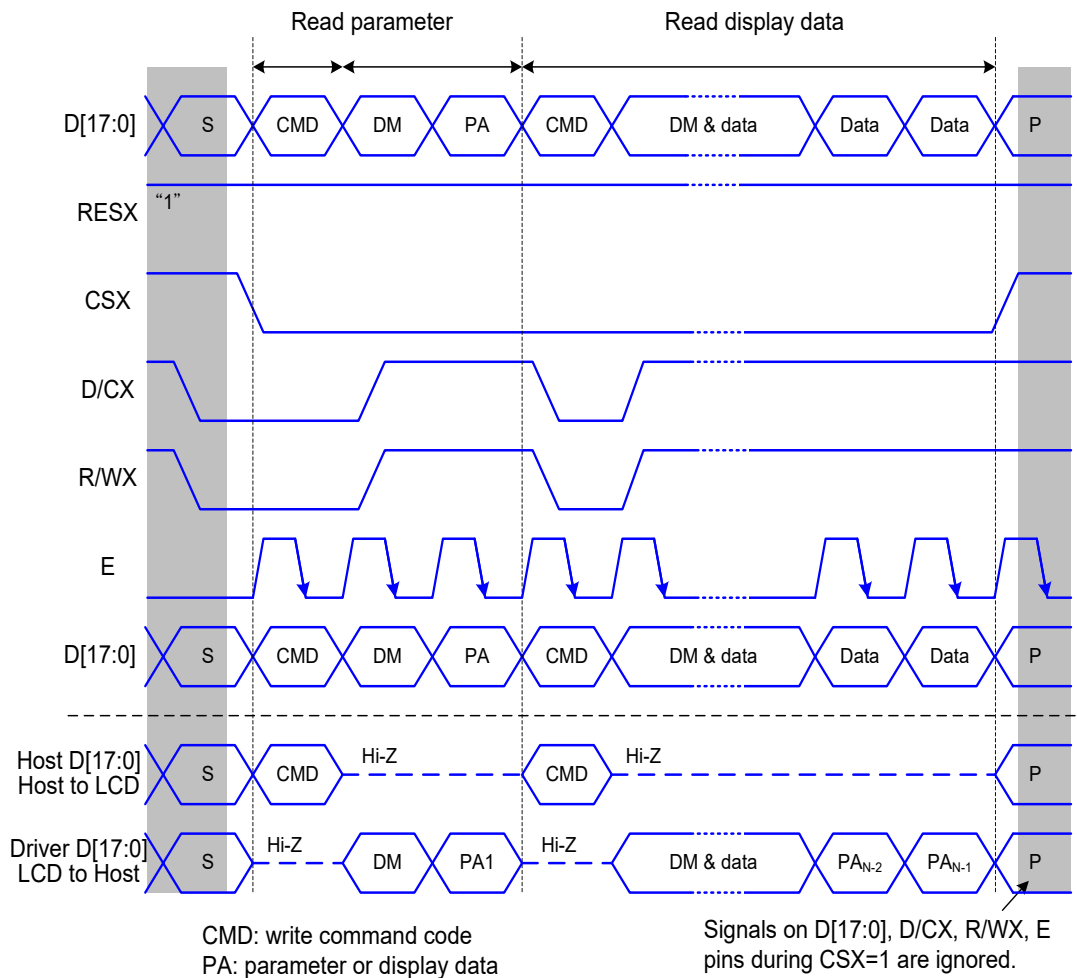


Figure 15 6800-series Parallel Bus Protocol, Read Data form Register or Display RAM

9.4 Serial Interface

The selection of this interface is done by IM2. See the Table 12.

IM2	4WSPI	Interface	Read Back Selection
0	0	3-line Serial Interface	Via the Read Instruction (8-bit, 24-bit and 32-bit Read Parameter)
0	1	4-line Serial Interface	Via the Read Instruction (8-bit, 24-bit and 32-bit Read Parameter)

Table 12 Selection of Serial Interface

The serial interface is either 3-lines/9-bits or 4-lines/8-bits bi-directional interface for communication between the micro controller and the LCD driver. The 3-lines serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-lines serial interface use: CSX (chip enable), D/CX (data/command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

9.4.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-lines serial data packet contains a control bit D/CX and a transmission byte. In 4-lines serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is "low", the transmission byte is interpreted as a command byte. If D/CX is "high", the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

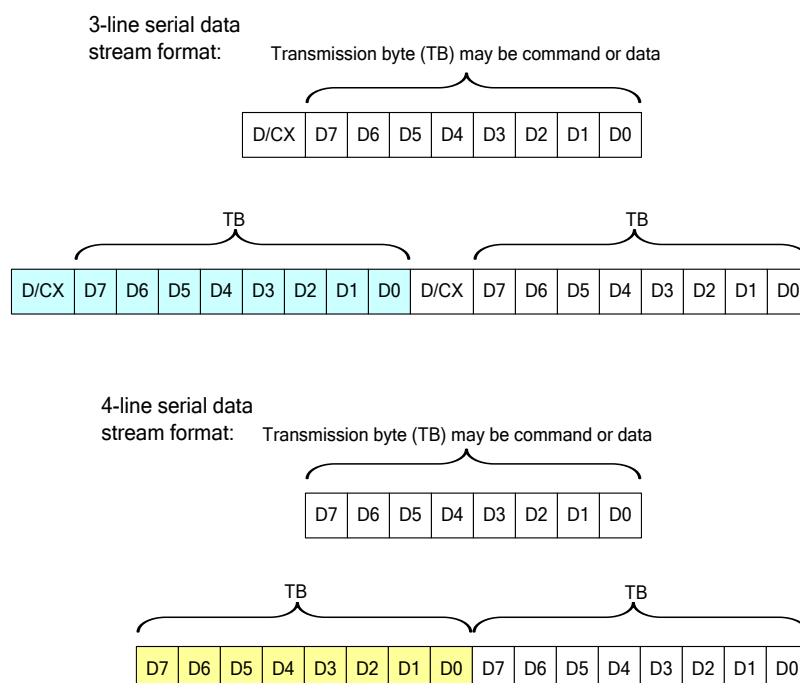


Figure 16 Serial Interface Data Stream Format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Figure 17). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX=’0’) or parameter/RAM data (D/CX=’1’). D/CX is sampled when first rising edge of SCL (3-lines serial interface) or 8th rising edge of SCL (4-lines serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-lines serial interface) or D7 (4-lines serial interface) of the next byte at the next rising edge of SCL..

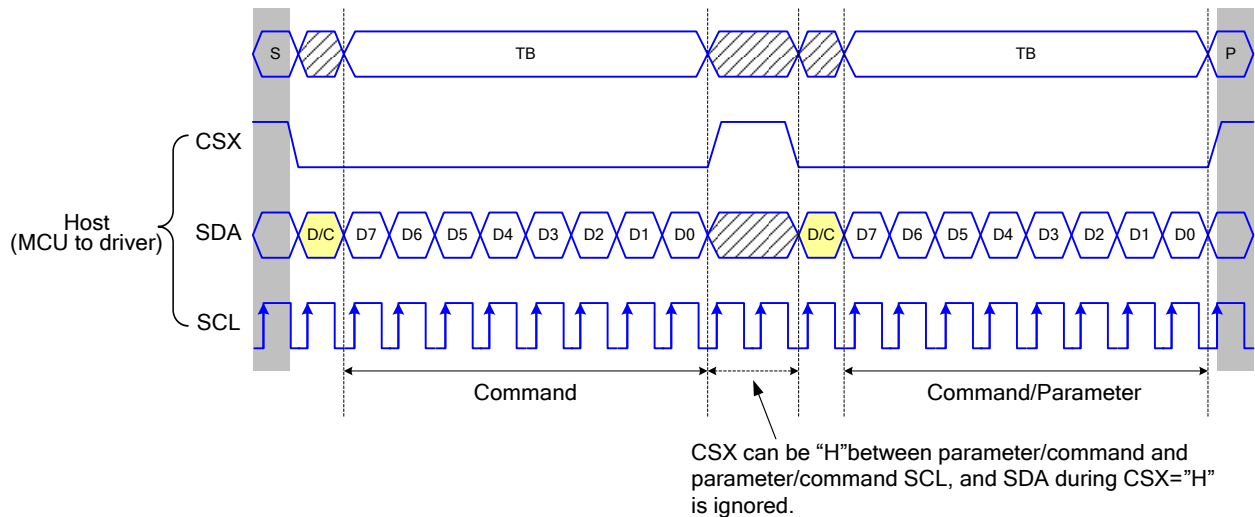


Figure 17 3-line Serial Interface Write Protocol (Write to Register with Control Bit in Transmission)

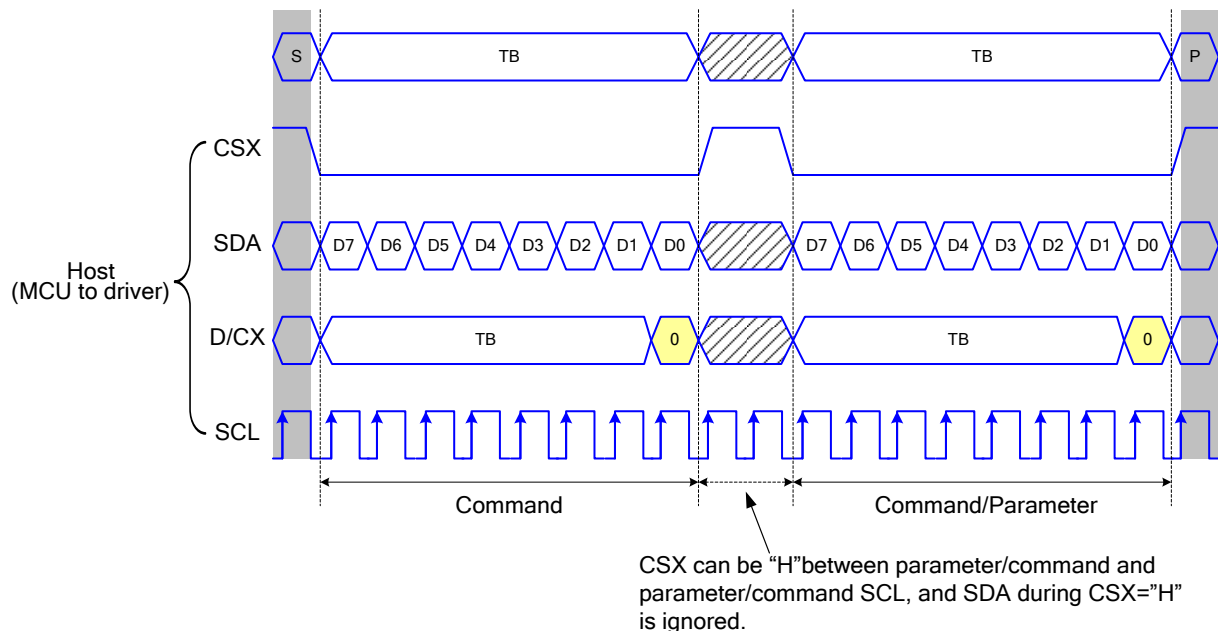


Figure 18 4-line Serial Interface Write Protocol (Write to Register with Control Bit in Transmission)

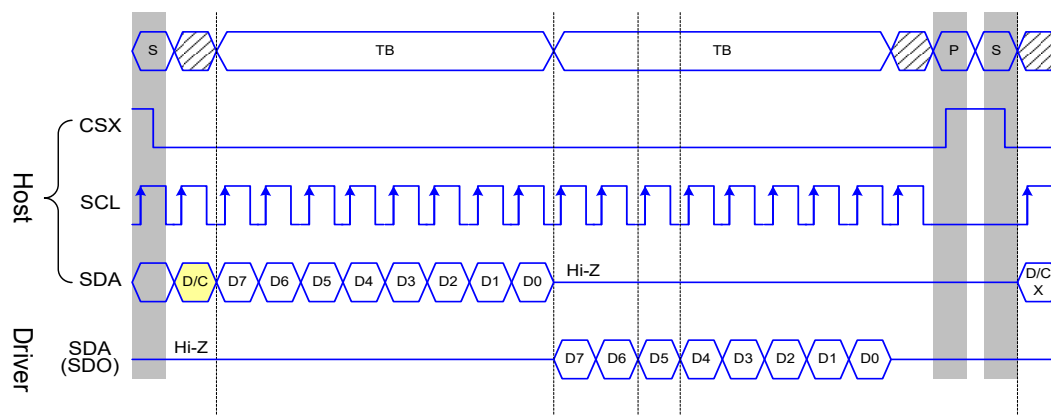
9.4.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

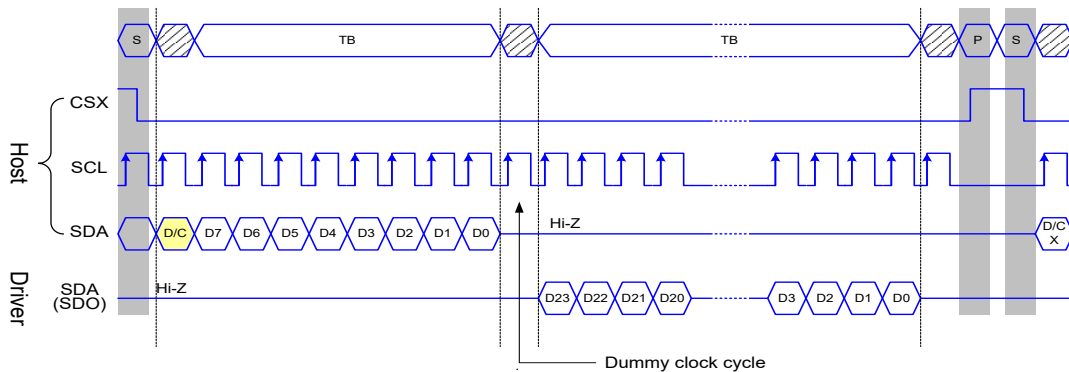
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

9.4.3 3-line Serial Protocol

3-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh Command: 8-bit Read):



3-line Serial Protocol (for RDDID Command: 24-bit Read)



3-line Serial Protocol (for RDDST Command: 32-bit Read)

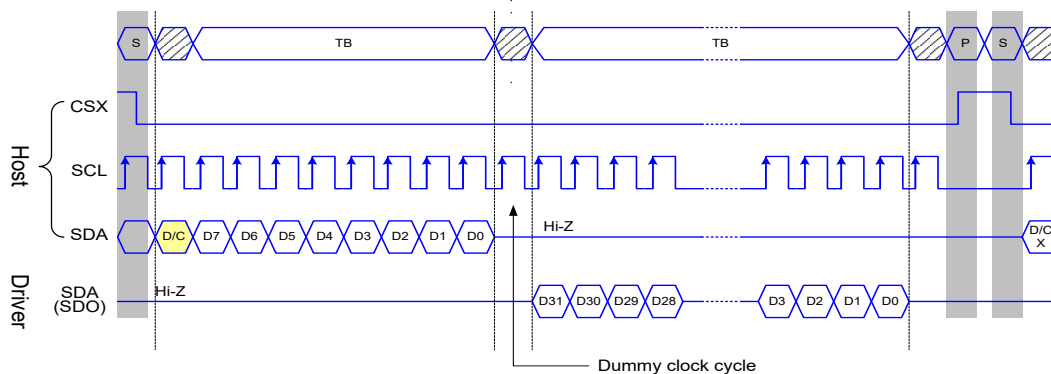
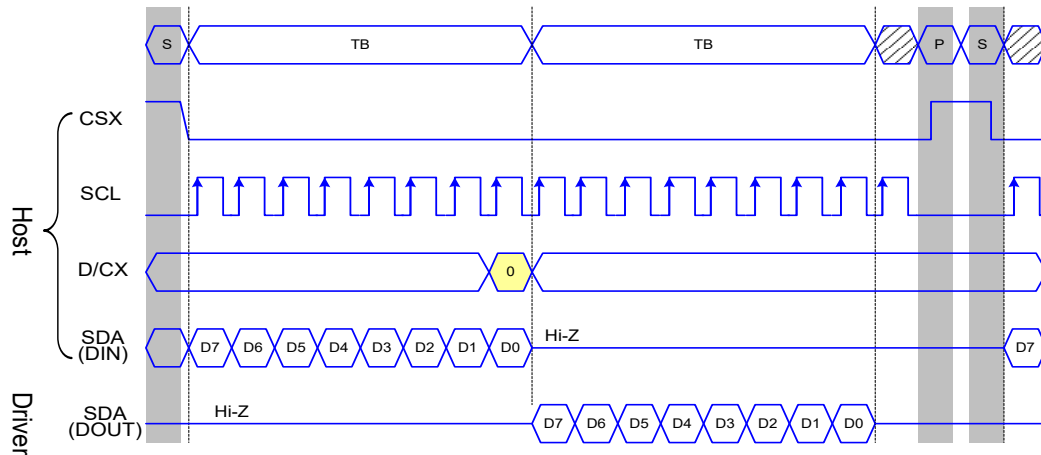


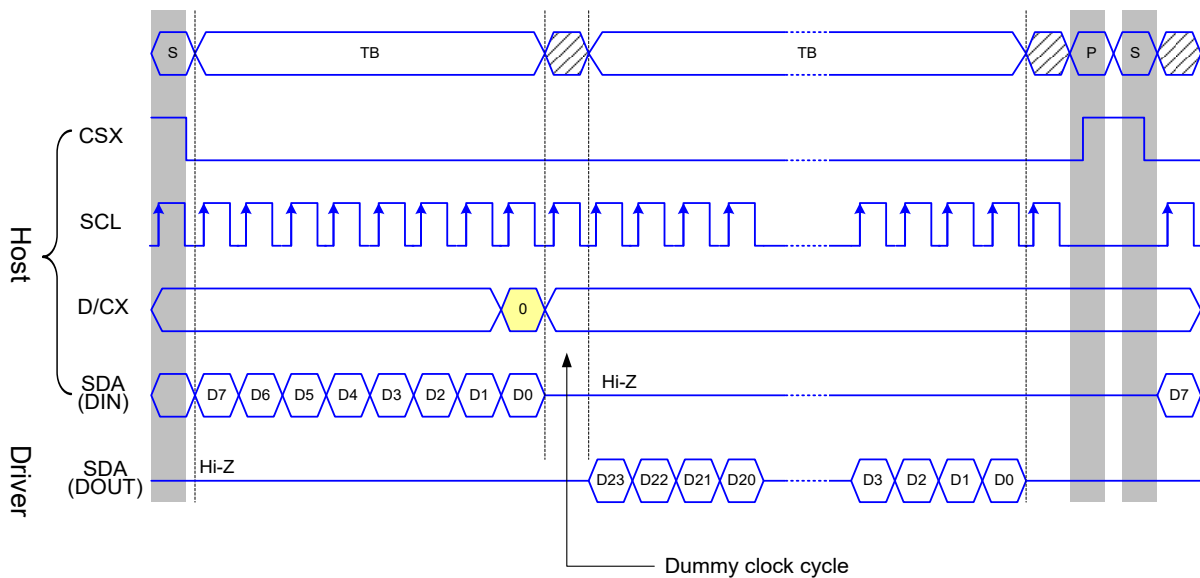
Figure 19 3-line Serial Interface Read Protocol

9.4.4 4-line Serial Protocol

4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh Command: 8-bit Read):



4-line Serial Protocol (for RDDID Command: 24-bit Read)



4-line Serial Protocol (for RDDST Command: 32-bit Read)

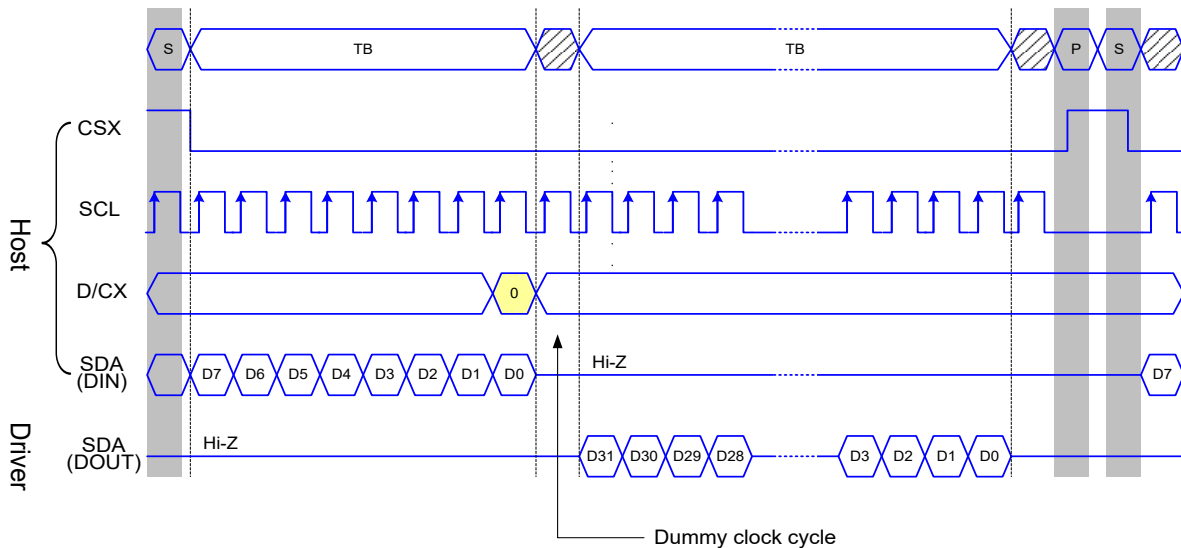


Figure 20 4-line Serial Interface Read Protocol

9.5 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example

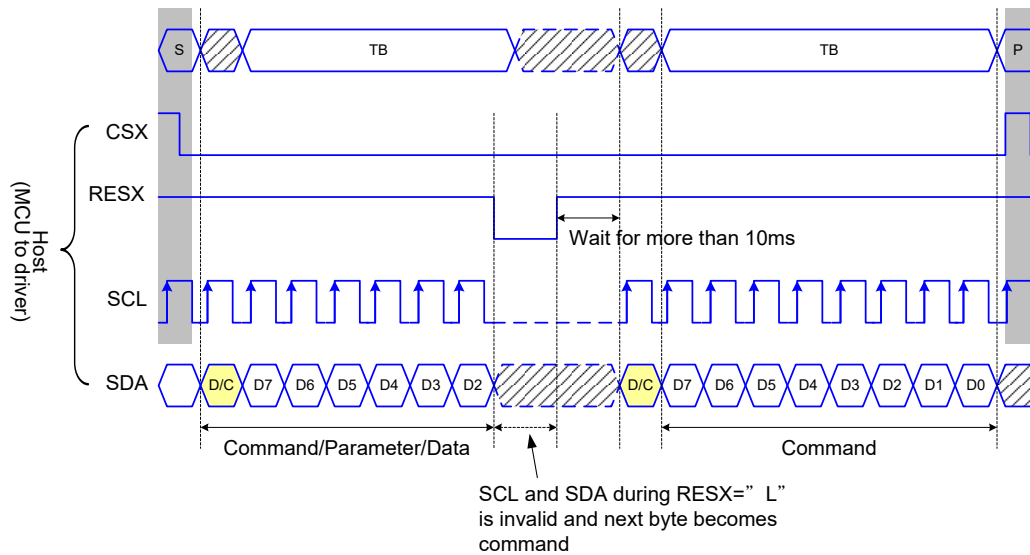


Figure 21 Serial Bus Protocol, Write Mode – Interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

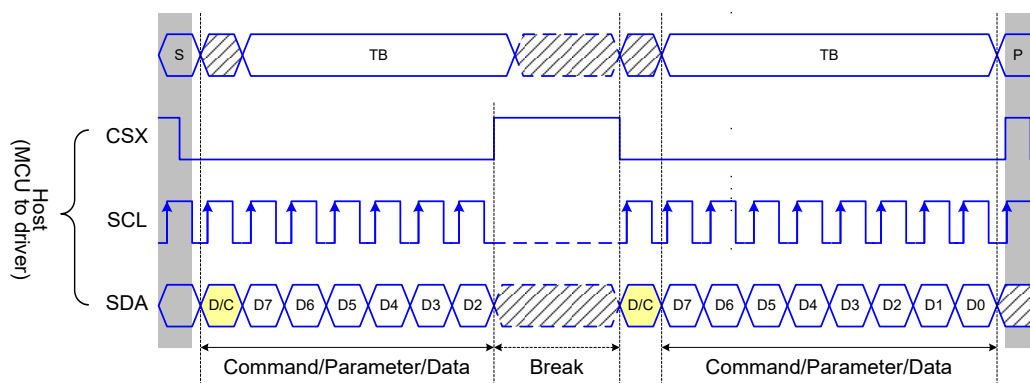


Figure 22 Serial Bus Protocol, Write Mode – Interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

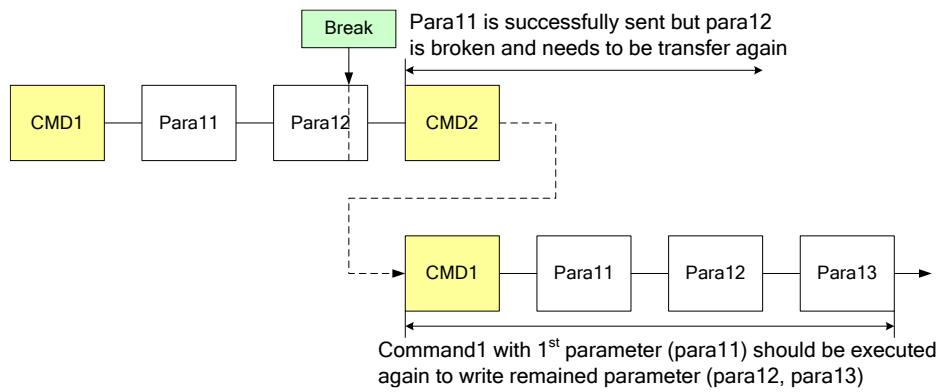


Figure 23 Write Interrupts Recovery (Serial Interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

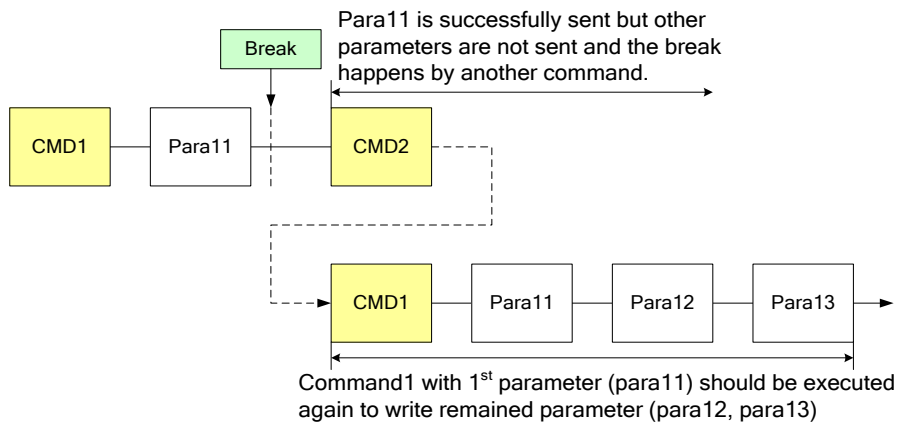


Figure 24 Write Interrupts Recovery (Both Serial and Parallel Interface)

9.6 Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

9.6.1 Serial Interface Pause

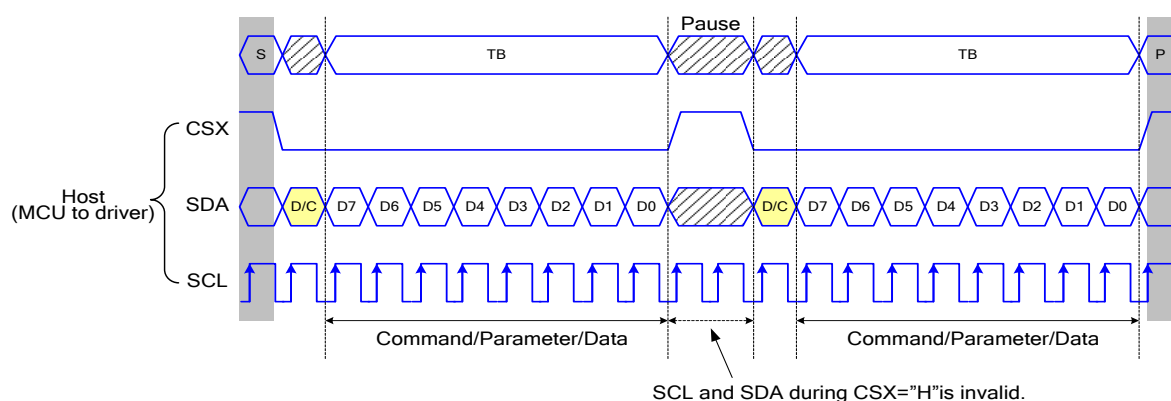


Figure 25 Serial Interface Pause Protocol (Pause by CSX)

9.6.2 Parallel Interface Pause

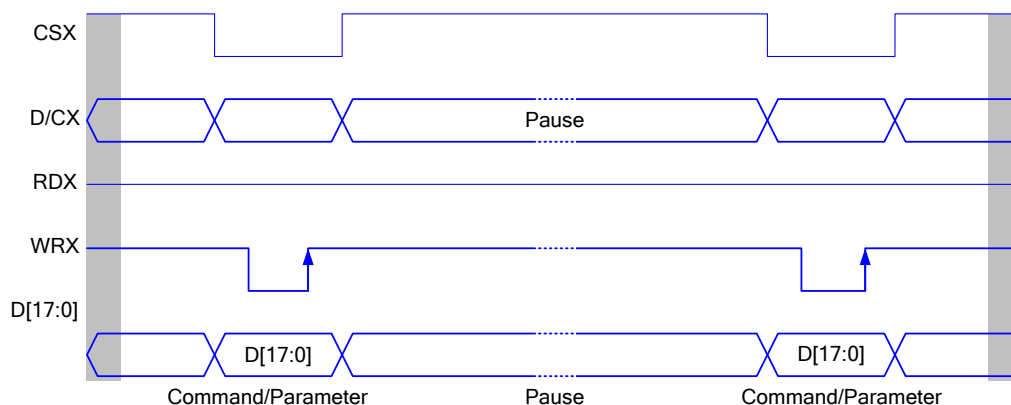


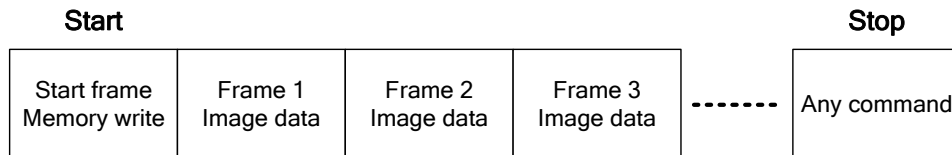
Figure 26 Parallel Bus Pause Protocol (Paused by CSX)

9.7 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

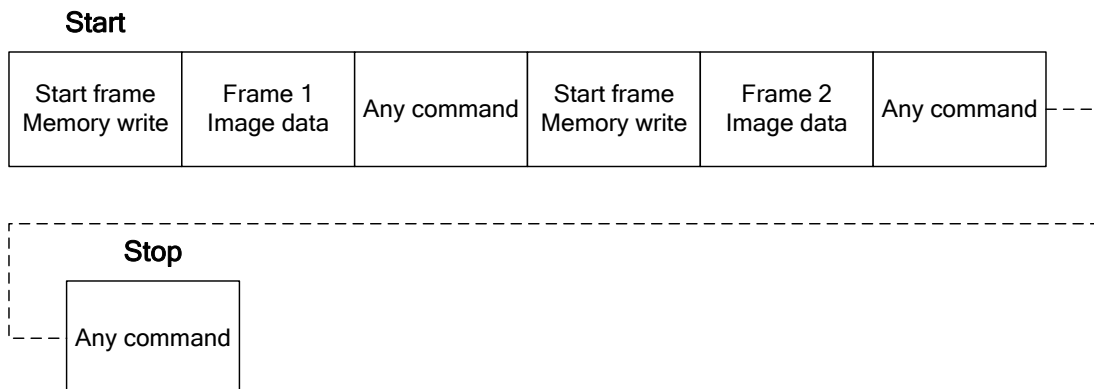
9.7.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



9.7.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

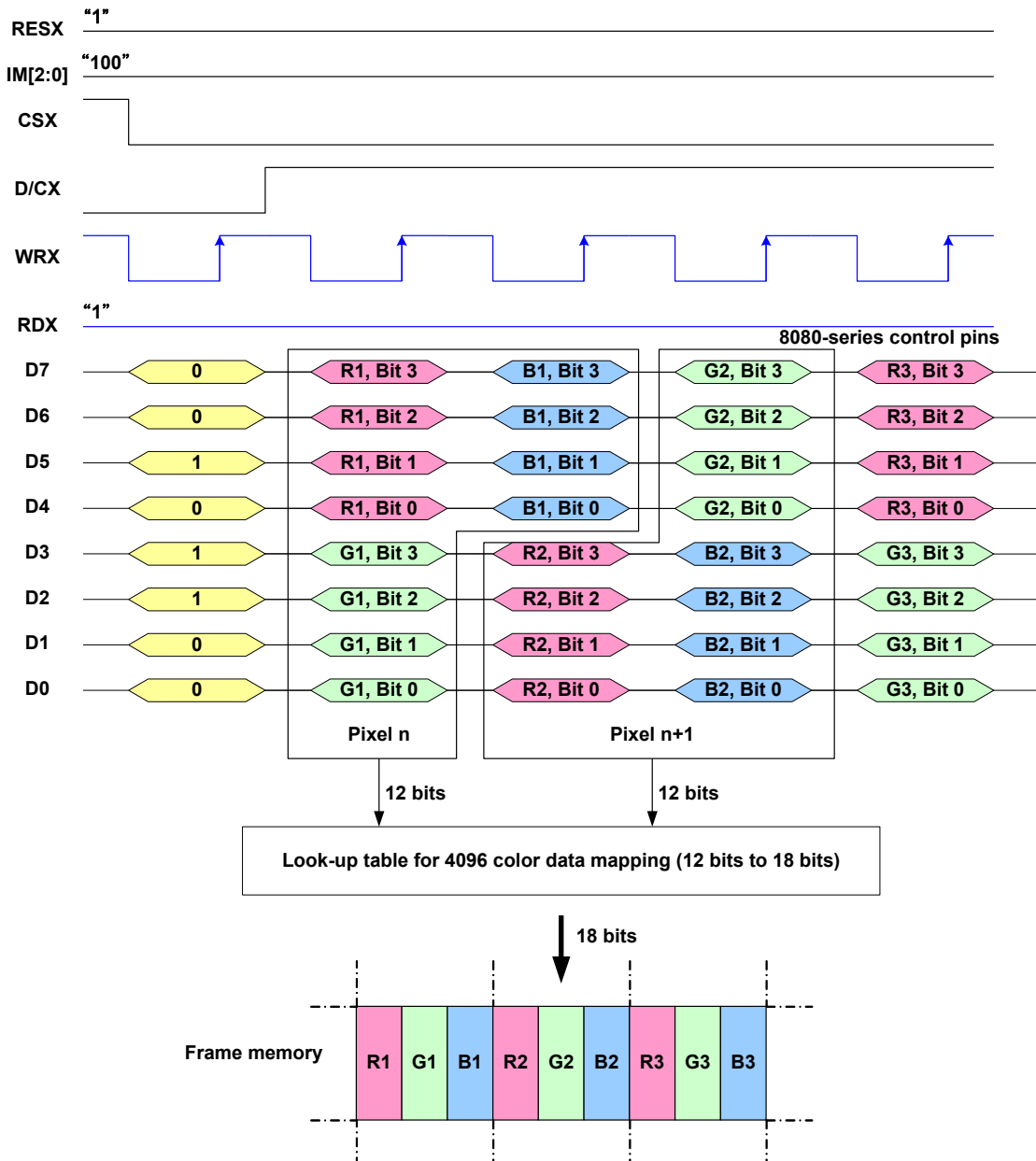
9.8 Data Color Coding

9.8.1 8-bit Parallel Interface (IM2, IM1, IM0= "100")

Different display data formats are available for three Colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit Input.
- 65k Colors, RGB 5,6,5-bit Input.
- 262k Colors, RGB 6,6,6-bit Input.

9.8.2 8-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= "03h"



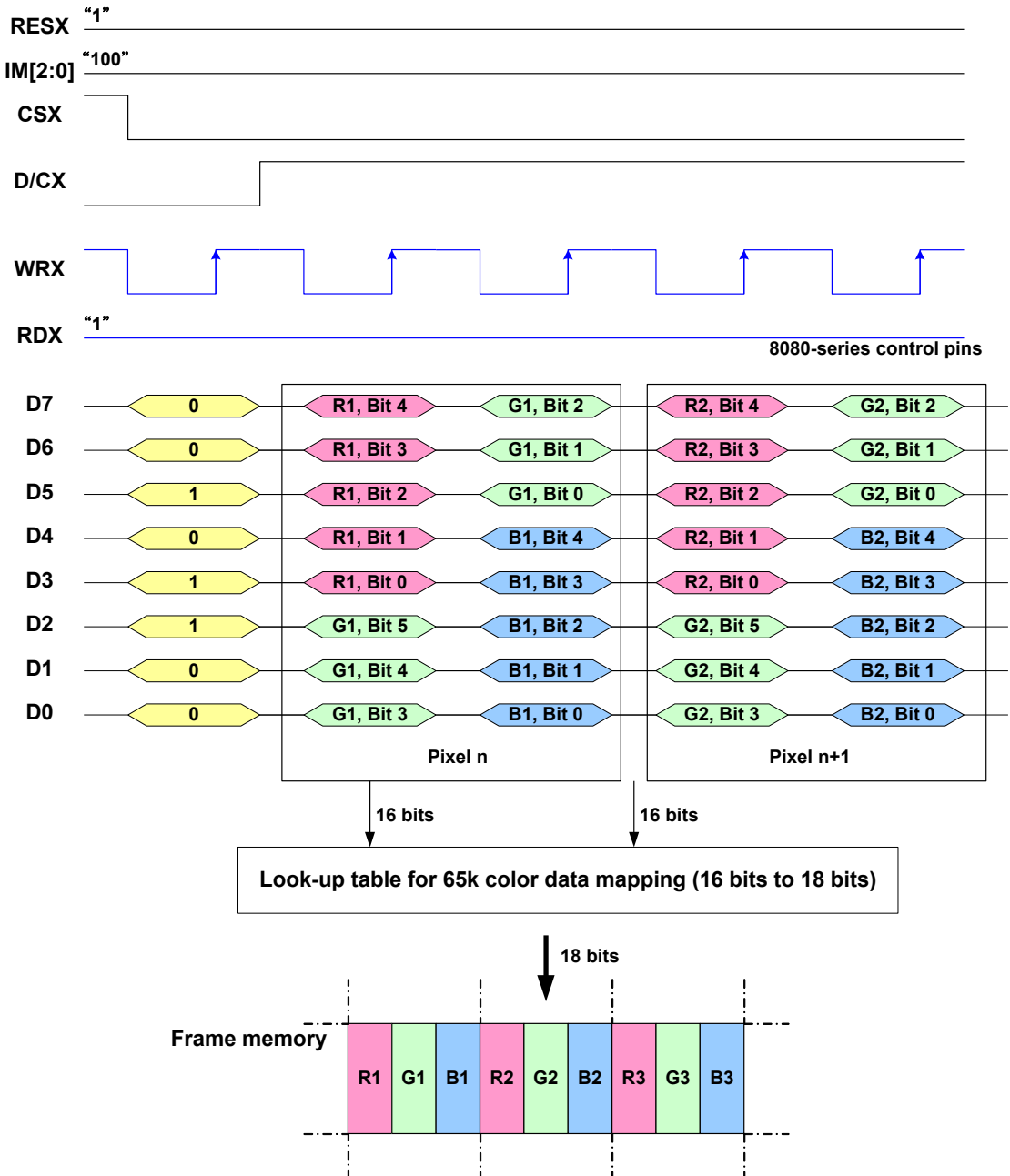
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

9.8.3 8-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 2-byte



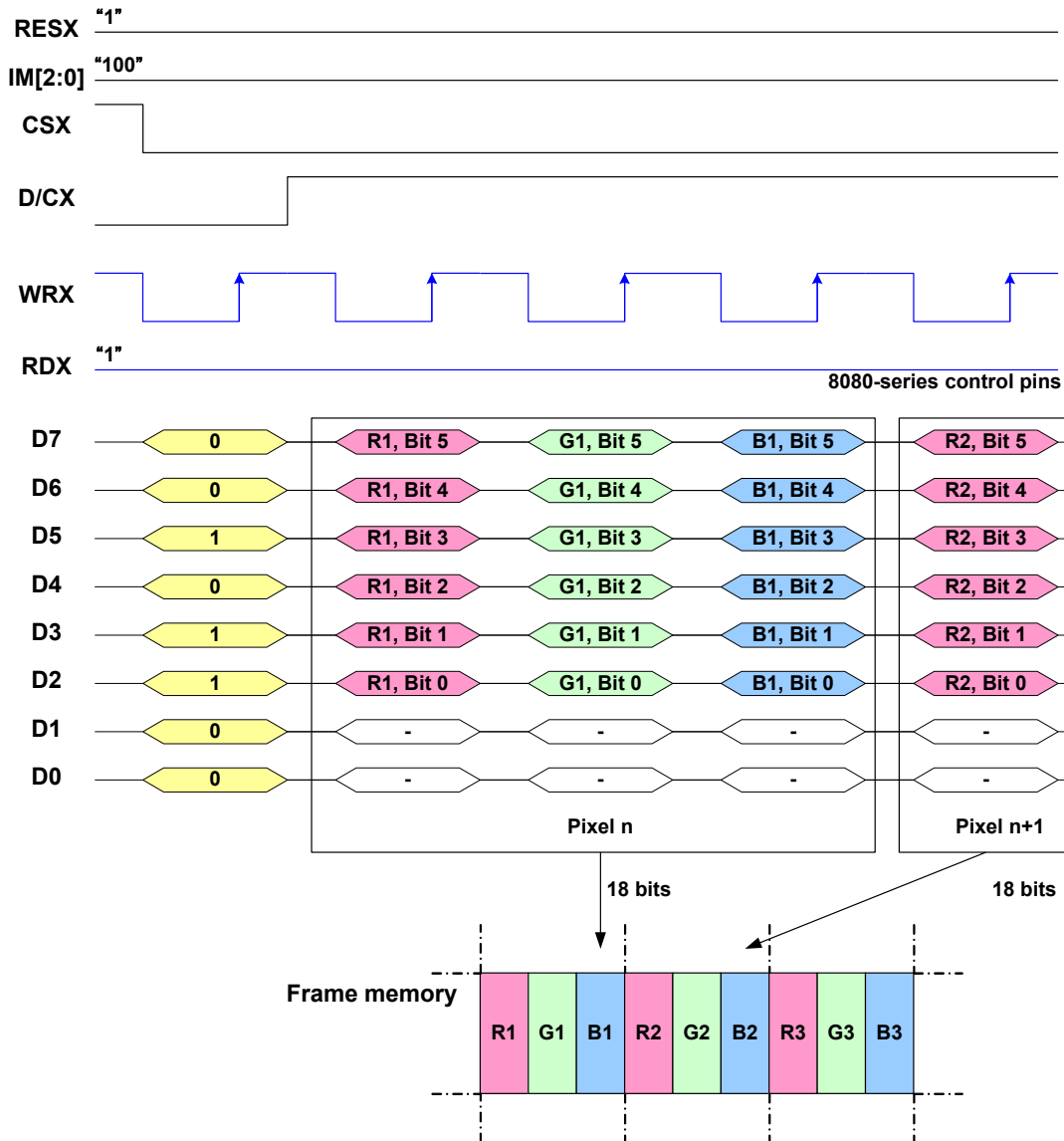
Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

9.8.4 8-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= "06h"

There is 1 pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

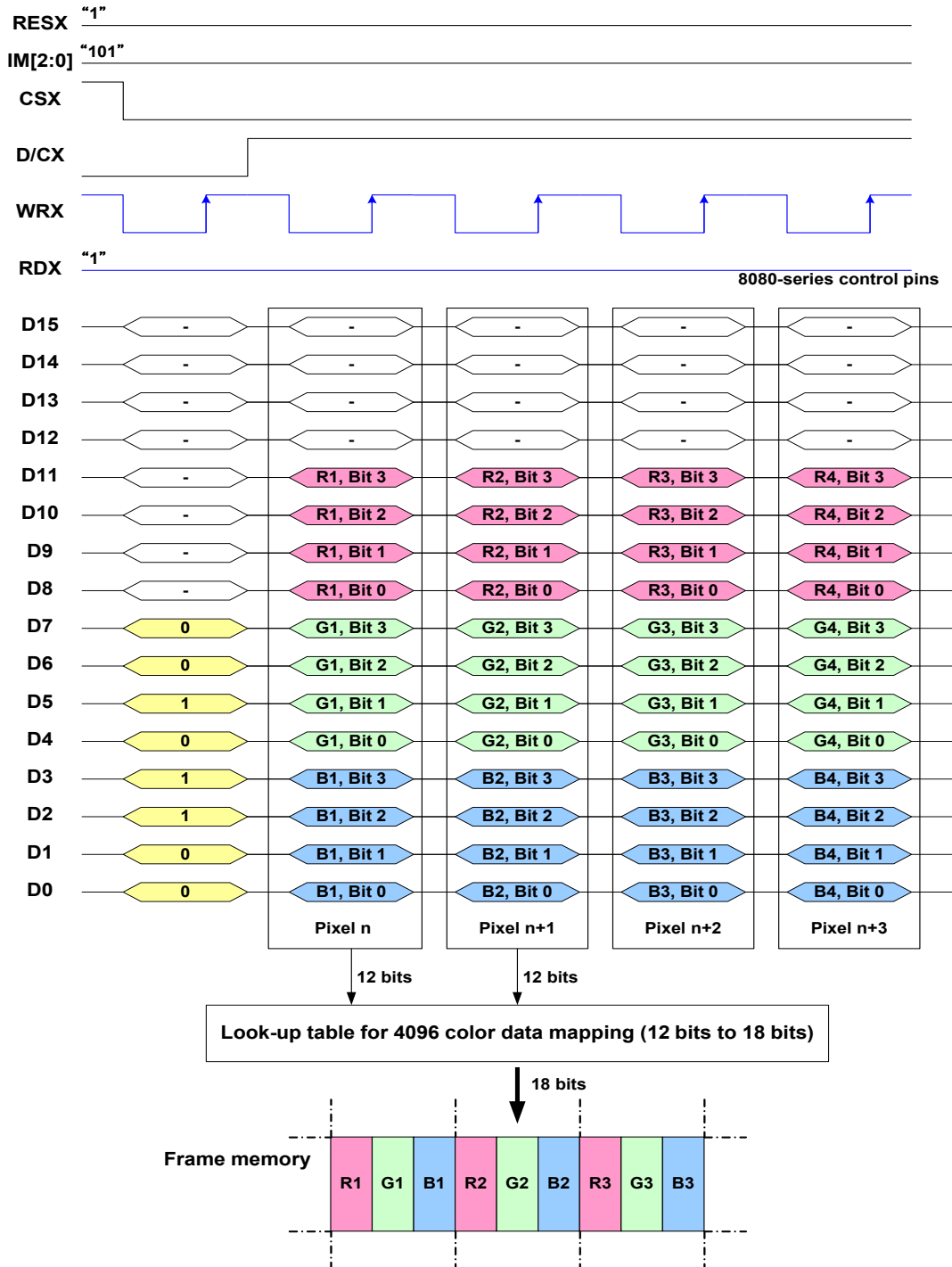
9.8.5 16-Bit Parallel Interface (IM2,IM1, IM0= "101")

Different display data formats are available for three colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit Input
- 65k Colors, RGB 5,6,5-bit Input
- 262k Colors, RGB 6,6,6-bit Input

9.8.6 16-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH= "03h"

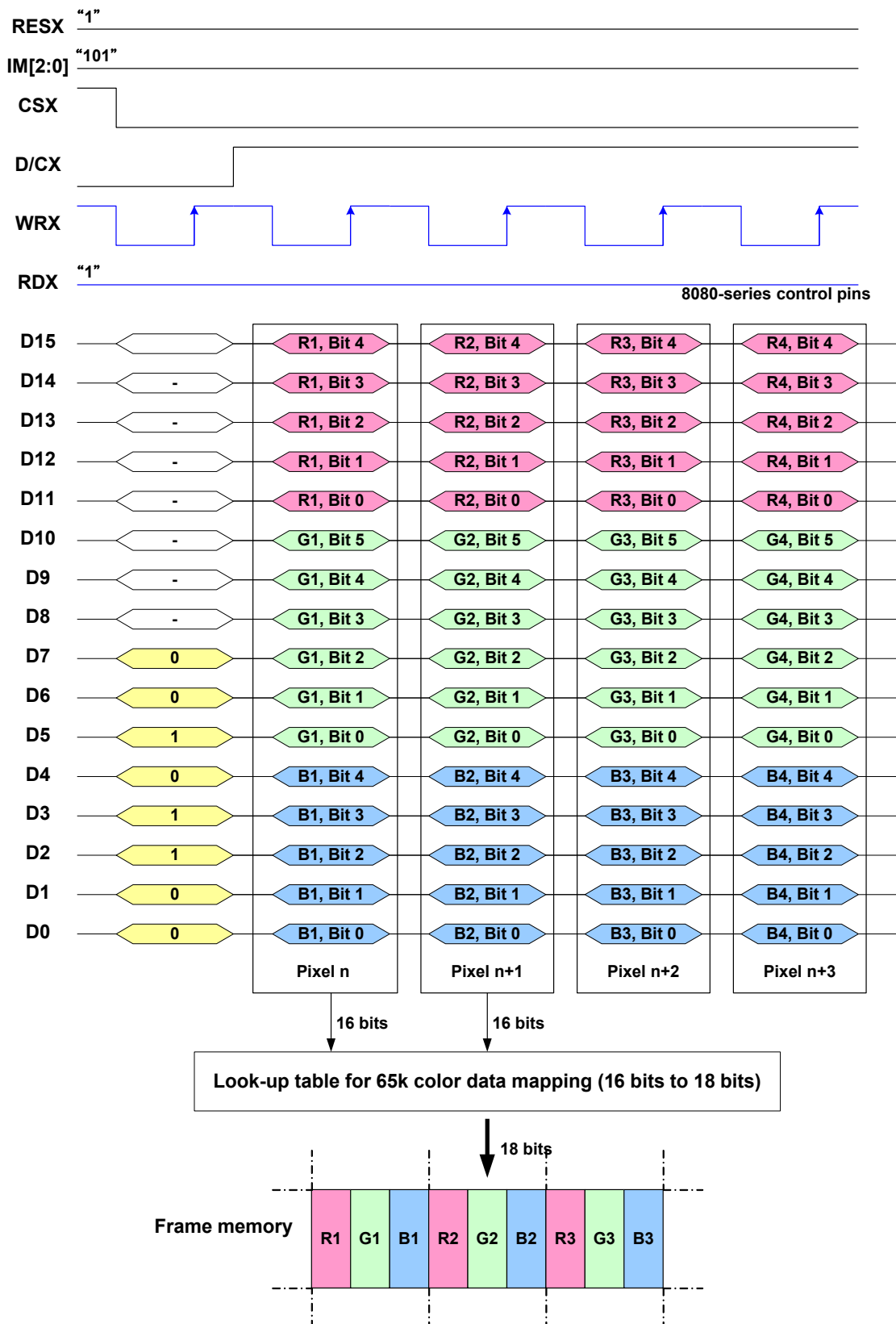
There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
 Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.7 16-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 1 byte



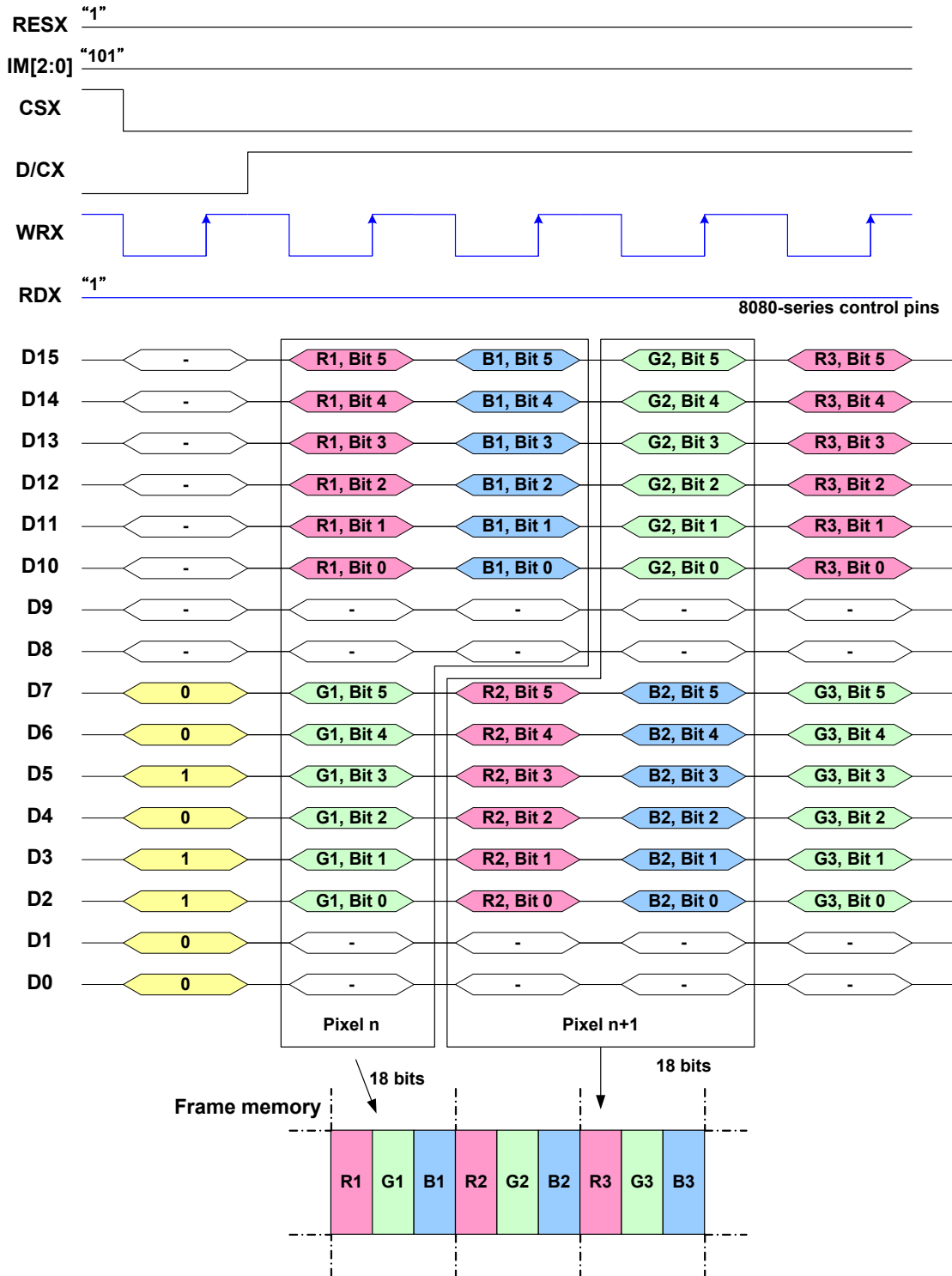
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

9.8.8 16-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH= "06h"

There are 2 pixels (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

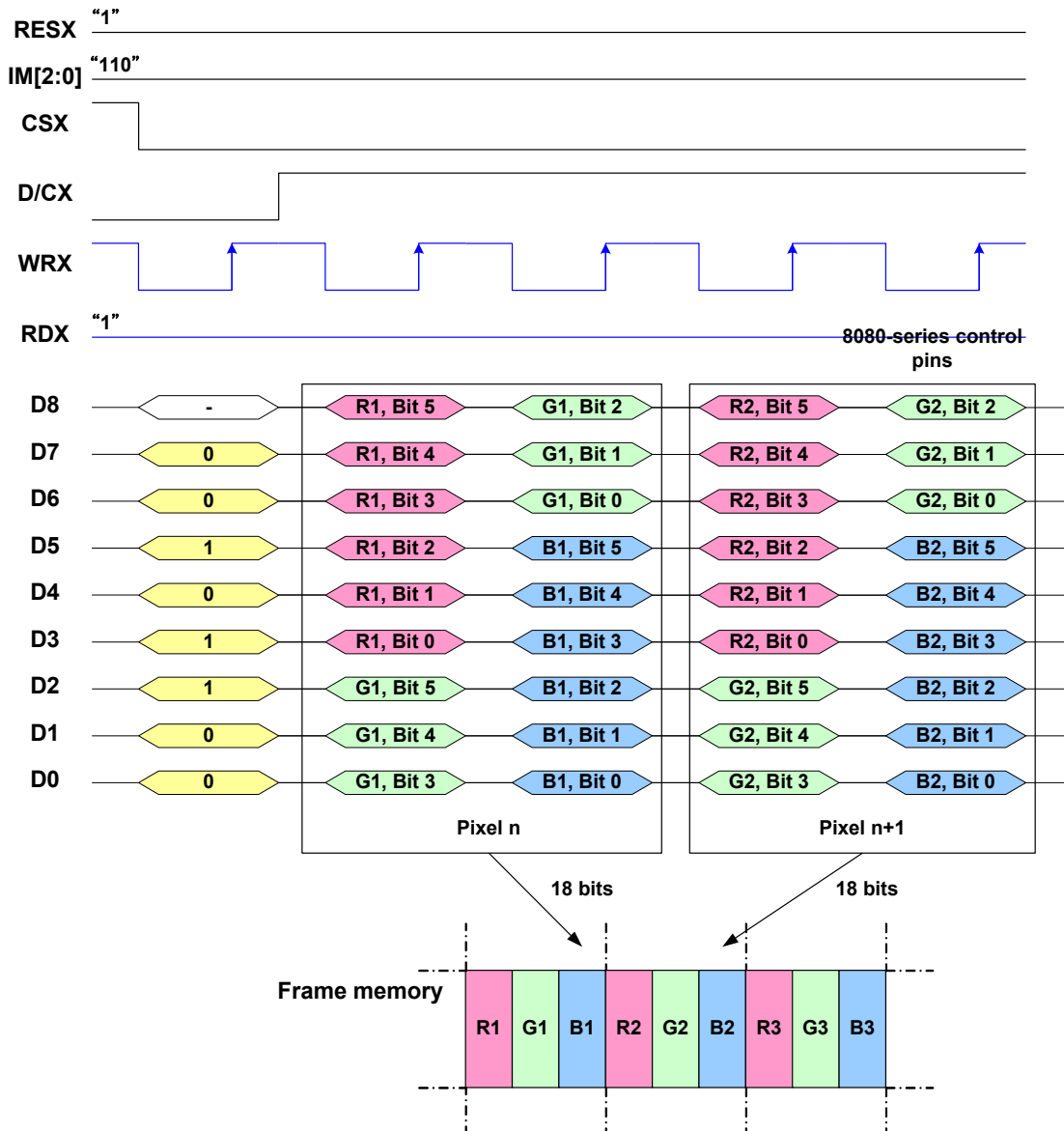
9.8.9 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.

-262k colors, RGB 6,6,6-bit input

9.8.10 Write 9-bit Data for RGB 6-6-6-bit Input (262k-color)

There is 1 pixel (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care – Can be set to '0' or '1'

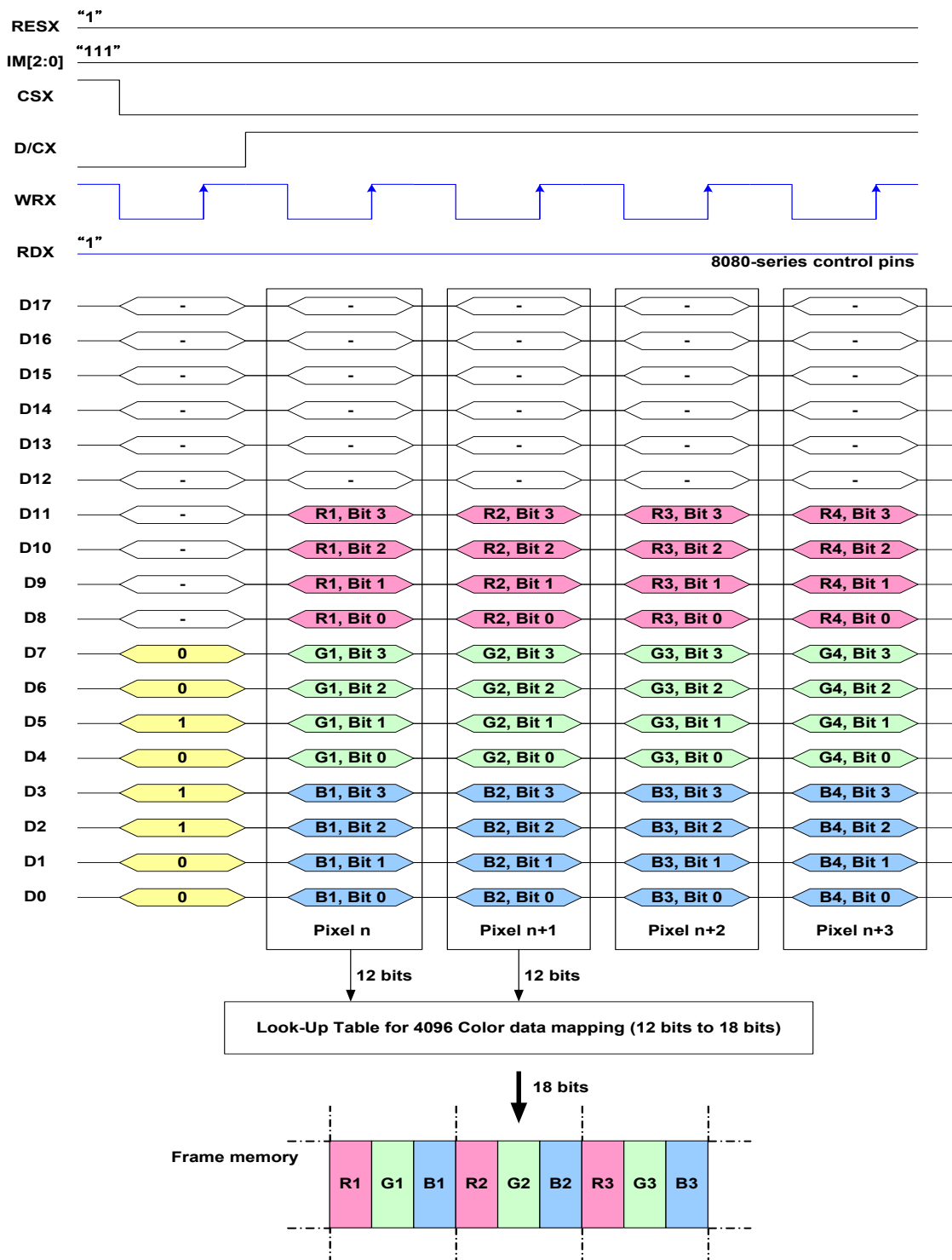
9.8.11 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.

- 4k Colors, RGB 4,4,4-bit Input
- 65k Colors, RGB 5,6,5-bit Input
- 262k Colors, RGB 6,6,6-bit Input.

9.8.12 18-bit Data Bus for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h"

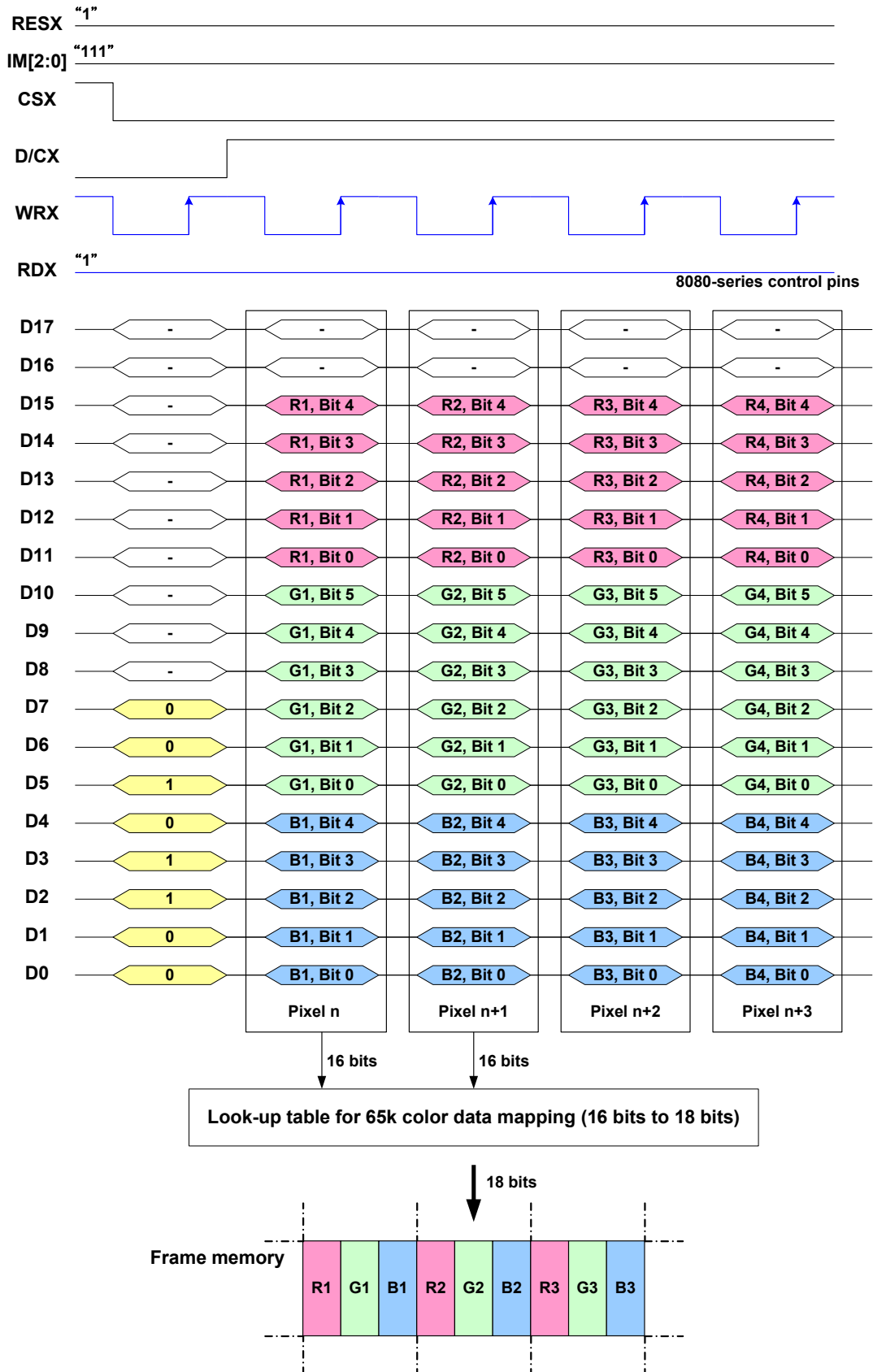
There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.
 Note 2: 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

9.8.13 18-bit Data Bus for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h"

There is 1 pixel (3 sub-pixels) per 1 byte

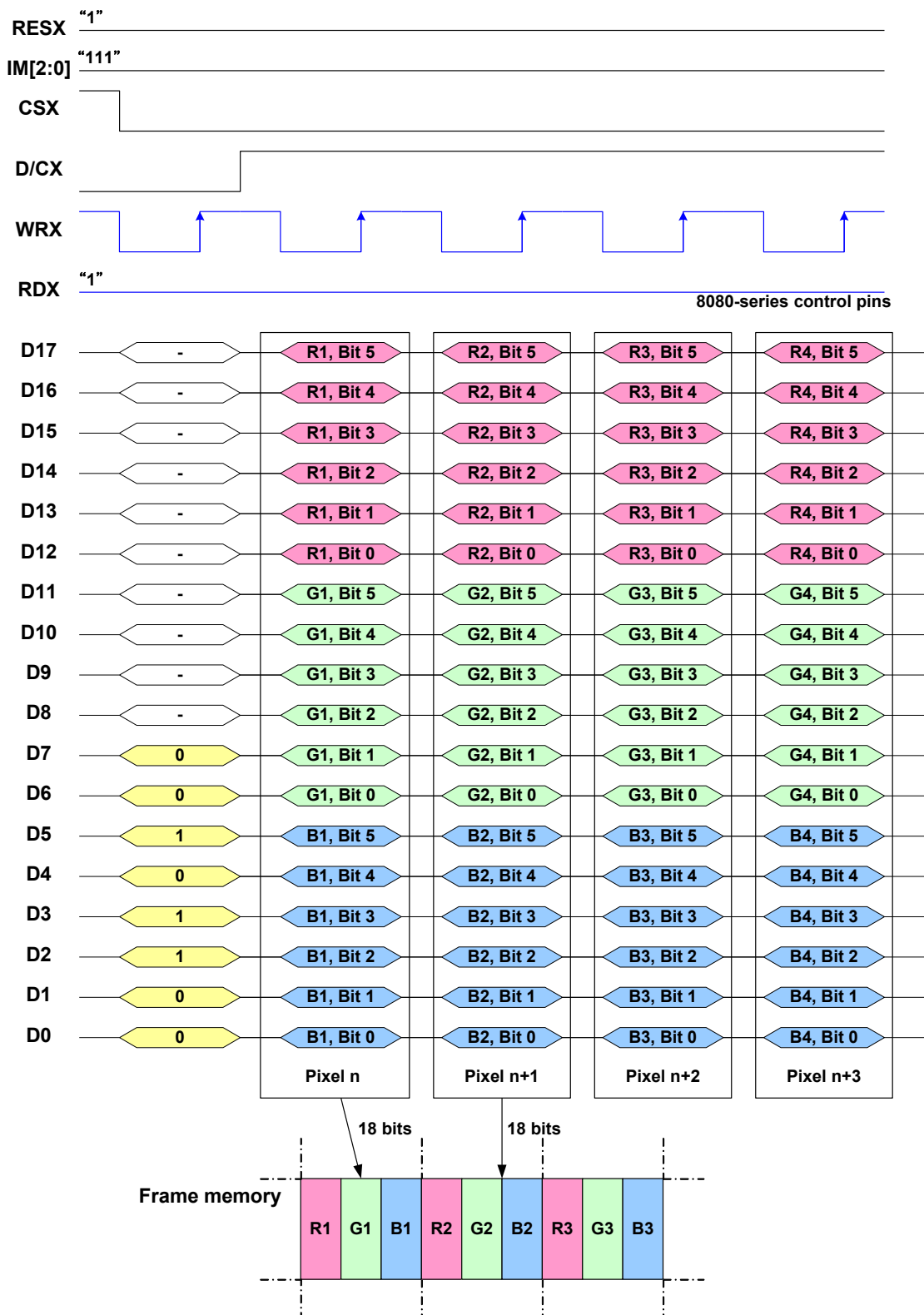


Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

9.8.14 18-bit Data Bus for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

9.8.15 3-line Serial Interface

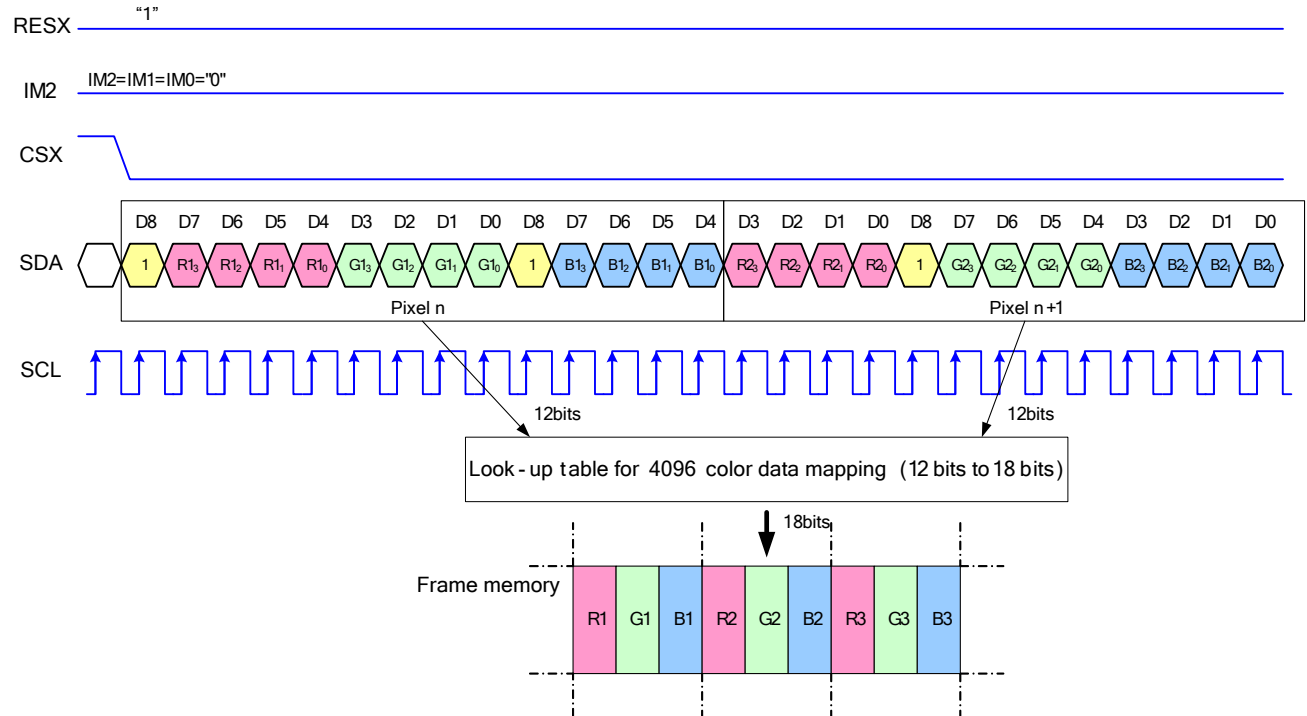
Different display data formats are available for three colors depth supported by the LCM listed below.

4k Colors, RGB 4-4-4-bit Input

65k Colors, RGB 5-6-5-bit Input

262k Colors, RGB 6-6-6-bit Input

9.8.16 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h"

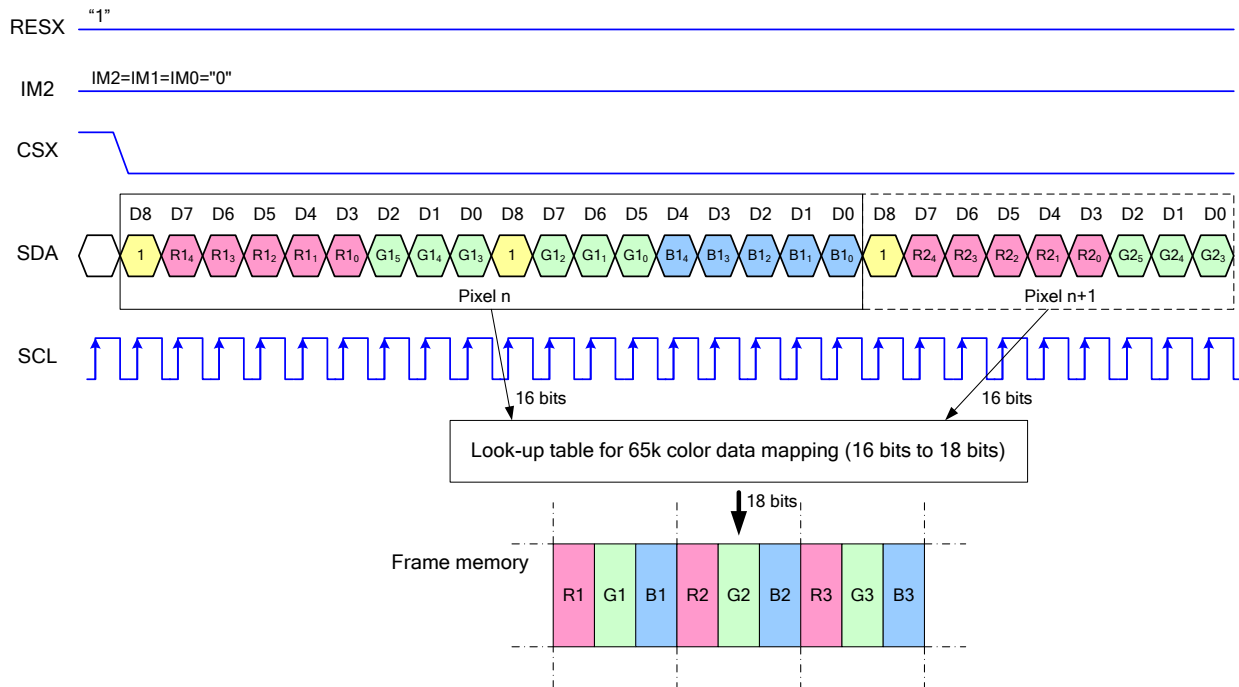


Note 1: Pixel data with the 12-bit color depth information

Note 2: The most significant bits are: Rx3, Gx3 and Bx3

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.17 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h"

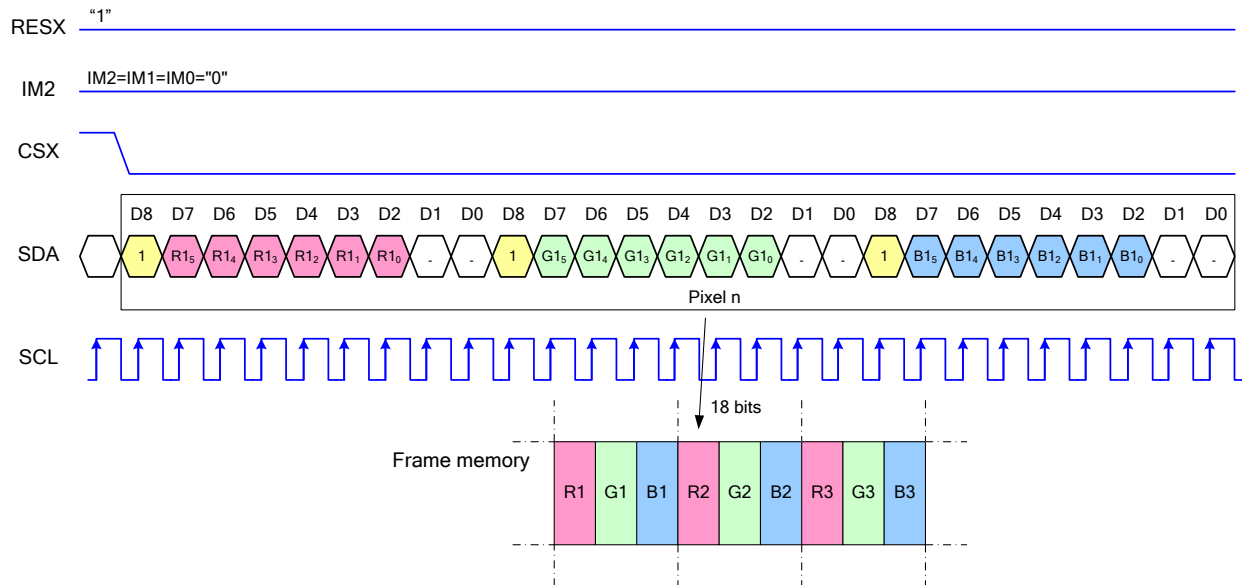


Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.18 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h"



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8.19 4-line Serial Interface

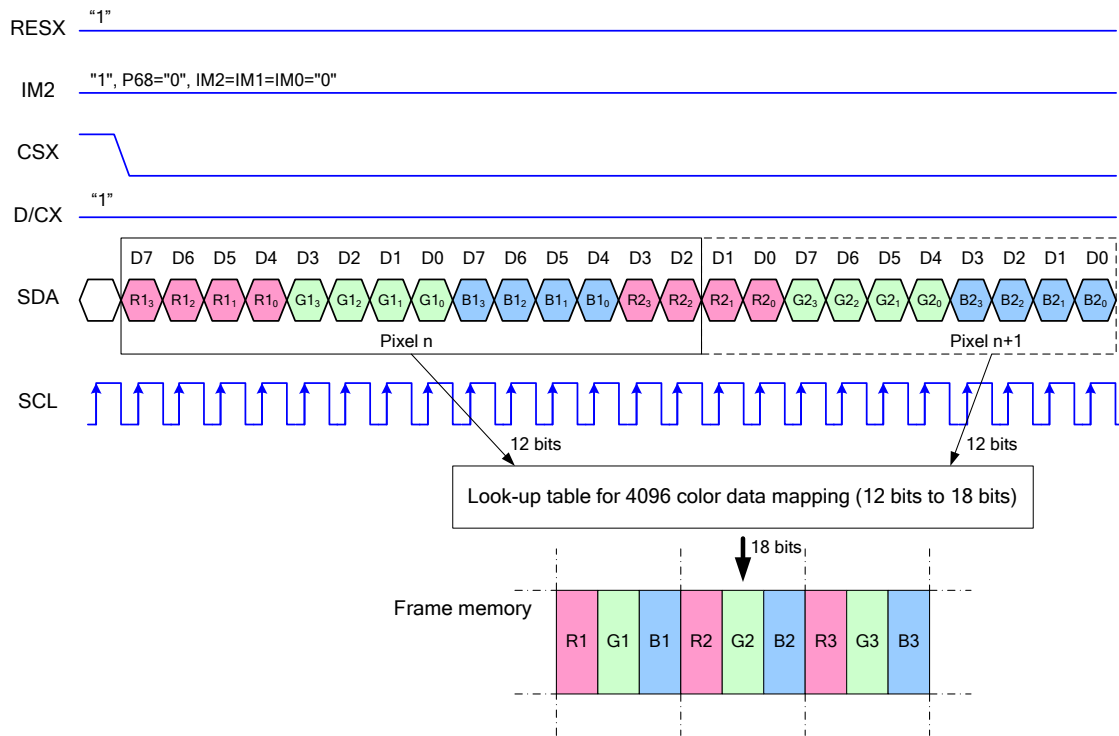
Different display data formats are available for three colors depth supported by the LCM listed below.

4k Colors, RGB 4-4-4-bit Input

65k Colors, RGB 5-6-5-bit Input

262k Colors, RGB 6-6-6-bit Input

9.8.20 Write Data for 12-bit/Pixel (RGB 4-4-4-bit Input), 4K-Colors, 3AH="03h"

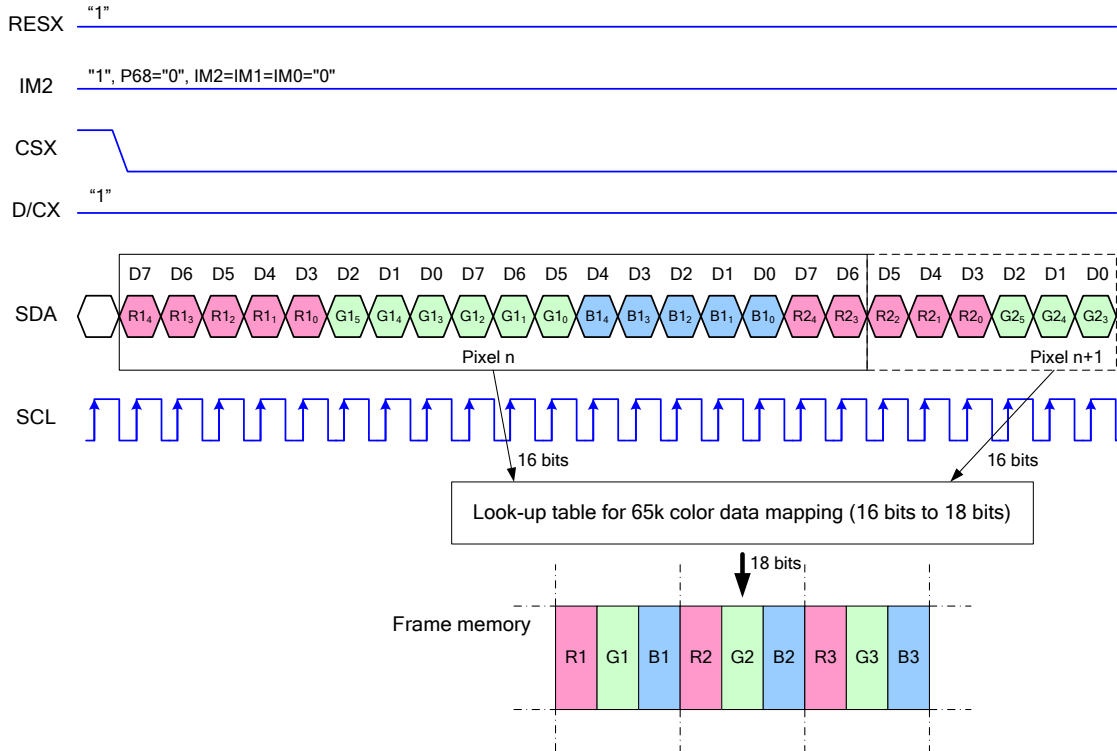


Note 1. Pixel data with the 12-bit color depth information

Note 2. The most significant bits are: Rx3, Gx3 and Bx3

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.21 Write Data for 16-bit/Pixel (RGB 5-6-5-bit Input), 65K-Colors, 3AH="05h"

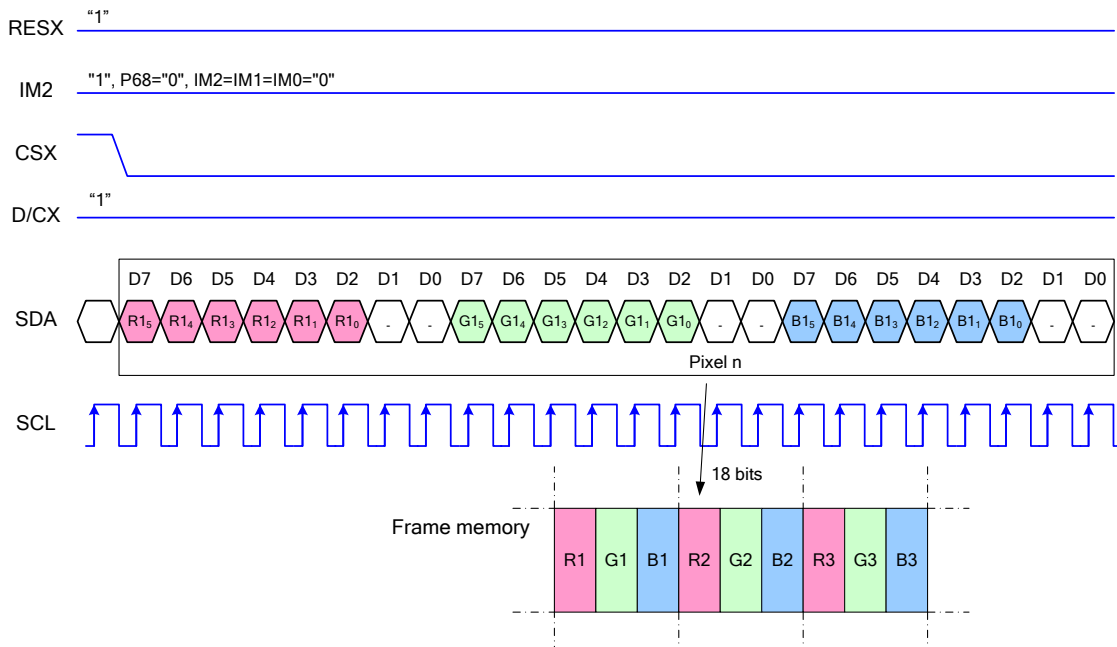


Note 1. Pixel data with the 16-bit color depth information

Note 2. The most significant bits are: Rx4, Gx5 and Bx4

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.8.22 Write Data for 18-bit/Pixel (RGB 6-6-6-bit Input), 262K-Colors, 3AH="06h"



Note 1. Pixel data with the 18-bit color depth information

Note 2. The most significant bits are: Rx5, Gx5 and Bx5

Note 3. The least significant bits are: Rx0, Gx0 and Bx0

9.9 Display Data RAM

9.9.1 Configuration (GM[1:0] = "00")

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

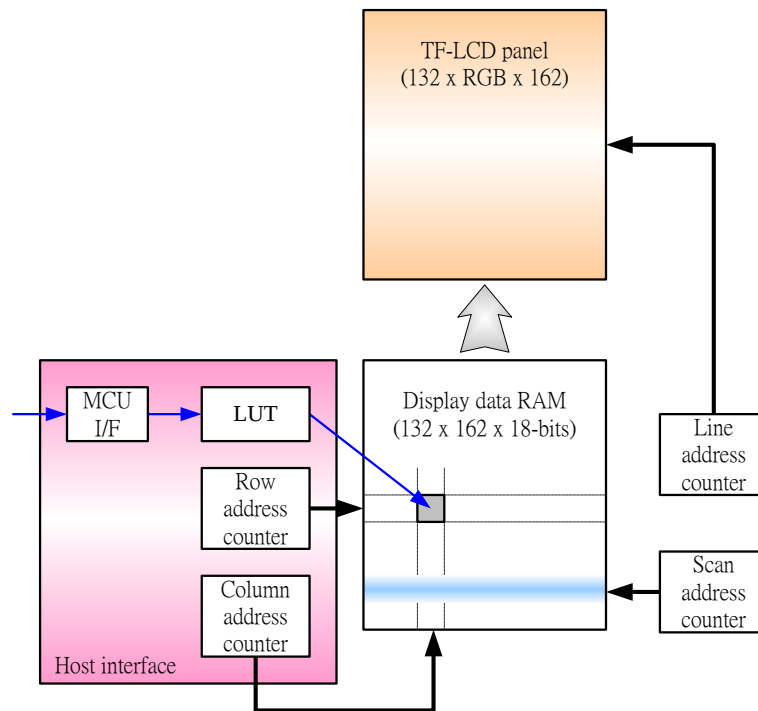
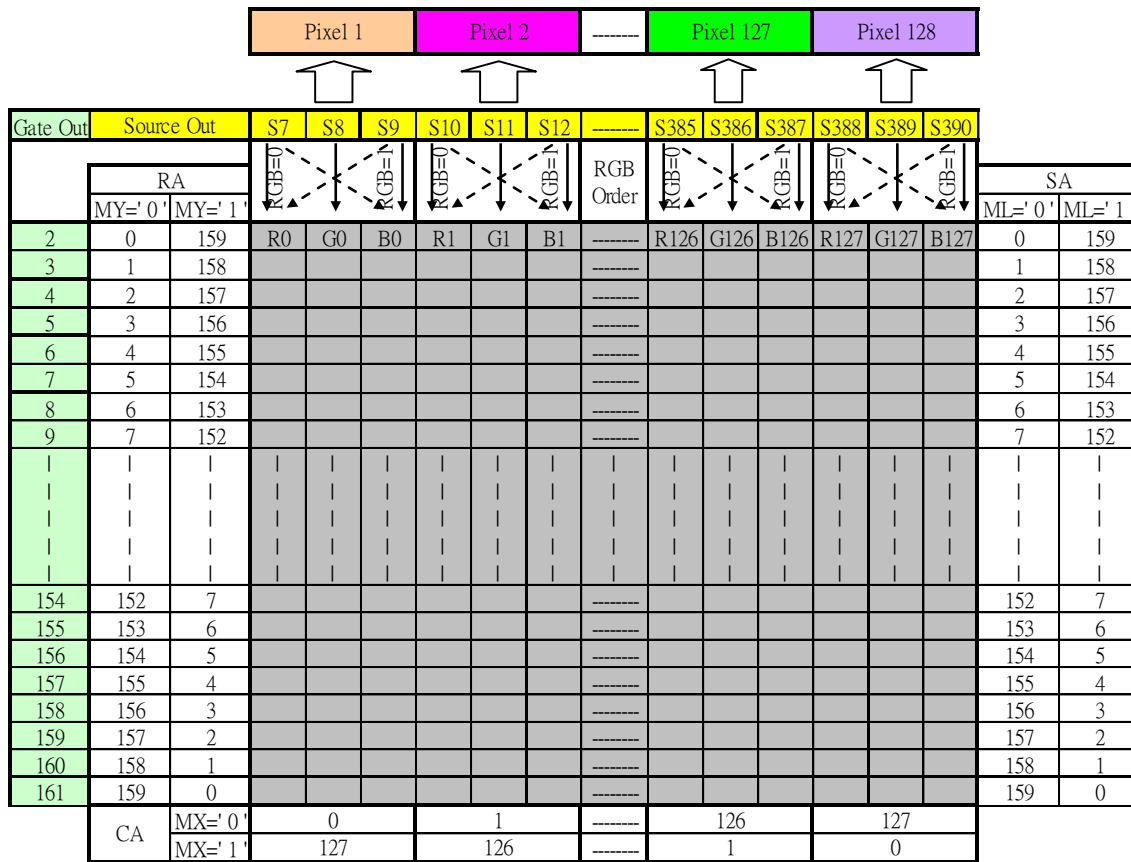


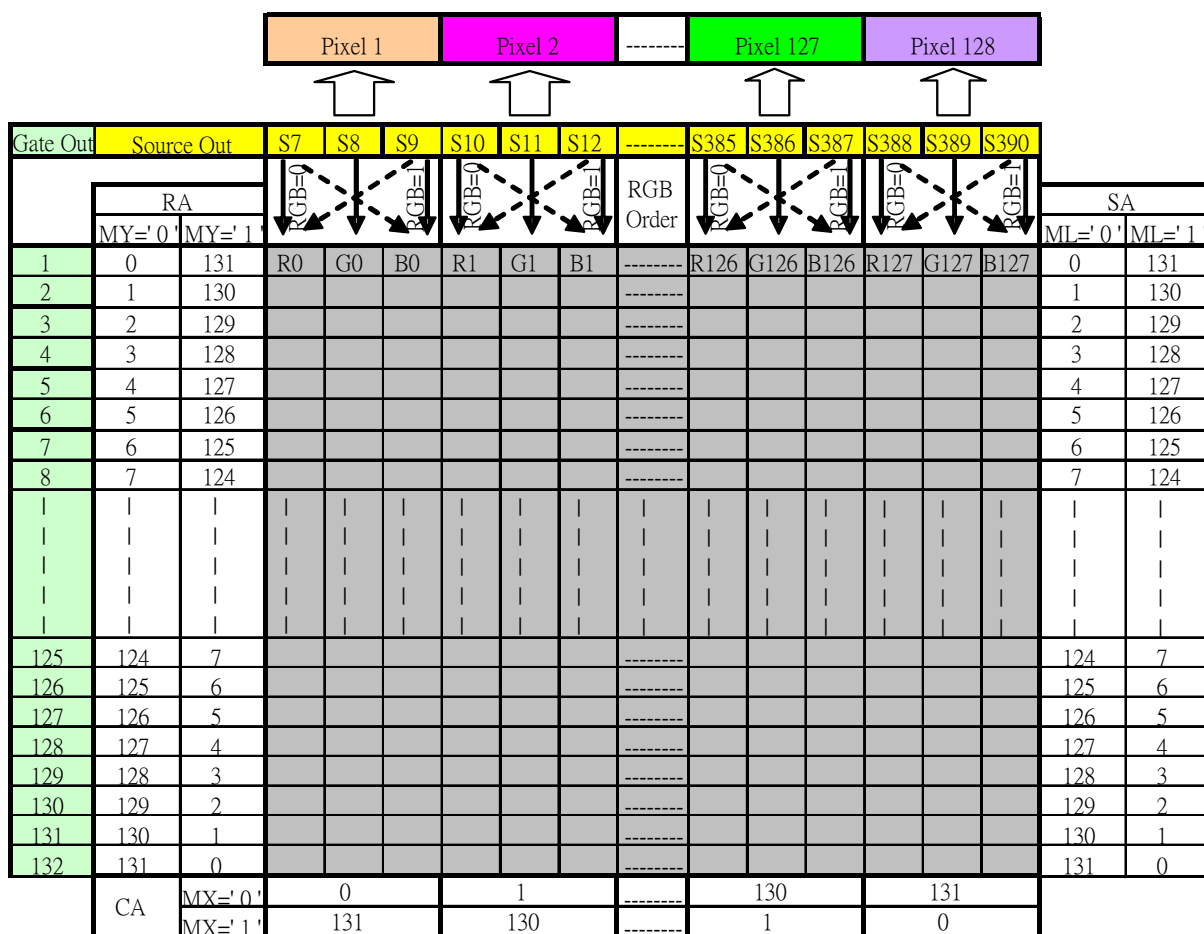
Figure 27 Display Data RAM Organization

9.9.2 Memory to Display Address Mapping

9.9.3 When using 128RGB x 160 resolution (GM[1:0] = "11", SMX=SMY=SRGB= '0')



9.9.4 When using 132RGB x 132resolution (GM[1:0] = "01", SMX=SMY=SRGB= '0')



Note

RA = Row Address,

CA = Column Address

SA = Scan Address

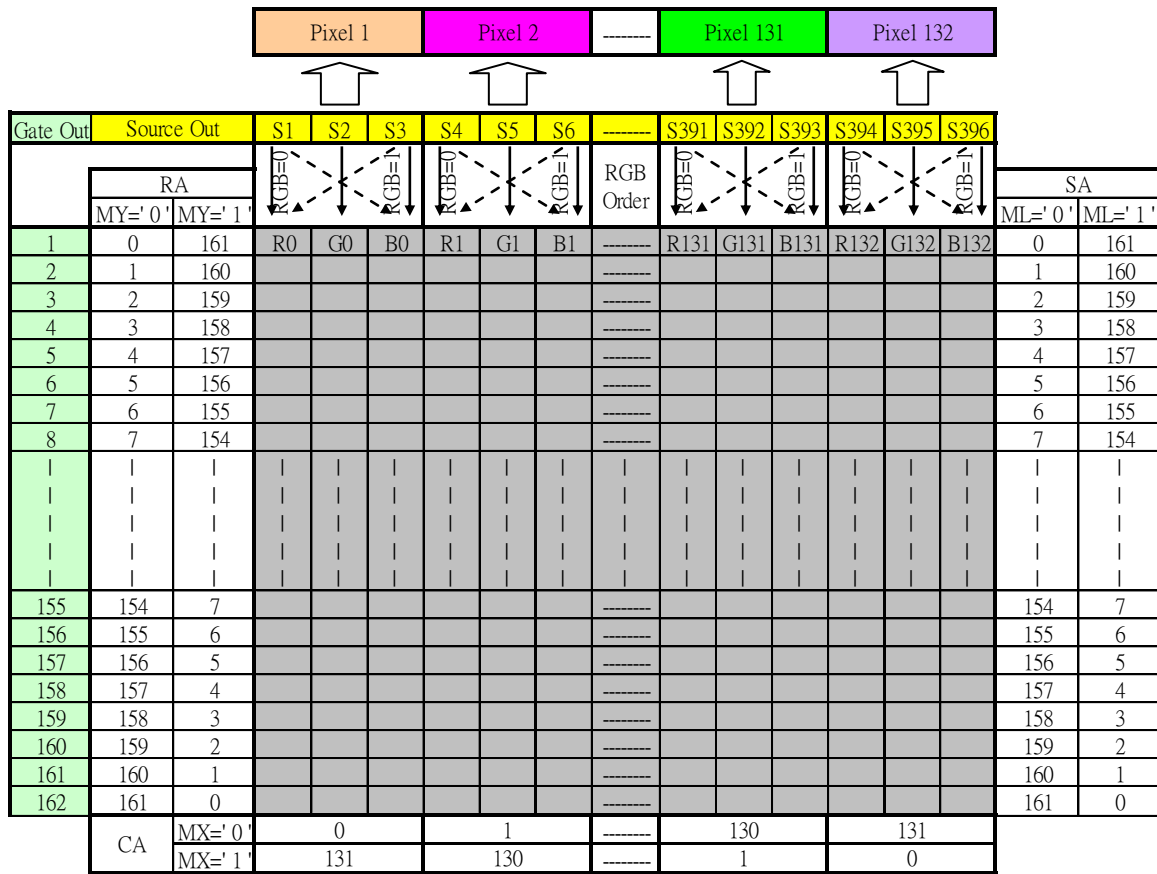
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.5 When using 132RGB x 162 resolution (GM[1:0] = "00", SMX=SMY=SRGB= '0')



Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

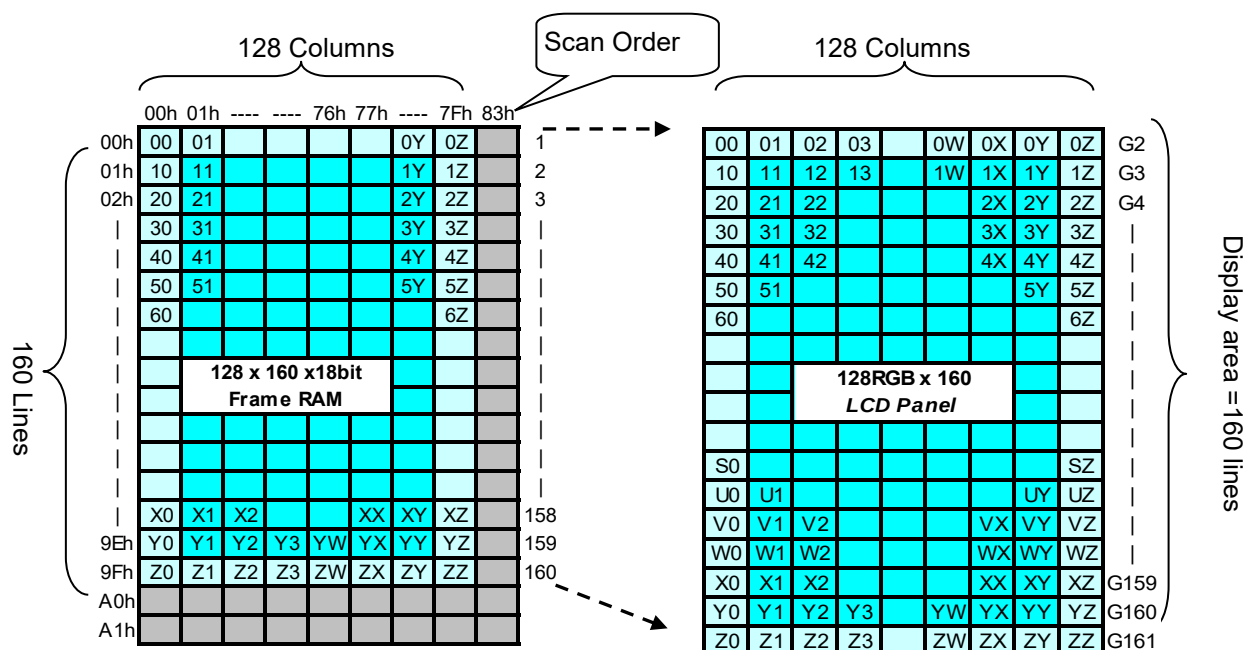
RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

9.9.6 Normal Display On or Partial Mode On

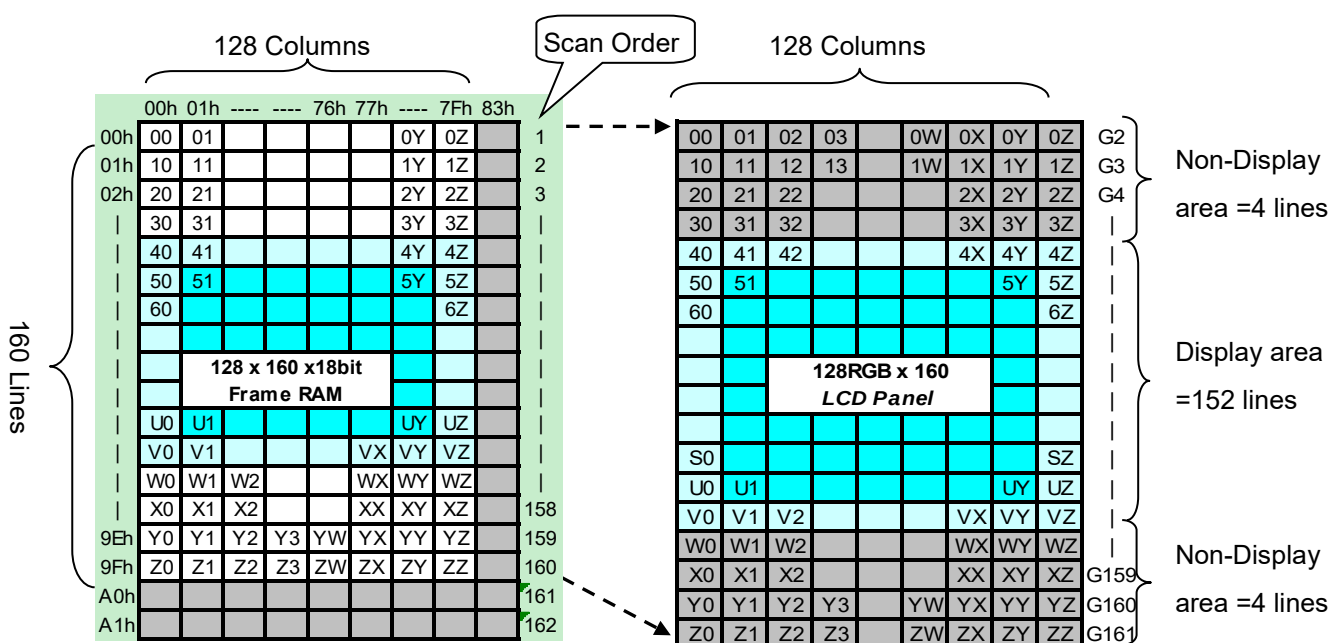
9.9.7 When using 128RGB x 160 resolution (GM[1:0] = "11")

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



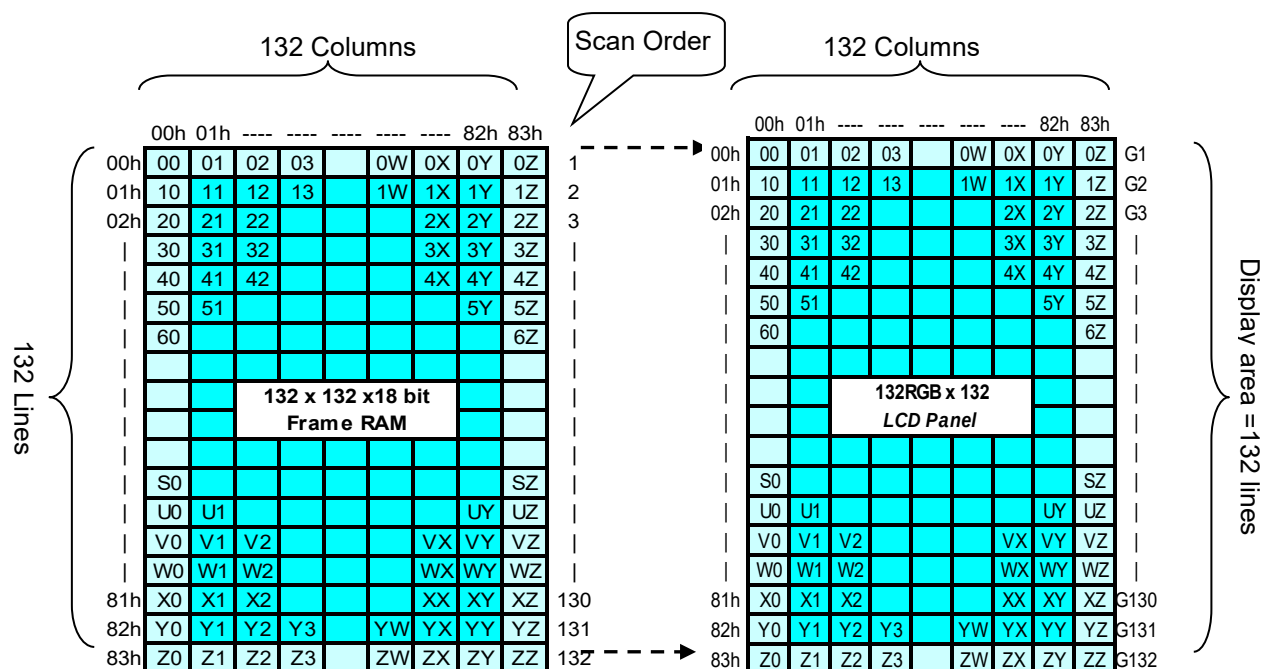
2). Example for Partial Display On (PSL[7:0]=04h, PEL[7:0]=9Bh, MX=MV=ML='0', SMX=SMY='0')



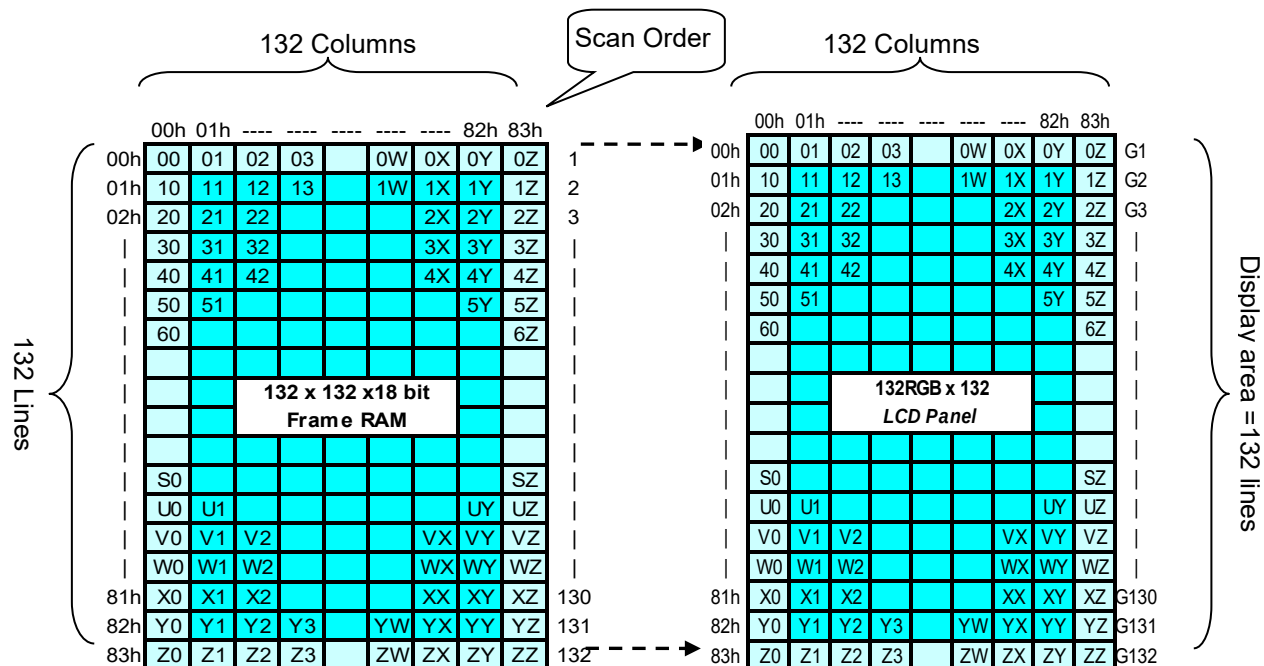
9.9.8 When using 128RGB x 160 resolution (GM[1:0] = "01")

In this mode, the content of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to 83h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



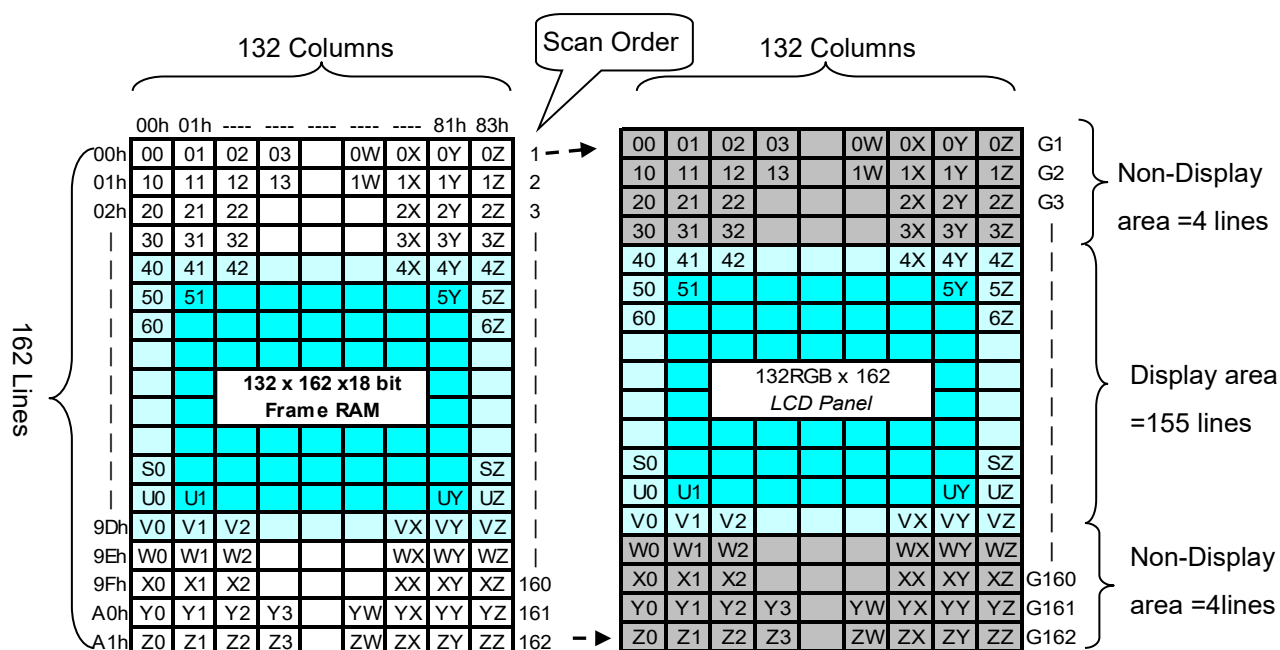
2). Example for Partial Display On (PSL[7:0]=00h, PEL[7:0]=83h, MX=MV=ML='0', SMX=SMY='0')



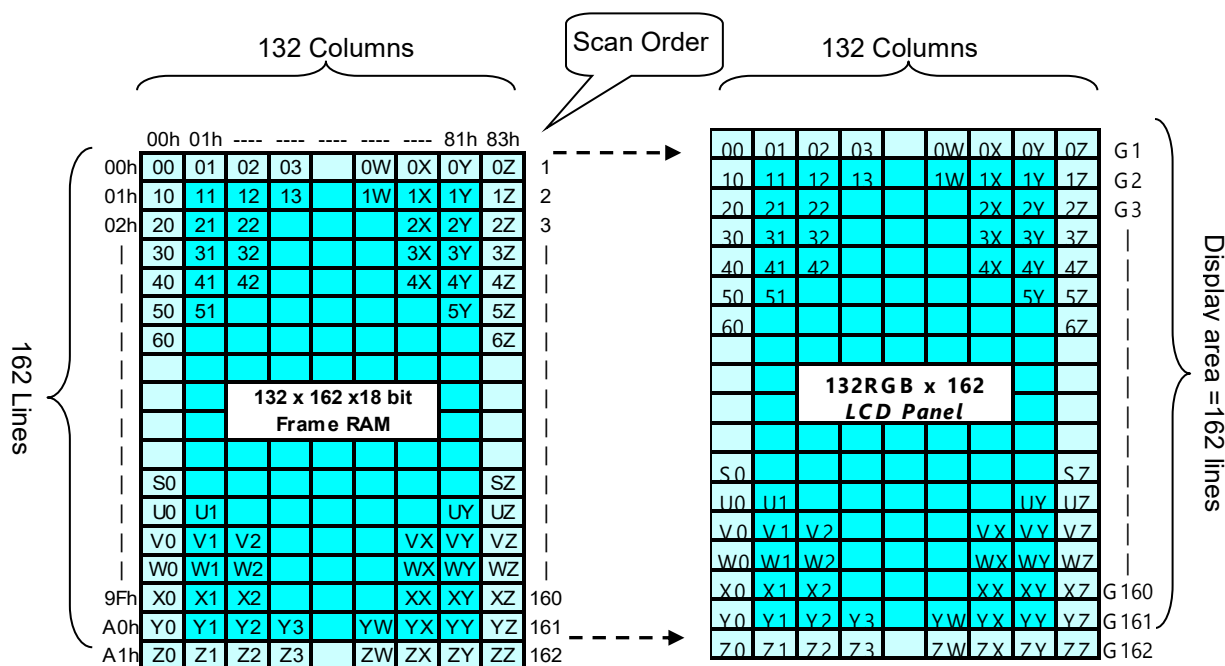
9.9.9 When using 132RGB x 162 resolution (GM[1:0] = "00")

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0)

1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



2). Example for Partial Display On (PSL[7:0]=04h, PEL[7:0]=9Dh, MX=MV=ML='0', SMX=SMY='0')



9.10 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET and MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data must be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.11 below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

9.11 Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

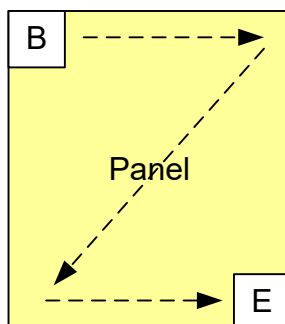


Figure 28 Data Streaming order

9.11.1 When 128RGBx160 (GM= “11”)

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

9.11.2 When 132RGBx132 (GM= “01”)

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (131-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (131-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (131-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (131-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

9.11.3 When 132RGBx162 (GM= “00”)

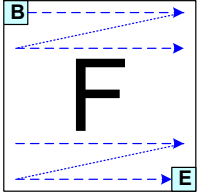
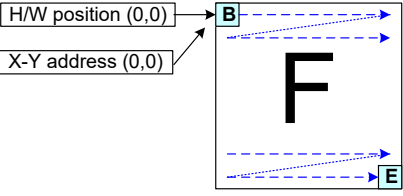
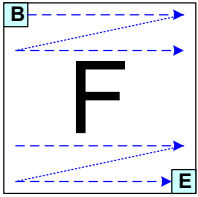
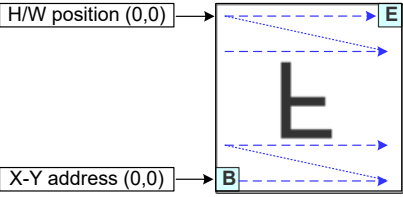
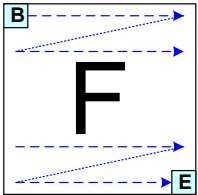
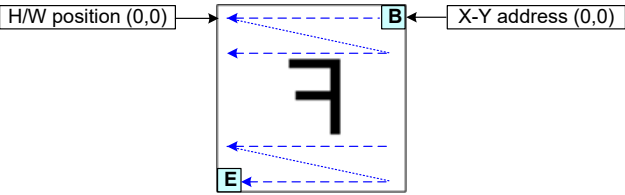
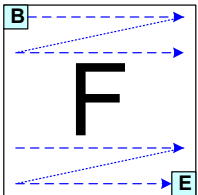
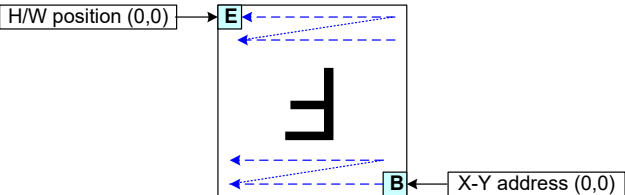
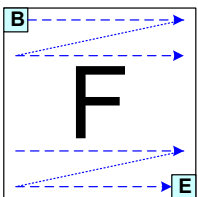
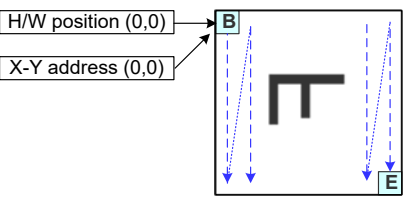
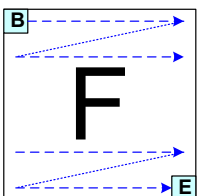
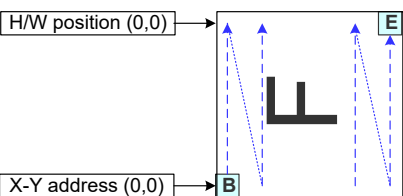
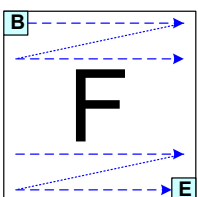
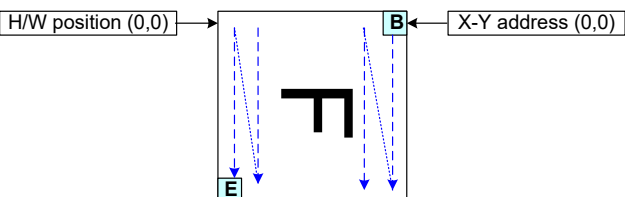
MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (161-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (161-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits D7 (MY), D6 (MX), D5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

9.11.4 Frame Data Write Direction According to the MADCTL Parameters (MV, MX and MY)

Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		

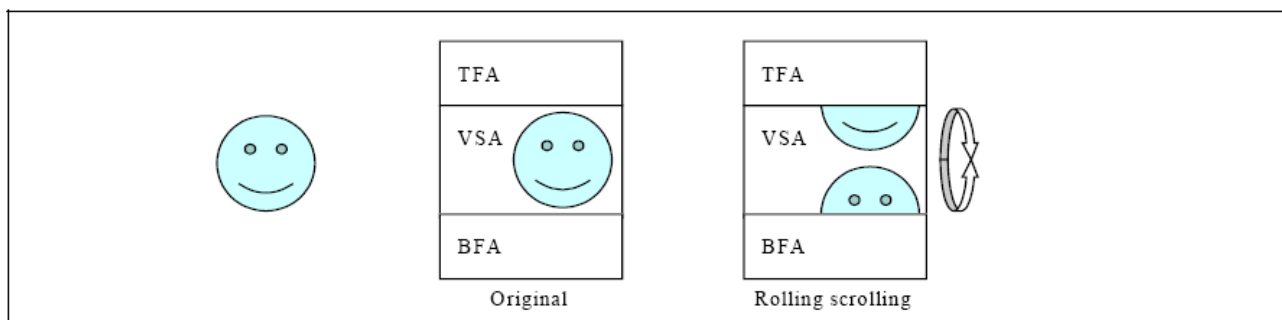
X-Y Exchange					
X-Mirror	1	1	1		
Y-Mirror					

9.11.5 Scroll Address Circuit

The circuit associates lines on DDRAM with Gate output. ST7735V processes signals for the liquid crystal display on 1-line basis. Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in line.

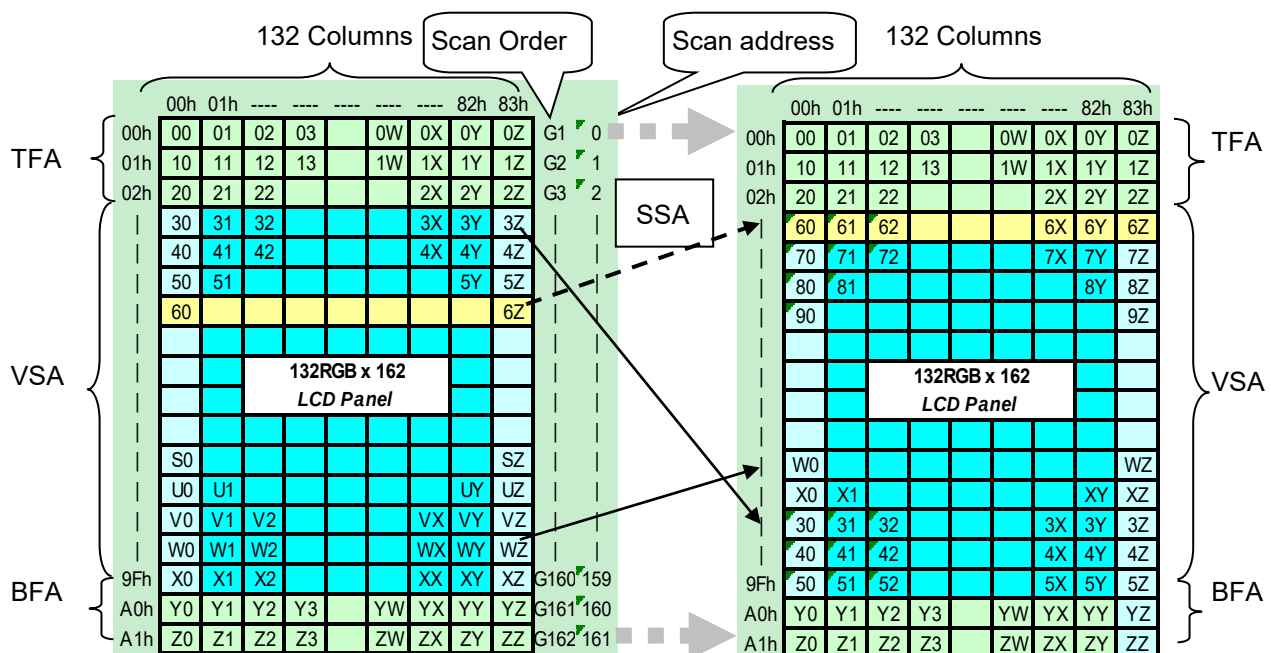
9.11.6 Vertical Scroll Mode

There is just one types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h)

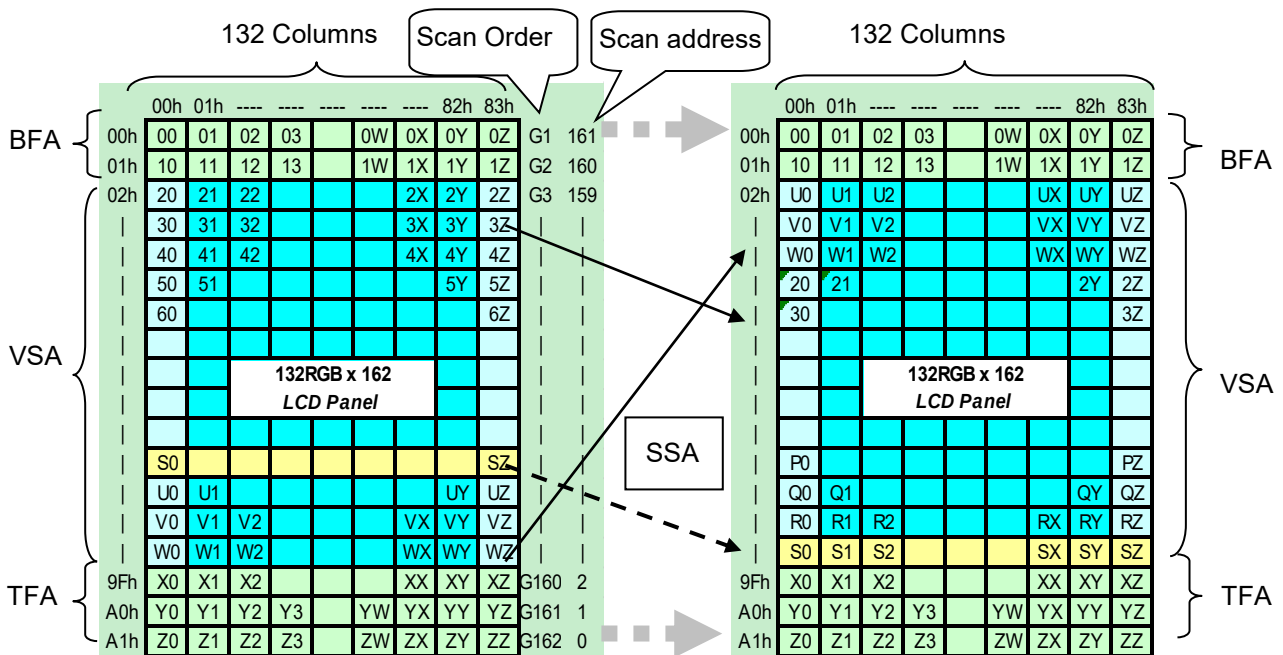


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =162. In this case, ‘rolling’ scrolling is applied as shown below. All the memory contents will be used.

Example 1) Panel size=132(RGB) x 162, TFA =3, VSA=157, BFA=2, SSA=6, MADCTR (ML) =0: Rolling Scroll



Example 2) Panel size=132(RGB) x 162, TFA =3, VSA=157, BFA=2, SSA=6, MADCTR (ML) =1: Rolling Scroll.



9.11.7 Vertical Scroll Example

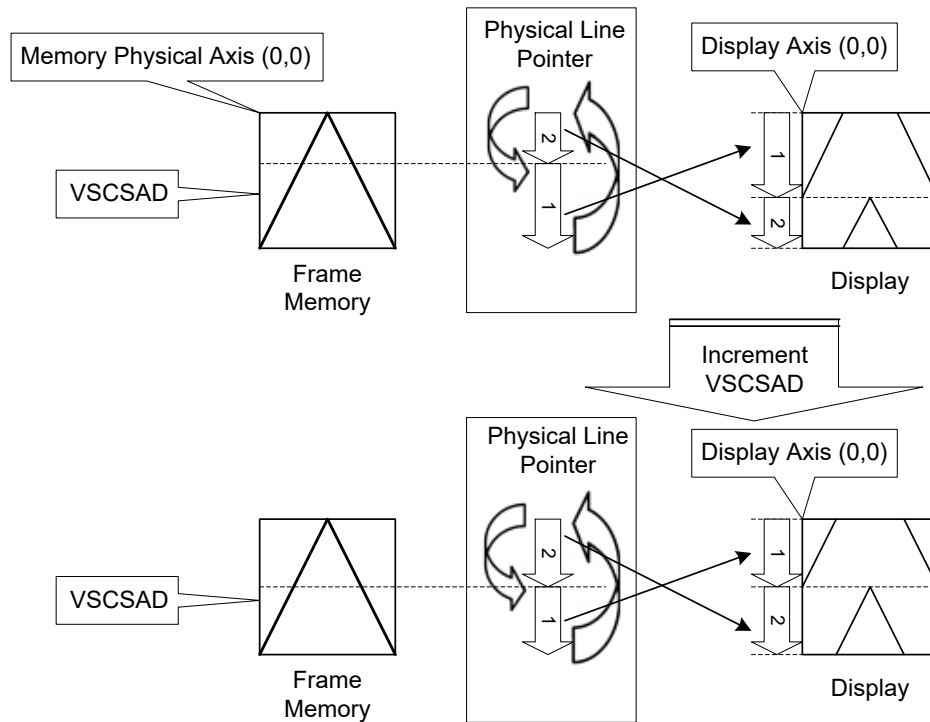
There are 2 types of vertical scrolling, which are determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

9.11.8 Case 1: TFA + VSA + BFA < 162

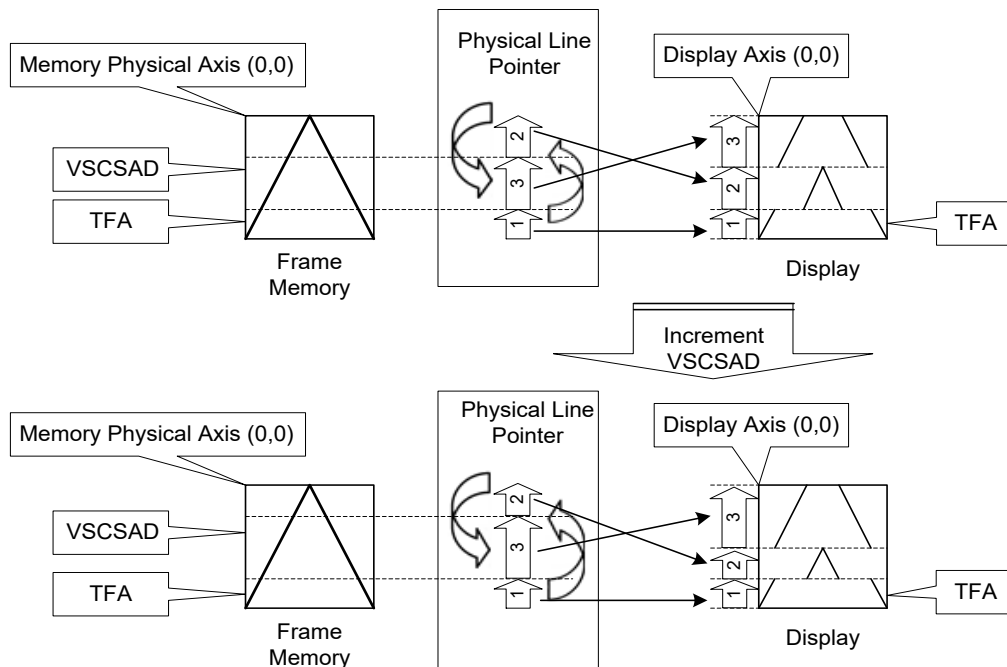
N/A. Do not set TFA + VSA + BFA < 162. In that case, unexpected picture will be shown.

9.11.9 Case 2: TFA + VSA + BFA=162 (Rolling Scrolling)

Example 2-a) When MADCTR parameter ML="0", TFA=0, VSA=162, BFA=0 and VSCSAD=40



Example 2-b) When MADCTR parameter ML="1", TFA=10, VSA=152, BFA=0 and VSCSAD=30

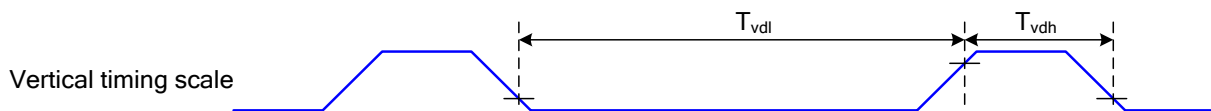


9.12 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

9.12.1 Tearing Effect Line Modes

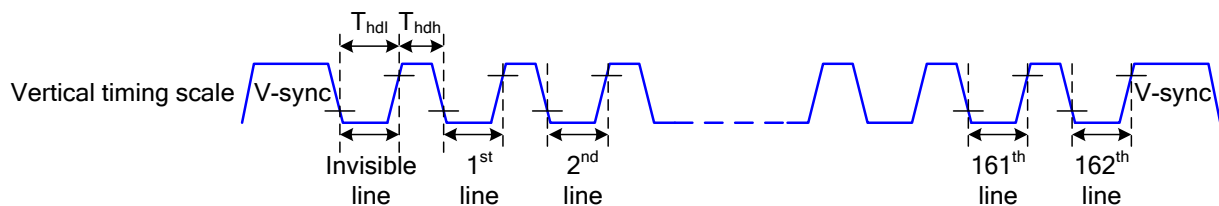
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh} = The LCD display is not updated from the Frame Memory

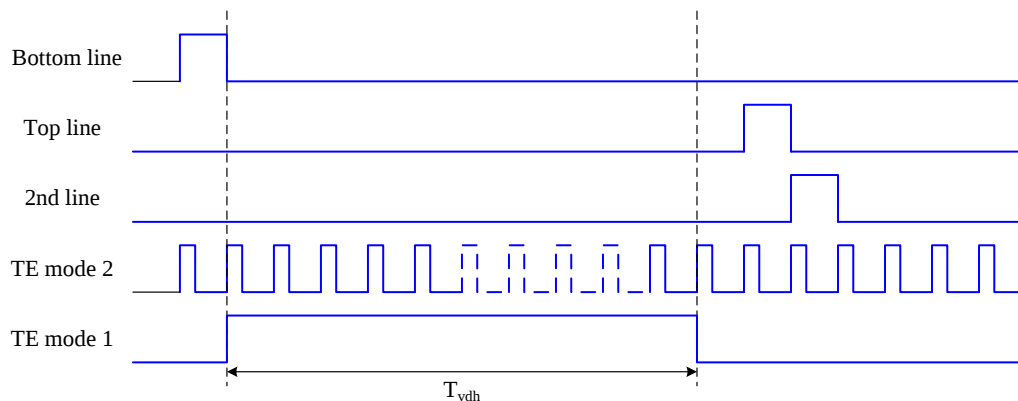
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



t_{hdh} = The LCD display is not updated from the Frame Memory

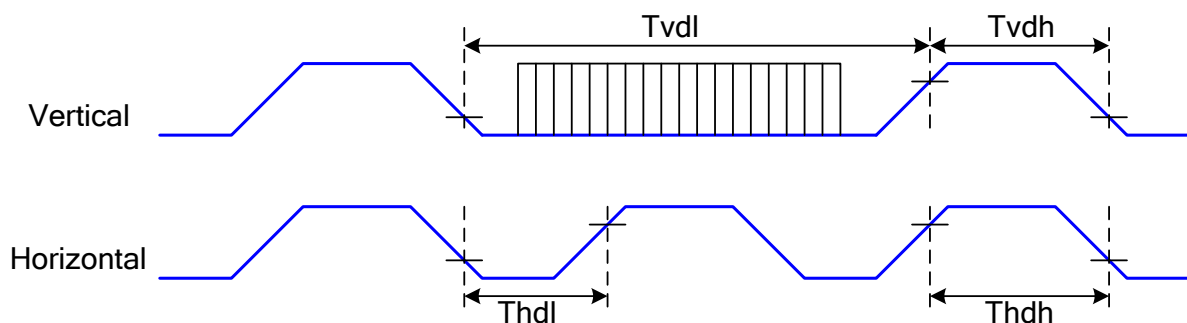
t_{hdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

9.12.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

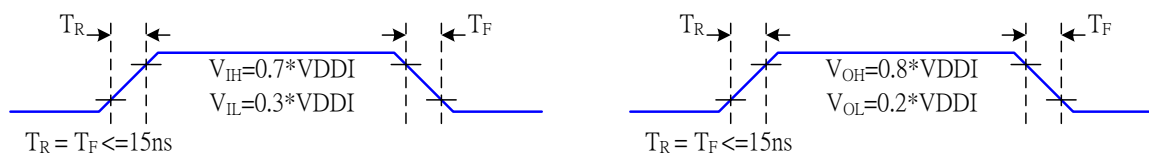


Symbol	Parameter	min	max	unit	description
Tvdl	Vertical Timing Low Duration	11	-	ms	
Tvdh	Vertical Timing High Duration	3000	-	μs	
Thdl	Horizontal Timing Low Duration	33	-	μs	
Thdh	Horizontal Timing Low Duration	25	500	μs	

Table 13 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

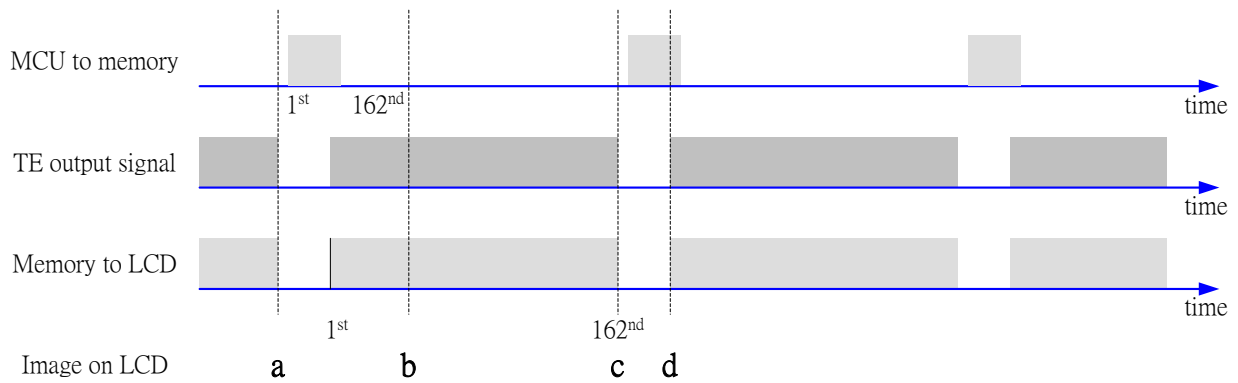
Note: The timings in Table 9.10.1 apply when MADCTL ML=0 and ML=1

The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.

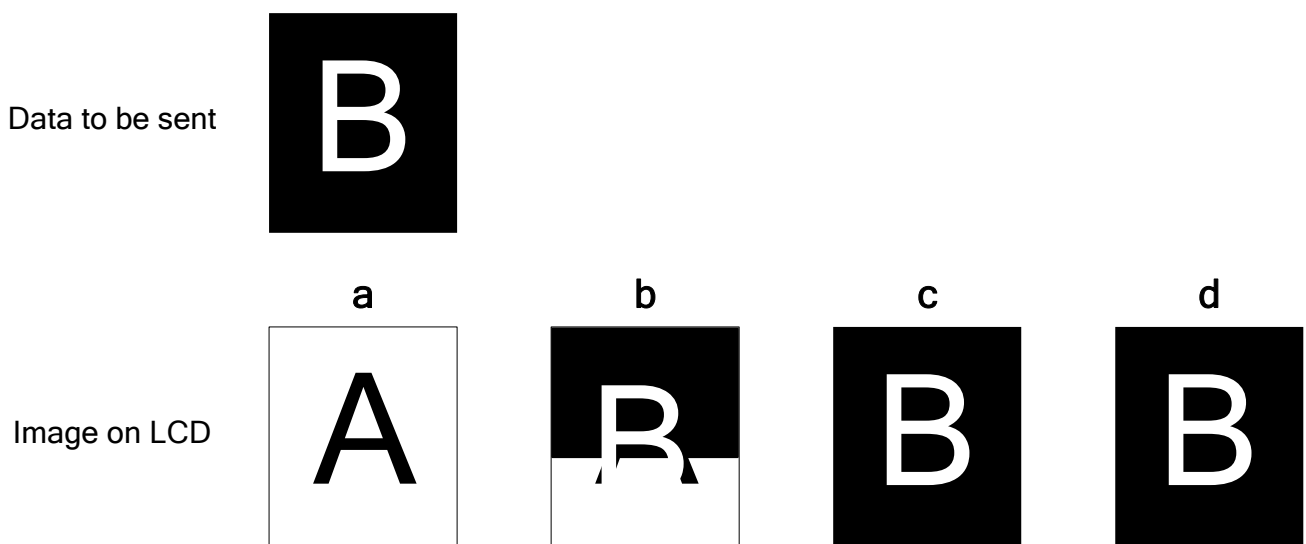


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

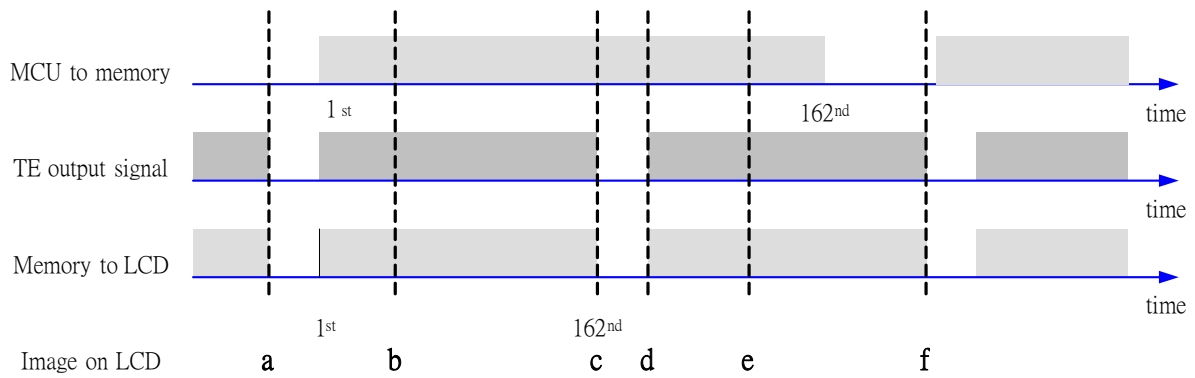
9.12.3 Example 1: MPU Write is faster than panel read



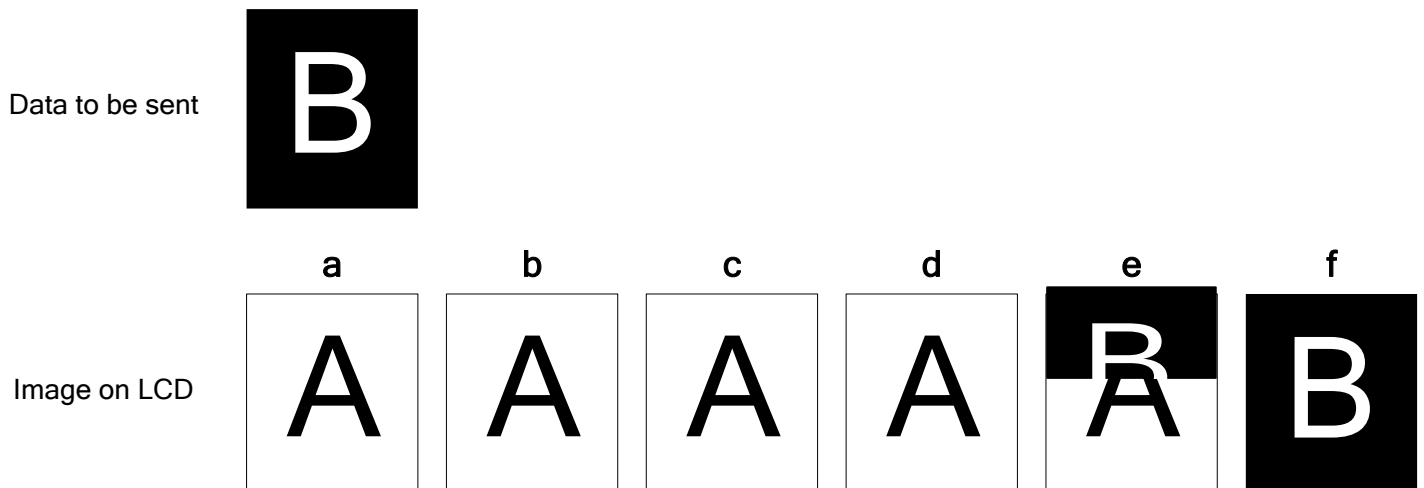
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



9.12.4 Example 2: MPU Write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MPU to Frame memory write position.



9.13 Power ON/OFF Sequence

VDDI and VDD can be applied in any order

VDD and VDDI can be powered down in any order

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

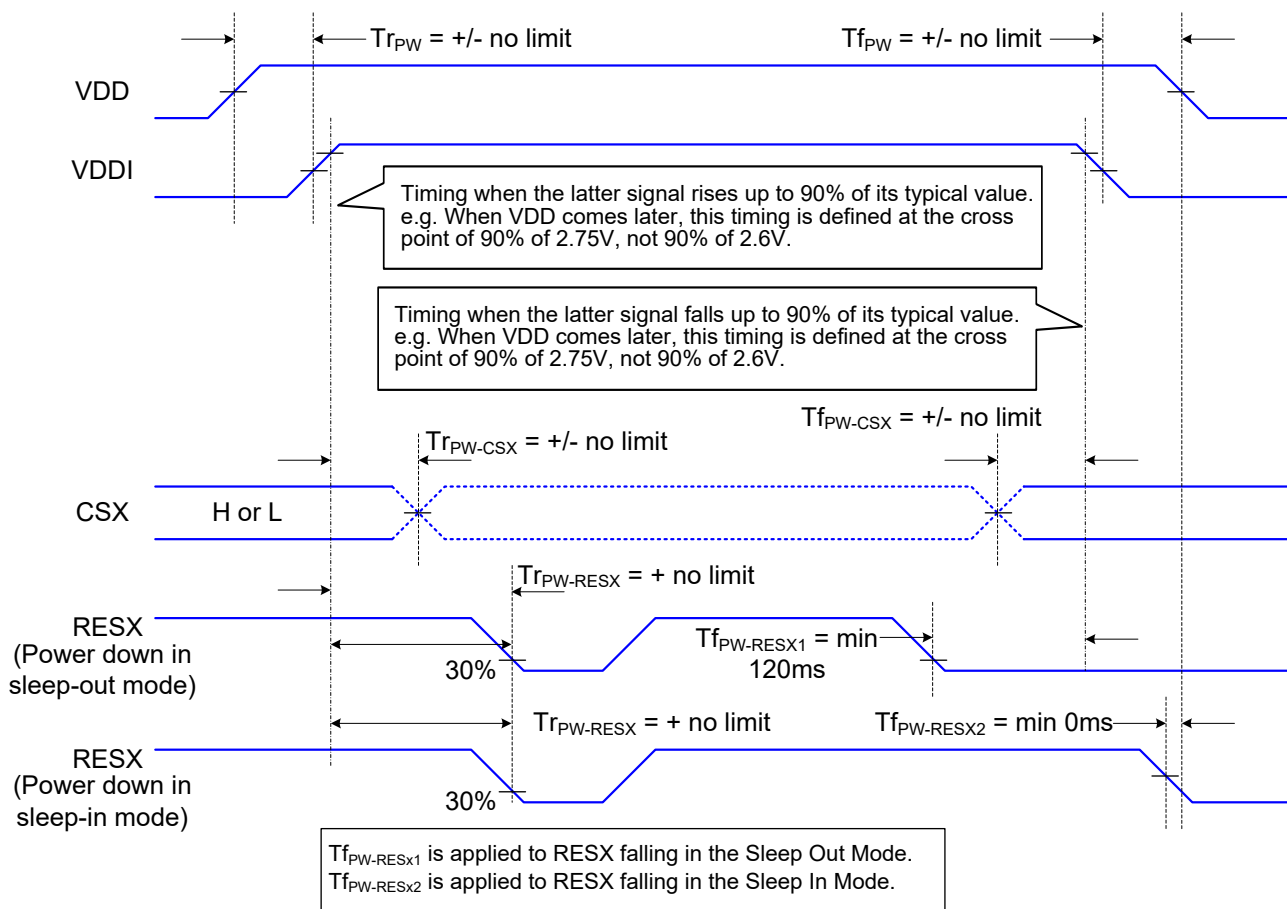
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



9.13.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

9.14 Power Level Definition

9.14.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

1. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

1. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

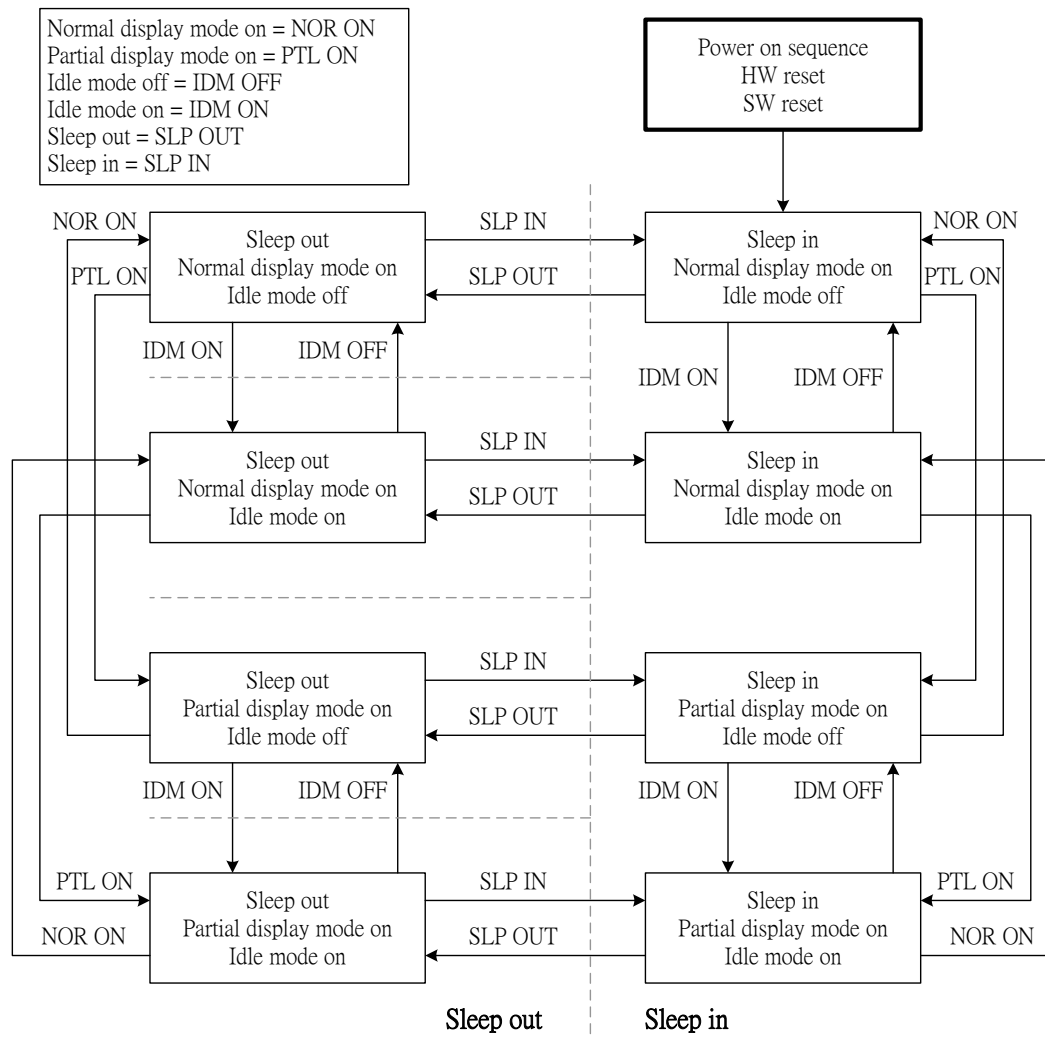
5. Sleep In Mode

In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.



9.15 Reset Table
9.15.1 Reset Table(Default Value, GM[1:0]="11", 128RGB x 160)

Item	After Power On	After H/W Reset	After S/W Reset
Frame Memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display Mode (Normal/Partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	Random values	Random values	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	00A0h	00A0h	00A0h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID1	NV value	NV value	NV value
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.15.2 Reset Table (GM[1:0]= “01”, 132RGB x 132)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display Mode (Normal/Partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 0083h (131d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	0083h	0083h	0083h (131d) (when MV=0) 0083h (131d) (when MV=1)
Gamma Setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	See Section 9.17	See Section 9.17	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	0083h	0083h	0083h
Tearing: On/Off	Off	Off	Off
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0084h	0084h	0084h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID1	NV value	NV value	NV value
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.15.3 Reset Table (GM[1:0]= "00", 132RGB x 162)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 00A1h (161d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00A1h	00A1h	00A1h (161d) (when MV=0) 0083h (131d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	Random values	Random values	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00A2h	00A2h	00A2h
Scroll: Top Fixed Area (TFA)	0000h	0000h	0000h
Scroll: Scroll Area (VSA)	0084h	0084h	0084h
Scroll: Bottom Fixed Area (BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
ID1	NV value	NV value	NV value
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

9.16 Module Input/Output Pins

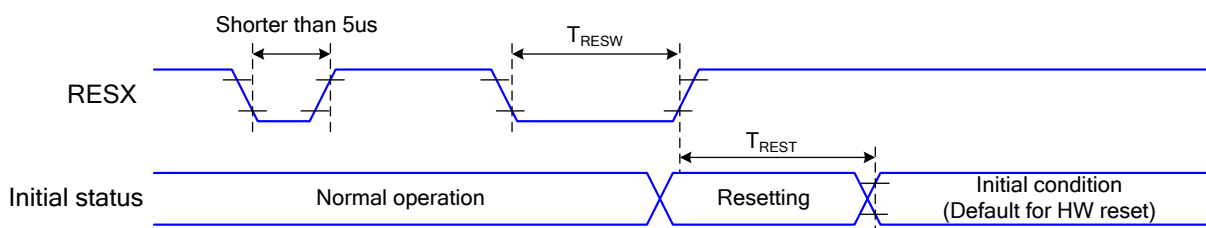
9.16.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.13	Input valid	Input valid	Input valid	See 9.13
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

9.17 Reset Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset Pulse Duration	10	-	us
	tREST	Reset Cancel	-	5 (Note1,5)	ms
				120 (Note1,6,7)	ms

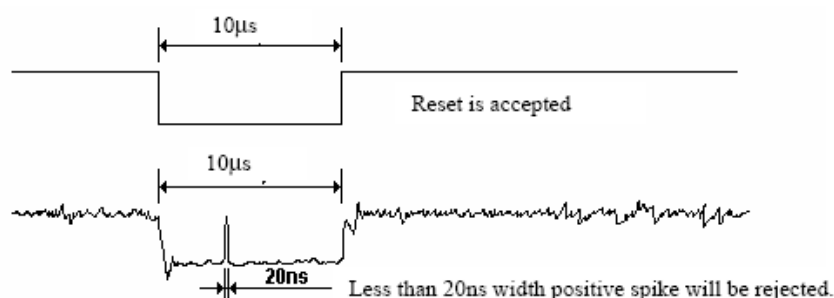
Table 14 Reset Timing

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9.18 Color Depth Conversion Look Up Tables
9.18.1 65536 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
RED	R005 R004 R003 R002 R001 R000	1	00000
	R015 R014 R013 R012 R011 R010	2	00001
	R025 R024 R023 R022 R021 R020	3	00010
	R035 R034 R033 R032 R031 R030	4	00011
	R045 R044 R043 R042 R041 R040	5	00100
	R055 R054 R053 R052 R051 R050	6	00101
	R065 R064 R063 R062 R061 R060	7	00110
	R075 R074 R073 R072 R071 R070	8	00111
	R085 R084 R083 R082 R081 R080	9	01000
	R095 R094 R093 R092 R091 R090	10	01001
	R105 R104 R103 R102 R101 R100	11	01010
	R115 R114 R113 R112 R111 R110	12	01011
	R125 R124 R123 R122 R121 R120	13	01100
	R135 R134 R133 R132 R131 R130	14	01101
	R145 R144 R143 R142 R141 R140	15	01110
	R155 R154 R153 R152 R151 R150	16	01111
	R165 R164 R163 R162 R161 R160	17	10000
	R175 R174 R173 R172 R171 R170	18	10001
	R185 R184 R183 R182 R181 R180	19	10010
	R195 R194 R193 R192 R191 R190	20	10011
	R205 R204 R203 R202 R201 R200	21	10100
	R215 R214 R213 R212 R211 R210	22	10101
	R225 R224 R223 R222 R221 R220	23	10110
	R235 R234 R233 R232 R231 R230	24	10111
	R245 R244 R243 R242 R241 R240	25	11000
	R255 R254 R253 R252 R251 R250	26	11001
	R265 R264 R263 R262 R261 R260	27	11010
	R275 R274 R273 R272 R271 R270	28	11011
	R285 R284 R283 R282 R281 R280	29	11100
	R295 R294 R293 R292 R291 R290	30	11101
	R305 R304 R303 R302 R301 R300	31	11110
	R315 R314 R313 R312 R311 R310	32	11111

Color	Look Up Table Output	RGBSET Parameter	Look Up Table Input Data
	Frame Memory Data (6-bits)		65k Color (5-bits)
GREEN	G005 G004 G003 G002 G001 G000	33	000000
	G015 G014 G013 G012 G011 G010	34	000001
	G025 G024 G023 G022 G021 G020	35	000010
	G035 G034 G033 G032 G031 G030	36	000011
	G045 G044 G043 G042 G041 G040	37	000100
	G055 G054 G053 G052 G051 G050	38	000101
	G065 G064 G063 G062 G061 G060	39	000110
	G075 G074 G073 G072 G071 G070	40	000111
	G085 G084 G083 G082 G081 G080	41	001000
	G095 G094 G093 G092 G091 G090	42	001001
	G105 G104 G103 G102 G101 G100	43	001010
	G115 G114 G113 G112 G111 G110	44	001011
	G125 G124 G123 G122 G121 G120	45	001100
	G135 G134 G133 G132 G131 G130	46	001101
	G145 G144 G143 G142 G141 G140	47	001110
	G155 G154 G153 G152 G151 G150	48	001111
	G165 G164 G163 G162 G161 G160	49	010000
	G175 G174 G173 G172 G171 G170	50	010001
	G185 G184 G183 G182 G181 G180	51	010010
	G195 G194 G193 G192 G191 G190	52	010011
	G205 G204 G203 G202 G201 G200	53	010100
	G215 G214 G213 G212 G211 G210	54	010101
	G225 G224 G223 G222 G221 G220	55	010110
	G235 G234 G233 G232 G231 G230	56	010111
	G245 G244 G243 G242 G241 G240	57	011000
	G255 G254 G253 G252 G251 G250	58	011001
	G265 G264 G263 G262 G261 G260	59	011010
	G275 G 274 G273 G272 G271 G270	60	011011
	G285 G 284 G283 G282 G281 G280	61	011100
	G295 G 294 G293 G292 G291 G290	62	011101
	G305 G 304 G303 G302 G301 G300	63	011110
	G315 G 314 G313 G312 G311 G310	64	011111
	G325 G324 G323 G322 G321 G320	65	100000
	G335 G334 G333 G332 G331 G330	66	100001
	G345 G344 G343 G342 G341 G340	67	100010
	G355 G354 G353 G352 G351 G350	68	100011

G365 G364 G363 G362 G361 G360	69	100100
G375 G374 G373 G372 G371 G370	70	100101
G385 G384 G383 G382 G381 G380	71	100110
G395 G394 G393 G392 G391 G390	72	100111
G405 G404 G403 G402 G401 G400	73	101000
G415 G414 G413 G412 G411 G410	74	101001
G425 G424 G423 G422 G421 G420	75	101010
G435 G434 G433 G432 G431 G430	76	101011
G445 G444 G443 G442 G441 G440	77	101100
G455 G454 G453 G452 G451 G450	78	101101
G465 G464 G463 G462 G461 G460	79	101110
G475 G474 G473 G472 G471 G470	80	101111
G485 G484 G483 G482 G481 G480	81	110000
G495 G494 G493 G492 G491 G490	82	110001
G505 G504 G503 G502 G501 G500	83	110010
G515 G514 G513 G512 G511 G510	84	110011
G525 G524 G523 G522 G521 G520	85	110100
G535 G534 G533 G532 G531 G530	86	110101
G545 G544 G543 G542 G541 G540	87	110110
G555 G554 G553 G552 G551 G550	88	110111
G565 G564 G563 G562 G561 G560	89	111000
G575 G574 G573 G572 G571 G570	90	111001
G585 G584 G583 G582 G581 G580	91	111010
G595 G594 G593 G592 G591 G590	92	111011
G605 G604 G603 G602 G601 G600	93	111100
G615 G614 G613 G612 G611 G610	94	111101
G625 G624 G623 G622 G621 G620	95	111110
G635 G634 G633 G632 G631 G630	96	111111

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 65k Color (5-bits)
BLUE	B005 B004 B003 B002 B001 B000	97	00000
	B015 B014 B013 B012 B011 B010	98	00001
	B025 B024 B023 B022 B021 B020	99	00010
	B035 B034 B033 B032 B031 B030	100	00011
	B045 B044 B043 B042 B041 B040	101	00100
	B055 B054 B053 B052 B051 B050	102	00101
	B065 B064 B063 B062 B061 B060	103	00110

B075 B074 B073 B072 B071 B070	104	00111
B085 B084 B083 B082 B081 B080	105	01000
B095 B094 B093 B092 B091 B090	106	01001
B105 B104 B103 B102 B101 B100	107	01010
B115 B114 B113 B112 B111 B110	108	01011
B125 B124 B123 B122 B121 B120	109	01100
B135 B134 B133 B132 B131 B130	110	01101
B145 B144 B143 B142 B141 B140	111	01110
B155 B154 B153 B152 B151 B150	112	01111
B165 B164 B163 B162 B161 B160	113	10000
B175 B174 B173 B172 B171 B170	114	10001
B185 B184 B183 B182 B181 B180	115	10010
B195 B194 B193 B192 B191 B190	116	10011
B205 B204 B203 B202 B201 B200	117	10100
B215 B214 B213 B212 B211 B210	118	10101
B225 B224 B223 B222 B221 B220	119	10110
B235 B234 B233 B232 B231 B230	120	10111
B245 B244 B243 B242 B241 B240	121	11000
B255 B254 B253 B252 B251 B250	122	11001
B265 B264 B263 B262 B261 B260	123	11010
B275 B274 B273 B272 B271 B270	124	11011
B285 B284 B283 B282 B281 B280	125	11100
B295 B294 B293 B292 B291 B290	126	11101
B305 B304 B303 B302 B301 B300	127	11110
B315 B314 B313 B312 B311 B310	128	11111

9.18.2 4096 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	RGBSET Parameter	Look Up Table Input Data 4k Color (4-bits)
RED	R005 R004 R003 R002 R001 R000	1	0000
	R015 R014 R013 R012 R011 R010	2	0001
	R025 R024 R023 R022 R021 R020	3	0010
	R035 R034 R033 R032 R031 R030	4	0011
	R045 R044 R043 R042 R041 R040	5	0100
	R055 R054 R053 R052 R051 R050	6	0101
	R065 R064 R063 R062 R061 R060	7	0110
	R075 R074 R073 R072 R071 R070	8	0111
	R085 R084 R083 R082 R081 R080	9	1000
	R095 R094 R093 R092 R091 R090	10	1001
	R105 R104 R103 R102 R101 R100	11	1010
	R115 R114 R113 R112 R111 R110	12	1011
	R125 R124 R123 R122 R121 R120	13	1100
	R135 R134 R133 R132 R131 R130	14	1101
	R145 R144 R143 R142 R141 R140	15	1110
	R155 R154 R153 R152 R151 R150	16	1111
	R165 R164 R163 R162 R161 R160	17	Not used
	R315 R314 R313 R312 R311 R310	32	
GREEN	G005 G004 G003 G002 G001 G000	33	0000
	G015 G014 G013 G012 G011 G010	34	0001
	G025 G024 G023 G022 G021 G020	35	0010
	G035 G034 G033 G032 G031 G030	36	0011
	G045 G044 G043 G042 G041 G040	37	0100
	G055 G054 G053 G052 G051 G050	38	0101
	G065 G064 G063 G062 G061 G060	39	0110
	G075 G074 G073 G072 G071 G070	40	0111
	G085 G084 G083 G082 G081 G080	41	1000
	G095 G094 G093 G092 G091 G090	42	1001
	G105 G104 G103 G102 G101 G100	43	1010
	G115 G114 G113 G112 G111 G110	44	1011
	G125 G124 G123 G122 G121 G120	45	1100
	G135 G134 G133 G132 G131 G130	46	1101
	G145 G144 G143 G142 G141 G140	47	1110
	G155 G154 G153 G152 G151 G150	48	1111

	G165 G164 G163 G162 G161 G160	49	Not used
	G635 G634 G633 G632 G631 G630	96	
BLUE	B005 B004 B003 B002 B001 B000	97	0000
	B015 B014 B013 B012 B011 B010	98	0001
	B025 B024 B023 B022 B021 B020	99	0010
	B035 B034 B033 B032 B031 B030	100	0011
	B045 B044 B043 B042 B041 B040	101	0100
	B055 B054 B053 B052 B051 B050	102	0101
	B065 B064 B063 B062 B061 B060	103	0110
	B075 B074 B073 B072 B071 B070	104	0111
	B085 B084 B083 B082 B081 B080	105	1000
	B095 B094 B093 B092 B091 B090	106	1001
	B105 B104 B103 B102 B101 B100	107	1010
	B115 B114 B113 B112 B111 B110	108	1011
	B125 B124 B123 B122 B121 B120	109	1100
	B135 B134 B133 B132 B131 B130	110	1101
	B145 B144 B143 B142 B141 B140	111	1110
	B155 B154 B153 B152 B151 B150	112	1111
	B165 B164 B163 B162 B161 B160	113	Not used
	B315 B314 B313 B312 B311 B310	128	

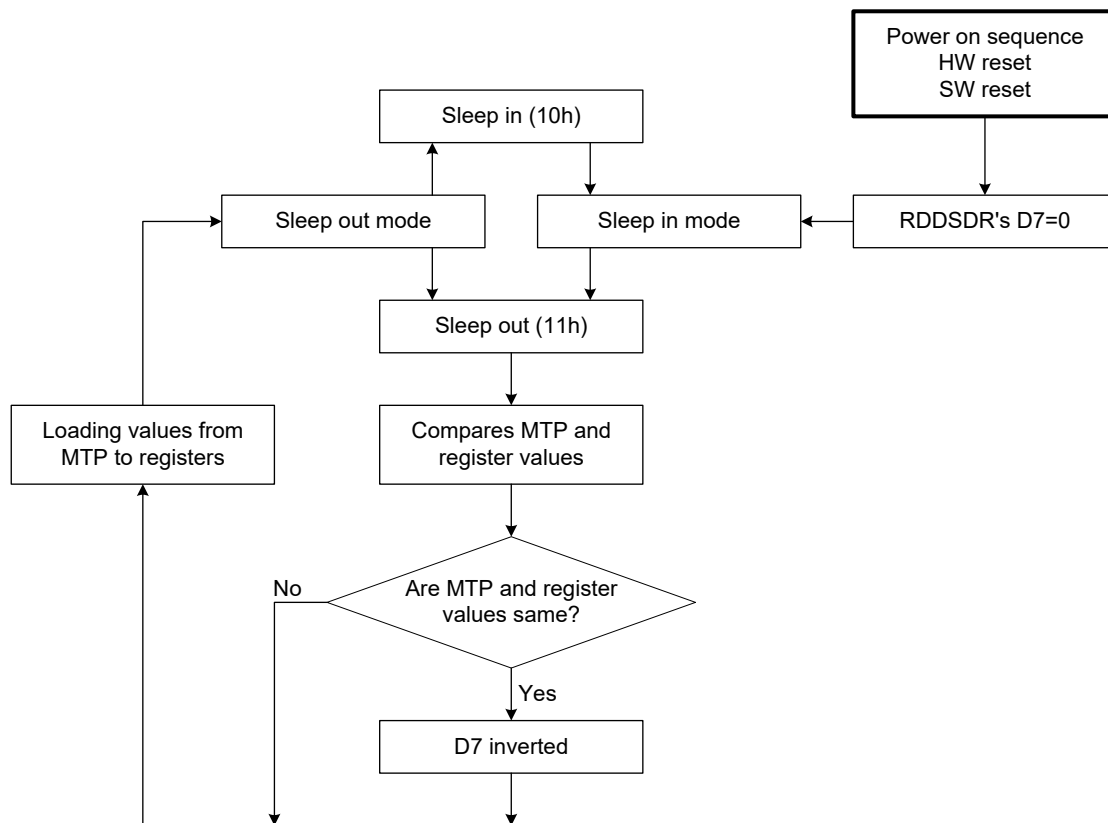
9.19 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

9.19.1 Register Loading Detection

Sleep Out-command (See section “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from MTP (or similar device) to registers of the display controller is working properly.

There are compared factory values of the MTP and register values of the display controller by the display controller. If those both values (MTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:

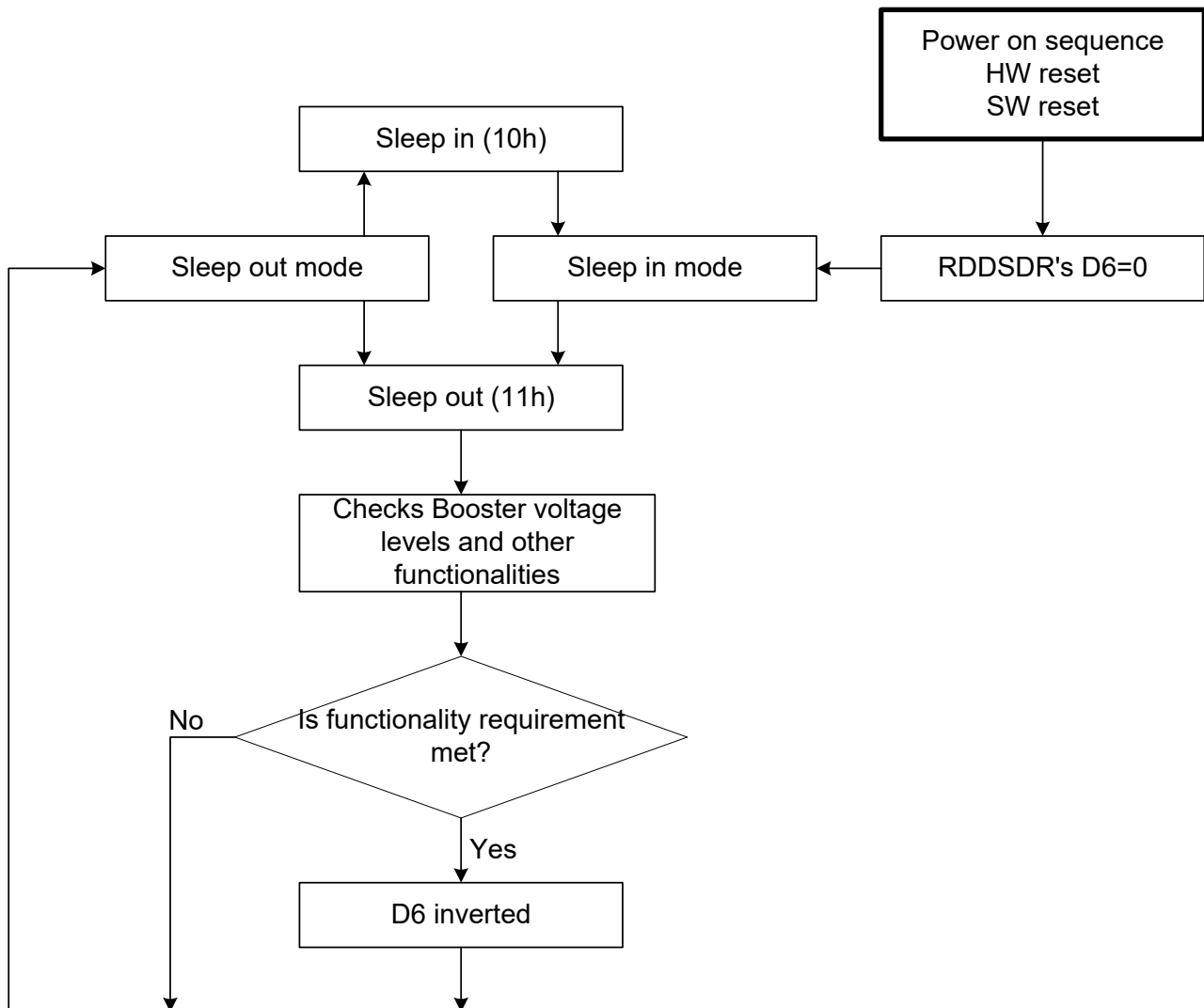


Note: There is not compared and loaded register values, which can be changed by user (00h to Afh and Dah to DDh), by the display module.

9.19.2 Functionality Detection

Sleep Out-command (See section “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is following:



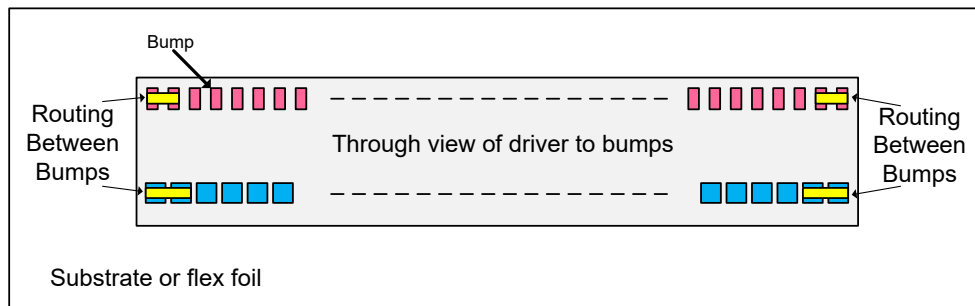
Note: There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

9.19.3 Chip Attachment Detection (Optional)

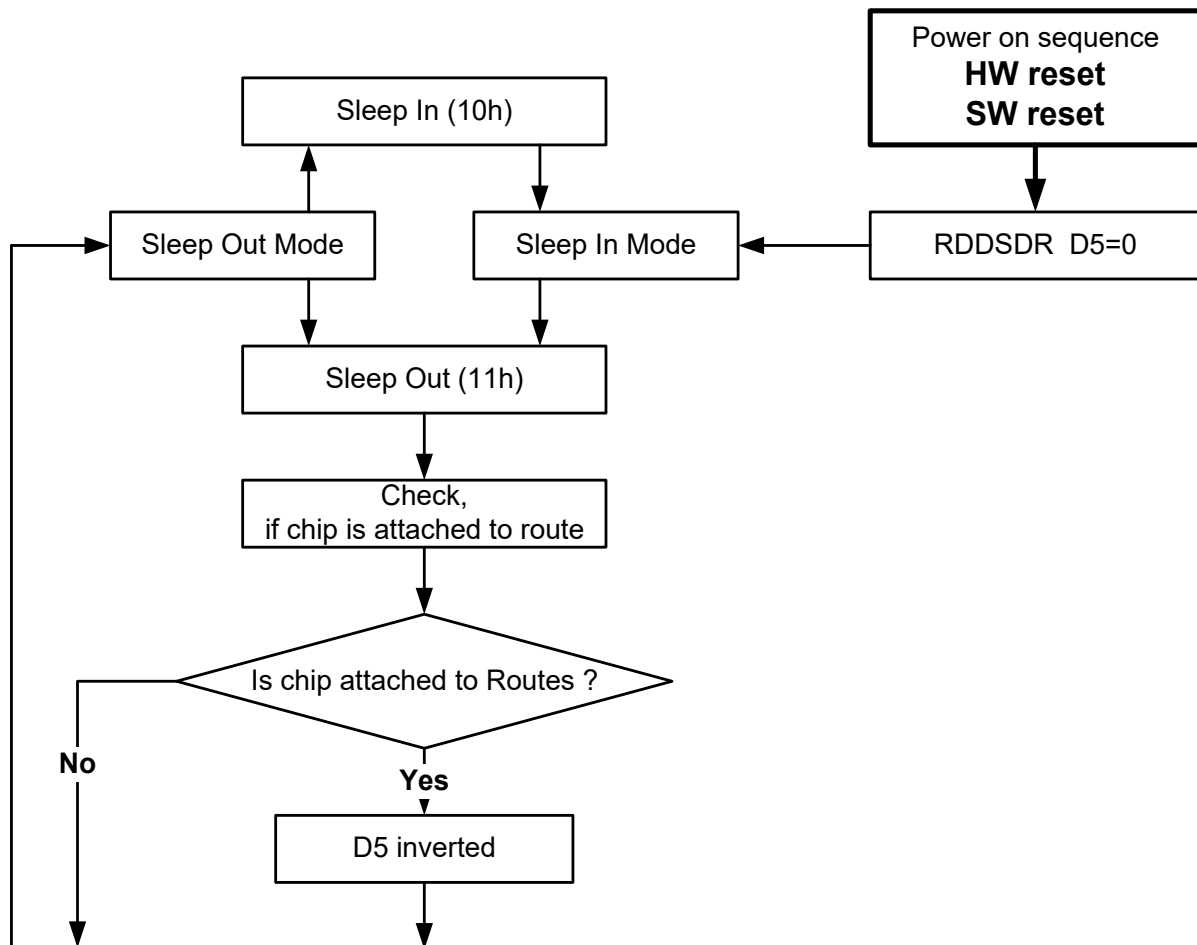
Sleep Out-command (See section “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= increased by 1).

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:

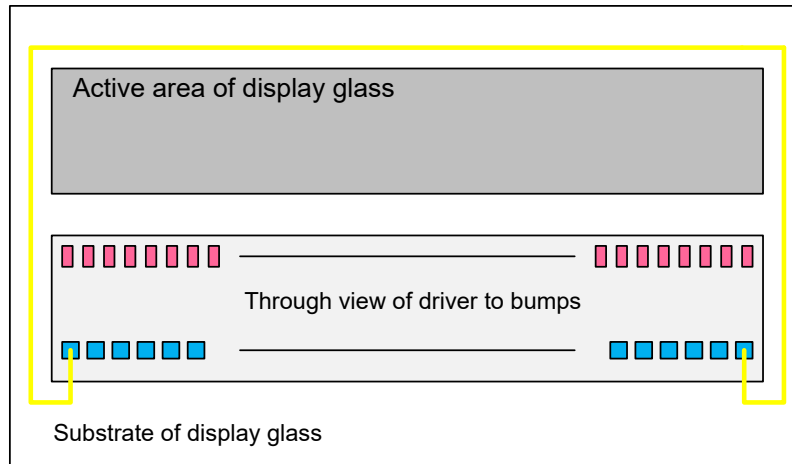


9.19.4 Display Glass Break Detection (Optional)

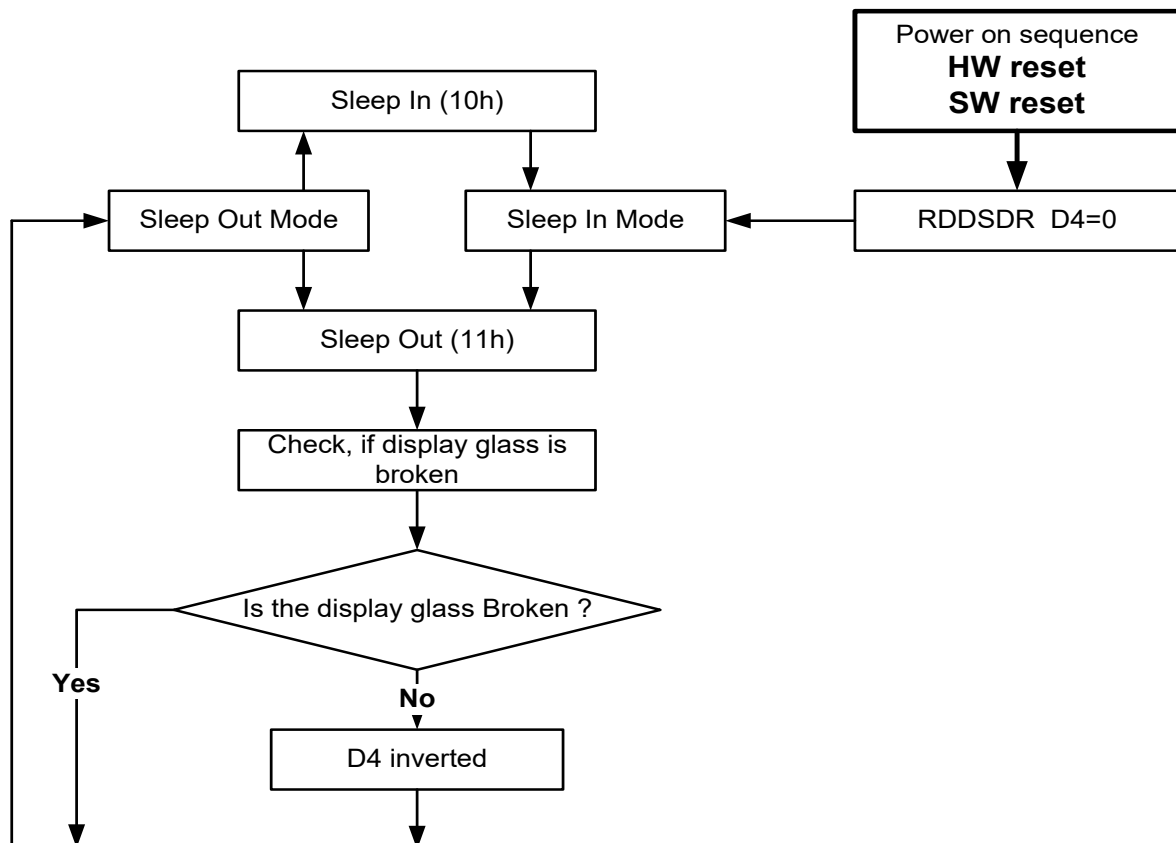
Sleep Out-command (See section “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display glass of the display module is broken or not.

There is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D4), if the display glass is not broken. If this display glass is broken, this bit (D4) is not inverted (= increased by 1).

The following figure is a reference, how this glass break detection can be implemented e.g. there is connected together 2 bumps via route of ITO. This route of ITO is the nearest route of the edge of the display glass.



The flow chart for this internal function is following:



10 COMMAND

10.1 System Function Command List and Description

Table 15 System Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	10.1.1	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	10.1.2	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software Reset
RDDID	10.1.3	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 Read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 Read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 Read
RDDST	10.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
		1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	10.1.5	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	-	-		-
RDD MADCTL	10.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display MADCTL
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	-	-		-
RDD COLMOD	10.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel Format
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0		-
RDDIM	10.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	VSSON	D6	INVON	-	-	GCS2	GCS1	GCS0		-
RDDSM	10.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal Mode
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	TEON	TEM	-	-	-	-	-	-		-
RDDSDR	10.1.10	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read Display Self-diagnostic
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	RELD	FUND	ATTD	BRD	-	-	-	-		-

“-”: Don't care

Table 16 System Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SLPIN	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep In & Booster Off
SLPOUT	10.1.12	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep Out & Booster On
PTLON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial Mode On
NORON	10.1.14	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial Off (Normal)
INVOFF	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display Inversion Off (Normal)
INVON	10.1.16	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display Inversion On
GAMSET	10.1.17	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma Curve Select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display Off
DISPON	10.1.19	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display On
CASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column Address Set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X Address Start: $0 \leq XS \leq X$
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X Address End: $S \leq XE \leq X$
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	10.1.21	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row Address Set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y Address Start: $0 \leq YS \leq Y$
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y Address End: $S \leq YE \leq Y$
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	10.1.22	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory Write Write Data
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		
RGBSET	10.1.23	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)	LUT for 4k,65k,262k Color display
		1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000		Red Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Ra5	Ra4	Ra3	Ra2	Ra1	Ra0		Red Tone "a"
		1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000		Green Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Gb5	Gb4	Gb3	Gb2	Gb1	Gb0		Green Tone "b"
		1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000		Blue Tone 0
		1	↑	1	-	-	-	:	:	:	:	:	:		:
		1	↑	1	-	-	-	Bc5	Bc4	Bc3	Bc2	Bc1	Bc0		Blue Tone "c"

"-": Don't care

Table 17 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PTLAR	10.1.25	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial Start/End Address Set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial Start Address (0,1,2, ..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		Partial End Address (0,1,2, ..., P)
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial End Address (0,1,2, ..., P)
SCRLAR	10.1.26	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Scroll area set
		1	↑	1	-	-	-	-	-	-	-	-	-		Top fixed area (0,1, 2, ..., 161)
		1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		Vertical scroll area (0,1, 2, ..., 161)
		1	↑	1	-	-	-	-	-	-	-	-	-		Vertical scroll area (0,1, 2, ..., 161)
		1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		Bottom fixed area (0,1, 2, ..., 161)
		1	↑	1	-	-	-	-	-	-	-	-	-		Bottom fixed area (0,1, 2, ..., 161)
TEOFF	10.1.27	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.28	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing Effect Mode Set & on
		1	↑	1	-	-	-	-	-	-	-	-	TEM		Mode1: TEM="0" Mode2: TEM="1"
MADCTL	10.1.29	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory Data Access Control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-		-
VSCSAD	10.1.30	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Scroll Start Address of RAM
		1	1	1	-	-	-	-	-	-	-	-	-		SSA=0,1,2,...,161
		1	1	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
IDMOFF	10.1.31	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle Mode Off
IDMON	10.1.32	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle Mode On
COLMOD	10.1.33	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface Pixel Format
		1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0		Interface Format
RDID1	10.1.34	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read Parameter
RDID2	10.1.35	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read Parameter
RDID3	10.1.36	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read Parameter

“-”: Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

10.1.1 NOP (00h)

00H	NOP (No Operation)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												-
Description	This command is empty command.												

“-“ Don't care

10.1.2 SWRESET (01h): Software Reset

01H	SWRESET (Software Reset)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)
Parameter	No Parameter												-
Description	“-“ Don't care -If Software Reset is applied during Sleep In mode, it will be necessary to wait 120msec before sending next command. -The display module loads all default values to the registers during 120msec. -If Software Reset is applied during Sleep Out or Display On Mode, it will be necessary to wait 120msec before sending next command.												
Flow Chart	SWRESET ↓ Display whole blank screen ↓ Set Commands to S/W Default Value ↓ Sleep In Mode Legend Command Parameter Display Action Mode Sequential transter												

10.1.3 RDDID (04h): Read Display ID

04H	RDDID (Read Display ID)																															
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)																			
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																			
2 nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10																				
3 rd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20																				
4 th Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30																				
Description	-This read byte returns 24-bit display identification information. -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. -The 3rd parameter (ID27 to ID20): LCD module/driver version ID -The 4th parameter (ID37 to UD30): LCD module/driver ID. -Commands RDID1/2/3(Dah, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively. -“ Don't care																															
Default	<table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr><tr><td>Power On Sequence</td><td>NV Value</td><td>NV Value</td><td>NV Value</td></tr><tr><td>S/W Reset</td><td>NV Value</td><td>NV Value</td><td>NV Value</td></tr><tr><td>H/W Reset</td><td>NV Value</td><td>NV Value</td><td>NV Value</td></tr></table>													Status	Default Value			ID1	ID2	ID3	Power On Sequence	NV Value	NV Value	NV Value	S/W Reset	NV Value	NV Value	NV Value	H/W Reset	NV Value	NV Value	NV Value
Status	Default Value																															
	ID1	ID2	ID3																													
Power On Sequence	NV Value	NV Value	NV Value																													
S/W Reset	NV Value	NV Value	NV Value																													
H/W Reset	NV Value	NV Value	NV Value																													
Flow Chart	Serial I/F Mode Read 04h Dummy Clock Send 2nd parameter Send 3rd parameter Send 4th parameter Parallel I/F Mode Read 04h Dummy Read Send 2nd parameter Send 3rd parameter Send 4th parameter Host Display Legend Command Parameter Display Action Mode Sequential transter																															

10.1.4 RDDST (09h): Read Display Status

09H	RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd Parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	
3 rd Parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	
4 th Parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	
5 th Parameter	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0	
Description	This command indicates the current status of the display as described in the table below:												
	Bit	Description	Value										
	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off										
	MY	Row Address Order (MY)	'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')										
	MX	Column Address Order (MX)	'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')										
	MV	Row/Column Exchange (MV)	'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')										
	ML	Scan Address Order (ML)	'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1' =Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')										
	RGB	RGB/ BGR Order (RGB)	'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')										
	MH	Horizontal Order	'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')										
	ST24	For Future Use	'0'										
	ST23	For Future Use	'0'										
	IFPF2	Interface Color Pixel Format Definition	"011" = 12-bit / pixel, "101" = 16-bit / pixel, "110" = 18-bit / pixel, others are no define										
	IFPF1												
	IFPF0												
	IDMON	Idle Mode On/Off	'1' = On, "0" = Off										
	PTLON	Partial Mode	'1' = On, "0" = Off										
	SLPOUT	Sleep In/Out	'1' = Out, "0" = In										
	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display										
	ST15	Vertical Scrolling	'1' = Scroll on,"0" = Scroll off										
	ST14	Horizontal Scroll	'0'										
	INVON	Inversion Status	'1' = On, "0" = Off										
	ST12	All Pixels On (Not	'0'										
	ST11	All Pixels Off (Not	'0'										
	DISON	Display On/Off	'1' = On, "0" = Off										
	TEON	Tearing effect line	'1' = On, "0" = Off										
	GCS2	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" to "111" = Not defined										
	GCS1												
	GCS0												

	<table><tr><td>TEM</td><td>Tearing effect line</td><td colspan="3">'0' = mode1, '1' = mode2</td></tr><tr><td>ST4</td><td>For Future Use</td><td colspan="3">'0'</td></tr><tr><td>ST3</td><td>For Future Use</td><td colspan="3">'0'</td></tr><tr><td>ST2</td><td>For Future Use</td><td colspan="3">'0'</td></tr><tr><td>ST1</td><td>For Future Use</td><td colspan="3">'0'</td></tr><tr><td>ST0</td><td>For Future Use</td><td colspan="3">'0'</td></tr></table>	TEM	Tearing effect line	'0' = mode1, '1' = mode2			ST4	For Future Use	'0'			ST3	For Future Use	'0'			ST2	For Future Use	'0'			ST1	For Future Use	'0'			ST0	For Future Use	'0'		
TEM	Tearing effect line	'0' = mode1, '1' = mode2																													
ST4	For Future Use	'0'																													
ST3	For Future Use	'0'																													
ST2	For Future Use	'0'																													
ST1	For Future Use	'0'																													
ST0	For Future Use	'0'																													
	“ - “ Don't care																														
Default	<table><tr><th rowspan="2">Status</th><th colspan="4">Default Value (ST31 to ST0)</th></tr><tr><th>ST[31-24]</th><th>ST[23-16]</th><th>ST[15-8]</th><th>ST[7-0]</th></tr><tr><td>Power On Sequence</td><td>0000-0000</td><td>0110-0001</td><td>0000-0000</td><td>0000-0000</td></tr><tr><td>S/W Reset</td><td>0xxx0xx00</td><td>0xxx-0001</td><td>0000-0000</td><td>0000-0000</td></tr><tr><td>H/W Reset</td><td>0000-0000</td><td>0110-0001</td><td>0000-0000</td><td>0000-0000</td></tr></table>	Status	Default Value (ST31 to ST0)				ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]	Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000	S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000	H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000						
Status	Default Value (ST31 to ST0)																														
	ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]																											
Power On Sequence	0000-0000	0110-0001	0000-0000	0000-0000																											
S/W Reset	0xxx0xx00	0xxx-0001	0000-0000	0000-0000																											
H/W Reset	0000-0000	0110-0001	0000-0000	0000-0000																											
Flow Chart	Serial I/F Mode RDDST 09h Dummy Clock Send 2nd parameter Send 3rd parameter Send 4th parameter Send 5th parameter Parallel I/F Mode RDDST 09h Dummy Read Send 2nd parameter Send 3rd parameter Send 4th parameter Sendth parameter Legend Command Parameter Display Action Mode Sequential transter																														

10.1.5 RDDPM (0Ah): Read Display Power Mode

0AH	RDDPM (Read Display Power Mode)																																							
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)																											
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																											
2 nd Parameter	1	1	↑		BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	D1	D0																												
Description	This command indicates the current status of the display as described in the table below: “-“ Don't care																																							
	<table><tr><th>Bit</th><th>Description</th><th>Value</th></tr><tr><td>BSTON</td><td>Booster Voltage Status</td><td>'1' =Booster on, '0' =Booster off</td></tr><tr><td>IDMON</td><td>Idle Mode On/Off</td><td>'1' = Idle Mode On, '0' = Idle Mode Off</td></tr><tr><td>PTLON</td><td>Partial Mode On/Off</td><td>'1' = Partial Mode On, '0' = Partial Mode Off</td></tr><tr><td>SLPON</td><td>Sleep In/Out</td><td>'1' = Sleep Out, '0' = Sleep In</td></tr><tr><td>NORON</td><td>Display Normal Mode On/Off</td><td>'1' = Normal Display, '0' = Partial Display</td></tr><tr><td>DISON</td><td>Display On/Off</td><td>'1' = Display On, '0' = Display Off</td></tr><tr><td>D1</td><td>Not Used</td><td>'0'</td></tr><tr><td>D0</td><td>Not Used</td><td>'0'</td></tr></table>													Bit	Description	Value	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display	DISON	Display On/Off	'1' = Display On, '0' = Display Off	D1	Not Used	'0'	D0	Not Used	'0'
	Bit	Description	Value																																					
	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off																																					
	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off																																					
	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off																																					
	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In																																					
	NORON	Display Normal Mode On/Off	'1' = Normal Display, '0' = Partial Display																																					
	DISON	Display On/Off	'1' = Display On, '0' = Display Off																																					
	D1	Not Used	'0'																																					
D0	Not Used	'0'																																						
Default	<table><tr><th>Status</th><th>Default Value (D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>0000_1000(08h)</td></tr><tr><td>S/W Reset</td><td>0000_1000(08h)</td></tr><tr><td>H/W Reset</td><td>0000_1000(08h)</td></tr></table>													Status	Default Value (D7 to D0)	Power On Sequence	0000_1000(08h)	S/W Reset	0000_1000(08h)	H/W Reset	0000_1000(08h)																			
	Status	Default Value (D7 to D0)																																						
	Power On Sequence	0000_1000(08h)																																						
	S/W Reset	0000_1000(08h)																																						
	H/W Reset	0000_1000(08h)																																						
Flow Chart	Serial I/F Mode RDDPM 0Ah Send 2nd parameter Parallel I/F Mode RDDPM 0Ah Dummy Read Send 2nd parameter Legend Command Parameter Display Action Mode Sequential transfer																																							

10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd Parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0	
Description	This command indicates the current status of the display as described in the table below: “- “ Don't care												
	Bit	Description					Value						
	MX	Column Address Order					'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')						
	MY	Row Address Order					'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')						
	MV	Row/Column Order (MV)					'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)						
	ML	Vertical Refresh Order					'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom						
	RGB	RGB/BGR Order					'1' =BGR, "0"=RGB						
	MH	Horizontal Refresh Order					LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left						
	D1	Not Used					'0'						
	D0	Not Used					'0'						
Default													
	Status					Default Value (D7 to D0)							
	Power On Sequence					0000_0000 (00h)							
	S/W Reset					No change							
H/W Reset					0000_0000 (00h)								
Flow Chart													
	Serial I/F Mode RDDMADCTL 0Bh ↓ Send 2nd parameter Parallel I/F Mode RDDMADCTL 0Bh ↓ Dummy Read ↓ Send 2nd parameter Legend Command Parameter Display Action Mode Sequential transfer												

10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

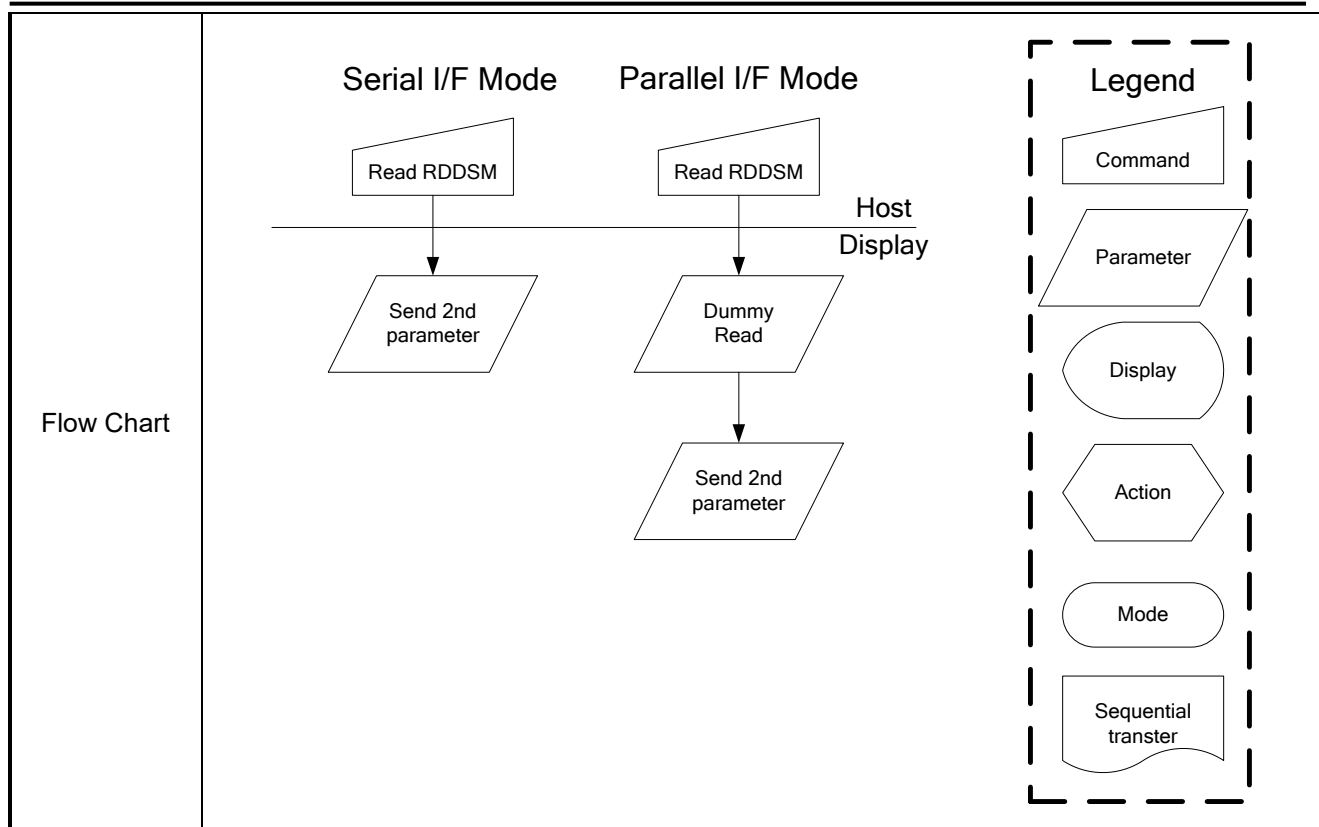
0CH	RDDCOLMOD (Read Display Pixel Format)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd Parameter	1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0	
Description	This command indicates the current status of the display as described in the table below:												
	IFPF[2:0]			MCU Interface Color Format									
	011			12-bit/pixel									
	101			16-bit/pixel									
	110			18-bit/pixel									
	111			No used									
Others are no define and invalid “-“ Don't care													
Default													
	Status			Default Value									
				IFPF[2:0]									
	Power On Sequence			0110 (18 bits/pixel)									
	S/W Reset			No Change									
	H/W Reset			0110 (18 bits/pixel)									
Flow Chart													

10.1.8 RDDIM (0Dh): Read Display Image Mode

0DH	RDDIM (0Dh): Read Display Image Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd Parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0	
Description	This command indicates the current status of the display as described in the table below: “-“ Don't care												
	Bit	Description					Value						
	VSSON	Reversed					“0”						
	D6	Reversed					“0”						
	INVON	Inversion On/Off					“1” = Inversion is On, “0” = Inversion is Off						
	D4	All Pixels On					“0” (Not used)						
	D3	All Pixels Off					“0” (Not used)						
	GCS2 GCS1 GCS0	Gamma Curve Selection					“000” = GC0, “001” = GC1, “010” = GC2, “011” = GC3, “100” to “111” = Not defined						
Default													
	Status					Default Value(D7 to D0)							
	Power On Sequence					0000_0000 (00h)							
	S/W Reset					0000_0000 (00h)							
	H/W Reset					0000_0000 (00h)							
Flow Chart													
	Serial I/F Mode RDDIM 0Dh ↓ Send 2nd parameter Parallel I/F Mode RDDIM 0Dh ↓ Dummy Read ↓ Send 2nd parameter Host Display Legend Command Parameter Display Action Mode Sequential transfer												

10.1.9 RDDSM (0Eh): Read Display Signal Mode

0EH	RDDSM (0Eh): Read Display Signal Mode												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd Parameter	1	1	↑	-	TEON	TEM	D5	D4	D3	D2	D1	D0	
Description	This command indicates the current status of the display as described in the table below: - “ Don't care												
	Bit		Description					Value					
	TEON		Tearing Effect Line On/Off					“1” = On, “0” = Off					
	TEM		Tearing effect line mode					“1” = Mode2, “0” = Mode1					
	D5		Not Used					“1” = On, “0” = Off					
	D4		Not Used					“1” = On, “0” = Off					
	D3		Not Used					“1” = On, “0” = Off					
	D2		Not Used					“1” = On, “0” = Off					
	D1		Not Used					“1” = On, “0” = Off					
	D0		Not Used					“1” = On, “0” = Off					
Default													
	Status					Default Value(D7~D0)							
	Power On Sequence					0000_0000 (00h)							
	S/W Reset					0000_0000 (00h)							
	H/W Reset					0000_0000 (00h)							



10.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

0FH	RDDSDR (0Fh): Read Display Self-Diagnostic Result												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2 nd Parameter	1	1	↑	-	RELD	FUND	ATTD	BRD	D3	D2	D1	D0	
Description	This command indicates the current status of the display as described in the table below: “-“ Don't care												
	Bit	Description							Value				
	RELD	Register Loading Detection							See Section 9.19.1				
	FUND	Functionality Detection							See Section 9.19.2				
	ATTD	Chip Attachment Detection							See Section 9.19.3				
	BRD	Display Glass Break Detection							See Section 9.19.4				
	D3	Not Used							“0”				
	D2	Not Used							“0”				
	D1	Not Used							“0”				
	D0	Not Used							“0”				
Default													
	Status							Default Value(D7~D0)					
	Power On Sequence							0000_0000 (00h)					
	S/W Reset							0000_0000 (00h)					
	H/W Reset							0000_0000 (00h)					
Flow Chart													
	Serial I/F Mode Read RDDSDR Send 2nd parameter Parallel I/F Mode Read RDDSDR Dummy Read Send 2nd parameter Host Display Legend Command Parameter Display Action Mode Sequential transter												

10.1.11 SLPIN (10h): Sleep In

10H	SLPIN (Sleep In)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)								
Parameter	No Parameter												-								
Description	-This command causes the LCD module to enter the minimum power consumption mode. -In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.																				
Restriction	-This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). -When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep in Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep in Mode
Status	Default Value																				
Power On Sequence	Sleep In Mode																				
S/W Reset	Sleep In Mode																				
H/W Reset	Sleep in Mode																				
Flow Chart	SLPIN Display whole blank screen (Automatic No effect to DISP ON/OFF Commands) Drain Charge From LCD Panel Stop DC-DC Converter Stop Internal Oscillator Sleep In Mode Legend Command Parameter Display Action Mode Sequential transfer																				

10.1.12 SLPOUT (11h): Sleep Out

11H	SLPOUT (Sleep Out)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)								
Parameter	No Parameter												-								
Description	-This command turns off sleep mode. -In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.																				
Restriction	-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). -When IC is in Sleep In mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits. -When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command due to the download of default value of registers and the execution of self-diagnostic function.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep in Mode</td></tr></table>													Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep in Mode
Status	Default Value																				
Power On Sequence	Sleep In Mode																				
S/W Reset	Sleep In Mode																				
H/W Reset	Sleep in Mode																				
Flow Chart	SLPOUT Start Internal Oscillator Start up DC:DC Converter Charge Offset voltage for LCD Panel Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands) Display Memory contents In accordance with the current command table settings Sleep Out mode Legend Command Parameter Display Action Mode Sequential transter																				

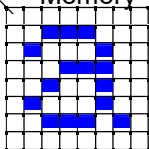
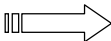
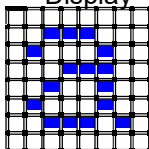
10.1.13 PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)
Parameter	No Parameter												-
Description	-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h) -To leave Partial mode, the Normal Display Mode On command (13h) should be written. “-“ Don't care												
Default	Status						Default Value						
	Power On Sequence						Normal Mode On						
	S/W Reset						Normal Mode On						
	H/W Reset						Normal Mode On						
Flow Chart	See Partial Area (30h)												

10.1.14 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)								
Parameter	No Parameter												-								
Description	-This command returns the display to normal mode. -Normal display mode on means Partial mode off. -Exit from NORON by the Partial mode On command (12h) “-“ Don't care																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></table>													Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On
Status	Default Value																				
Power On Sequence	Normal Mode On																				
S/W Reset	Normal Mode On																				
H/W Reset	Normal Mode On																				
Flow Chart	See Partial Area Definition Descriptions for details of when to use this command																				

10.1.15 INVOFF (20h): Display Inversion Off

20H	IVNOFF (Normal Display Mode Off)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)								
Parameter	No Parameter												-								
Description	-This command is used to recover from display inversion mode. “-” Don't care (Example) Top-Left Memory   Display 																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>S/W Reset</td><td>Display Inversion off</td></tr><tr><td>H/W Reset</td><td>Display Inversion off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value																				
Power On Sequence	Display Inversion off																				
S/W Reset	Display Inversion off																				
H/W Reset	Display Inversion off																				
Flow Chart	Display Inversion On Mode ↓ INVOFF (20h) ↓ Display Inversion OFF Mode Legend Command Parameter Display Action Mode Sequential transter																				

10.1.16 INVON (21h): Display Inversion On

21H	IVNOFF (Display Inversion On)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)								
Parameter	No Parameter												-								
Description	-This command is used to enter into display inversion mode -To exit from Display Inversion On, the Display Inversion Off command (20h) should be written. “-“ Don't care (Example) Top-Left (0,0) Memory Display																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion off</td></tr><tr><td>S/W Reset</td><td>Display Inversion off</td></tr><tr><td>H/W Reset</td><td>Display Inversion off</td></tr></table>													Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value																				
Power On Sequence	Display Inversion off																				
S/W Reset	Display Inversion off																				
H/W Reset	Display Inversion off																				
Flow Chart	Display Inversion OFF Mode ↓ INVON (21h) ↓ Display Inversion ON Mode Legend Command Parameter Display Action Mode Sequential transter																				

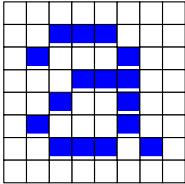
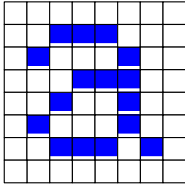
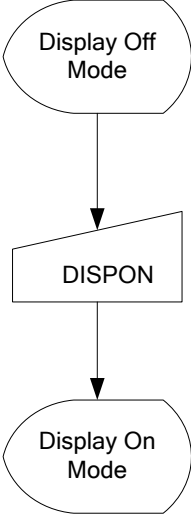
10.1.17 GAMSET (26h): Gamma Set

26H	GAMSET (Gamma Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)
Parameter	1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0	
Description	-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.												
	GC [7:0]		Parameter	Curve Selected									
				GS=1					GS=0				
	01h		GC0	Gamma Curve 1 (G2.2)					Gamma Curve 1 (G1.0)				
	02h		GC1	Gamma Curve 2 (G1.8)					Gamma Curve 2 (G2.5)				
	04h		GC2	Gamma Curve 3 (G2.5)					Gamma Curve 3 (G2.2)				
	08h		GC3	Gamma Curve 4 (G1.0)					Gamma Curve 4 (G1.8)				
Note: All other values are undefined.													
Default	Status					Default Value							
	Power On Sequence					01h							
	S/W Reset					01h							
	H/W Reset					01h							
Flow Chart	GAMSET (26h) ↓ 1st parameter: GC[7:0] ↓ New Gamma Curve Loaded												
	Legend Command Parameter Display Action Mode Sequential transter												

10.1.18 DISPOFF (28h): Display Off

28H	DISPOFF (Display Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)
Parameter	No Parameter												-
Description	</												

10.1.19 DISPON (29h): Display On

29H	DISPON (Display On)																			
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)							
Parameter	No Parameter												-							
Description	- This command is used to recover from DISPLAY OFF mode. - Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. (Example) Memory  → Display 																			
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display off</td></tr> <tr> <td>S/W Reset</td><td>Display off</td></tr> <tr> <td>H/W Reset</td><td>Display off</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																			
Power On Sequence	Display off																			
S/W Reset	Display off																			
H/W Reset	Display off																			
Flow Chart	 <pre> graph TD A([Display Off Mode]) --> B[/DISPON/] B --> C([Display On Mode]) </pre> Legend Command Parameter Display Action Mode Sequential transfer																			

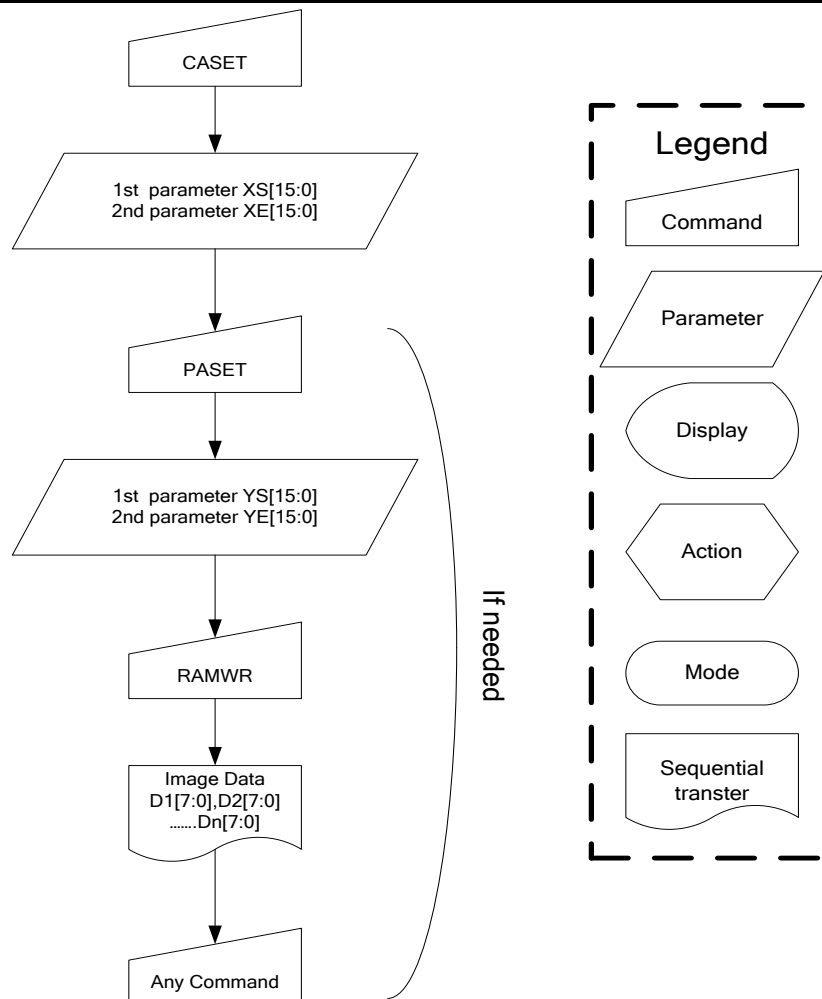
10.1.20 CASET (2Ah): Column Address Set

2AH	CASET(Column Address Set)_												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET(2Ah)	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)
1 st Parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	
2 nd Parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
3 rd Parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
4 th Parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
Description	-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes. -Each value represents one column line in the Frame Memory.												
Restriction	XS [15:0] always must be equal to or less than XE [15:0] When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored. 1. 128X160 memory base (GM = '11') (Parameter range: 0 < XS [15:0] < XE [15:0] < 127 (007Fh)): MV="0" (Parameter range: 0 < XS [15:0] < XE [15:0] < 159 (009Fh)): MV="1" 1. 132X132 memory base (GM = '01') (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV="0" (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV="1" 1. 132X162 memory base (GM = '00') (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV="0" (Parameter range: 0 < XS [15:0] < XE [15:0] < 161 (00A1h)): MV="1"												

Default

GM Status	Status	Default Value		
		XS [7:0]	XE [7:0] (MV='0')	XE [7:0] (MV='1')
GM='11' (128x160 Memory Base)	Power On Sequence	0000h	007Fh (127)	
	S/W Reset	0000h	007Fh (127)	009Fh (159)
	H/W Reset	0000h	007Fh (127)	
GM='01' (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
	S/W Reset	0000h	0083h (131)	0083h (131)
	H/W Reset	0000h	0083h (131)	
GM='00' (132x162 Memory Base)	Power On Sequence	0000h	0083h (131)	
	S/W Reset	0000h	0083h (131)	00A1h (161)
	H/W Reset	0000h	0083h (131)	

Flow Chart



10.1.21 RASET (2Bh): Row Address Set

2BH	RASET (Row Address Set)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RASET (2Bh)	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)
1 st Parameter	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	
2 nd Parameter	1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
3 rd Parameter	1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
4 th Parameter	1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
Description	The value of YS [7:0] and YE [7:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.												
	YS[7:0] → YE[7:0] →												
Restriction	YS [15:0] always must be equal to or less than YE [15:0] When YS [15:0] or YE [15:0] are greater than maximum row address like below, data of out of range will be ignored. 1. 128X160 memory base (GM = '11') (Parameter range: 0 < YS [15:0] < YE [15:0] < 159 (009Fh)): MV="0" (Parameter range: 0 < YS [15:0] < YE [15:0] < 127 (007Fh)): MV="1" 1. 132X132 memory base (GM = '00') (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (00A1h)): MV="0" (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1" 1. 132X162 memory base (GM = '00') (Parameter range: 0 < YS [15:0] < YE [15:0] < 161 (00A1h)): MV="0" (Parameter range: 0 < YS [15:0] < YE [15:0] < 131 (0083h)): MV="1"												

Default	GM status	Status	Default Value		
			YS [15:0]	YE [15:0] (MV='0 ')	YE [15:0] (MV='1')
	GM='11' (128x160 memory base)	Power On Sequence	0000h	009Fh (159)	
		S/W Reset	0000h	009Fh (159)	007Fh (127)
		H/W Reset	0000h	009Fh (159)	
	GM='01' (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
		S/W Reset	0000h	0083h (131)	0083h (131)
		H/W Reset	0000h	0083h (131)	
	GM='00' (132x162 memory base)	Power On Sequence	0000h	00A1h (161)	
		S/W Reset	0000h	00A1h (161)	0083h (131)
H/W Reset		0000h	00A1h (161)		

Flow Chart	CASET 1st parameter XS[15:0] 2nd parameter XE[15:0] PASET 1st parameter YS[15:0] 2nd parameter YE[15:0] RAMWR Image Data D1[7:0],D2[7:0]Dn[7:0] Any Command If needed If needed Legend Command Parameter Display Action Mode Sequential transfer
------------	--

10.1.22 RAMWR (2Ch): Memory Write

2CH	RAMWR (Memory Write)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)								
1 st Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0									
	1	↑	1																		
Nth Parameter	1	↑	1	D17-8	D7	D6	D5	D4	D3	D2	D1	D0									
Description	In all color modes, there is no restriction on length of parameters. 1. 128X160 memory base (GM = '11') 128x160x18-bit memory can be written by this command Memory range: (0000h, 0000h) -> (007Fh, 09Fh) 1. 132x132 memory base (GM = '01') 132x132x18-bit memory can be written on this command. Memory range: (0000h, 0000h) -> (0083h, 0083h) 1. 132x162 memory base (GM = '00') 132x162x18-bit memory can be written on this command. Memory range: (0000h, 0000h) -> (0083h, 00A1h)																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared
Status	Default Value																				
Power On Sequence	Contents of memory is set randomly																				
S/W Reset	Contents of memory is not cleared																				
H/W Reset	Contents of memory is not cleared																				
Flow Chart	RAMWR ↓ Image Data D1[7:0],D2[7:0]Dn[7:0] ↓ Any Command Legend Command Parameter Display Action Mode Sequential transter																				

10.1.23 RGBSET (2Dh): Color Setting for 4K, 65K and 262K

2DH	RGBSET (Color Set for 4K, 65K, 262K and 16.7M)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGBSET	0	↑	1	-	0	0	1	0	1	1	0	1	(2Dh)
1 st Parameter	1	↑	1	-	-	-	R005	R004	R003	R002	R001	R000	
	1	↑	1	-	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	
	1	↑	1	-	-	-	R315	R314	R313	R312	R311	R310	
	1	↑	1	-	-	-	G005	G004	G003	G002	G001	G000	
	1	↑	1	-	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	
	1	↑	1	-	-	-	G635	G634	G633	G632	G631	G630	
	1	↑	1	-	-	-	B005	B004	B003	B002	B001	B000	
	1	↑	1	-	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	
128 th Parameter	1	↑	1	-	-	-	B315	B314	B313	B312	B311	B310	
Description	This command is used to define the LUT for 12bits-to-16bits / 16-bit-to- 18bits color depth conversations. 128-Bytes must be written to the LUT regardless of the color mode. Only the values in Section 9.18 are referred. In this condition, 4K-color (4-4-4) and 65K-color(5-6-5) data input are transferred 6@-6(G)-6(B) through RGB LUT table. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to. Do not send any command before the last data is sent or LUT is not defined correctly.												
Default	Status						Default Value						
	Power On Sequence						Random						
	S/W Reset						Contents of the look-up table protected						
	H/W Reset						Random						
Flow Chart	RGBSET (2Dh) ↓ 1st parameter: 128th parameter: Legend Command Parameter Display Action Mode Sequential transfer												

10.1.24 RAMRD (2Eh): Memory Read

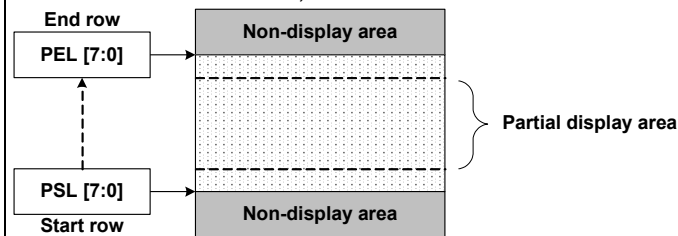
2EH	RAMHD (Memory Read)																				
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
RAMHD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)								
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-									
2 nd Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0									
	1	1	↑																		
(N+1)th Parameter	1	1	↑	D17-8	D7	D6	D5	D4	D3	D2	D1	D0									
Description	-This command is used to transfer data from frame memory to MCU. -When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. -The Start Column/Start Row positions are different in accordance with MADCTL setting. -Then D[17:0] is read back from the frame memory and the column register and the row register incremented as section 9.10 -Frame Read can be cancelled by sending any other command. -The data color coding is fixed to 18-bit in reading function. Please see section 9.8 “Data color coding” for color coding (18-bit cases), when there is used 8, 9, 16 and 18-bit data lines for image data. Note1: The Command 3Ah should be set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.																				
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	S/W Reset	Contents of memory is not cleared	H/W Reset	Contents of memory is not cleared
Status	Default Value																				
Power On Sequence	Contents of memory is set randomly																				
S/W Reset	Contents of memory is not cleared																				
H/W Reset	Contents of memory is not cleared																				
Flow Chart	RAMRD Dummy Image Data D1[7:0],D2[7:0]Dn[7:0] Any Command Legend Command Parameter Display Action Mode Sequential transfer																				

10.1.25 PTLAR (30h): Partial Area

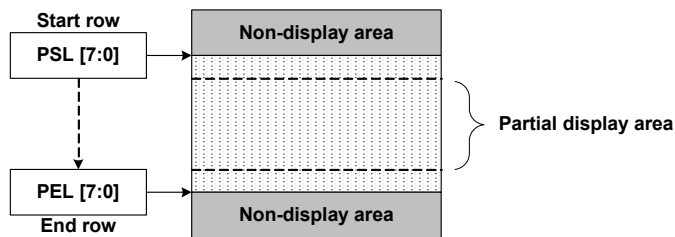
30H	PTLAR (Partial Area)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)
1 st Parameter	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	
2 nd Parameter	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
3 rd Parameter	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
4 th Parameter	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	

-This command defines the partial mode's display area.
 -There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

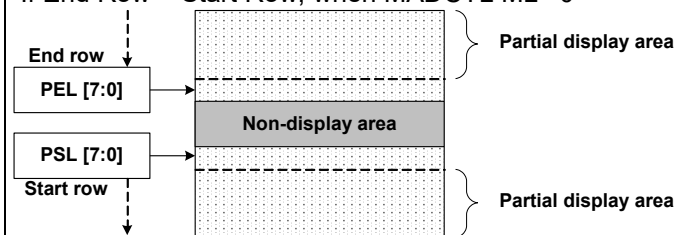
-If End Row > Start Row, when MADCTL ML='0'



-If End Row > Start Row, when MADCTL ML='1'



-If End Row < Start Row, when MADCTL ML='0'



-If End Row = Start Row then the Partial Area will be one row deep.

Default	Status	Default Value			
		PSL [15:0]	PEL [15:0]		
	GM[1:0]	"xx"	GM[1:0]="11"	GM[1:0]="01"	GM[1:0]="00"
	Power On Sequence	0000h	009Fh	0083h	00A1h
	S/W Reset	0000h	009Fh	0083h	00A1h
	H/W Reset	0000h	009Fh	0083h	00A1h

Flow Chart

2. Leave Partial Mode

```

graph TD
    subgraph "1. To Enter Partial Mode:"
        PLTAR[PLTAR] --> SR[SR[15:0]]
        SR --> ER[ER[15:0]]
        ER --> PTLON[PTLON]
        PTLON --> PM[Partial Mode]
    end

    subgraph "2. Leave Partial Mode"
        PM --> DISPOFF[DISPOFF]
        DISPOFF --> NORON[NORON]
        NORON --> PMOFF[Partial Mode OFF]
        PMOFF --> RAMRW[RAMRW]
        RAMRW --> ID[Image Data D1[7:0], D2[7:0] ..... Dn[7:0]]
        ID --> DISPON[DISPON]
    end

    DISPOFF -.-> Note["(Optional) To prevent Tearing Effect Image displayed"]
    
```

Legend

- Command
- Parameter
- Display
- Action
- Mode
- Sequential transfer

10.1.26 SCRLAR (33h): Scroll Area Set

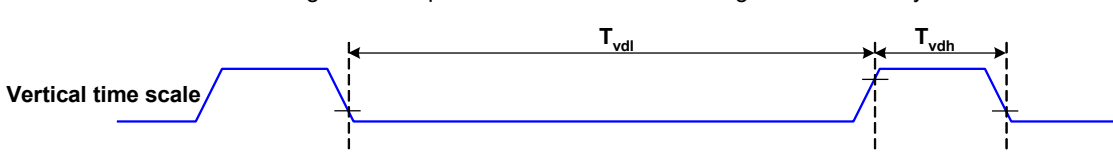
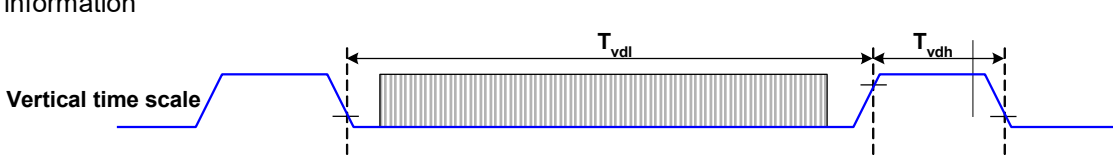
33H	SCRLAR (Scroll Area)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
SCRLAR	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)												
1 st parameter	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	-												
2 nd parameter	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	-												
3 rd parameter	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	-												
4 th parameter	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	-												
5 th parameter	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	-												
6 nd parameter	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	-												
Description	(0,0) TFA[15:0] VSA[15:0] BFA[15:0] Top Fixed Area Scroll Area Bottom Fixed Area -This command just defines the Vertical Scrolling Area of the display and not performs vertical scroll -When MADCTR B4=0 -The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display). -The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address) The first line appears immediately after the bottom most line of the Top Fixed Area. -The 4th & 5th parameter BFA [6:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer																								
Restriction	The condition is (TFA+VSA+BFA) = 162, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTR parameter MV should be set to '0'-this only affects the Frame Memory Write. TFA[15:0], VSA[15:0] and BFA[15:0] is based on line unit. TFA[15:0]= 0000h, 0001h, 0002h, 0003h, ... , 00A2h VSA[15:0]= 0000h, 0001h, 0002h, 0003h, ... , 00A2h BFA[15:0]= 0000h, 0001h, 0002h, 0003h, ... , 00A2h																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								

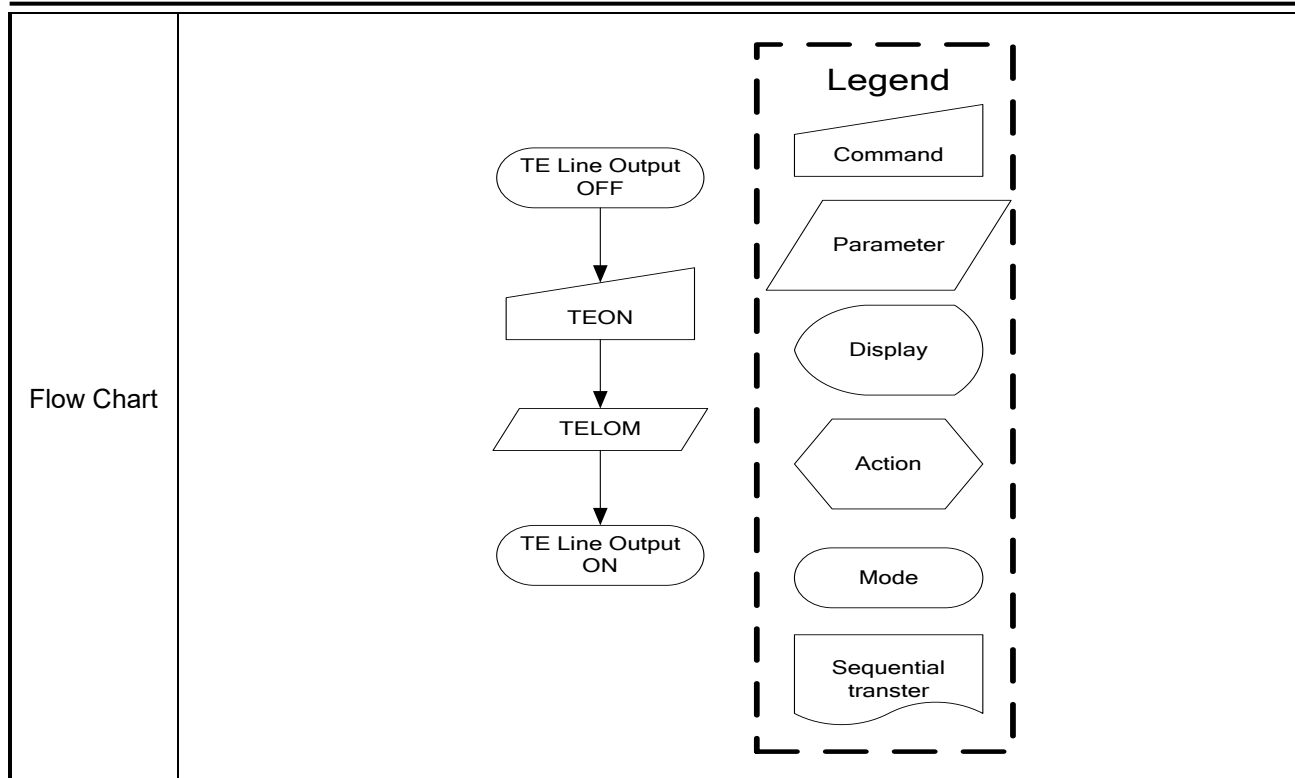
Default	<table><tr><th>Status</th><th colspan="3">Default Value GM[1:0]= "11"</th></tr><tr><td>Power On Sequence</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=00A0h</td><td>BFA[15:0]=0000h</td></tr><tr><td>S/W Reset</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=00A0h</td><td>BFA[15:0]=0000h</td></tr><tr><td>H/W Reset</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=00A0h</td><td>BFA[15:0]=0000h</td></tr><tr><th>Status</th><th colspan="3">Default Value GM[1:0]= "01"</th></tr><tr><td>Power On Sequence</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=0084h</td><td>BFA[15:0]=0000h</td></tr><tr><td>S/W Reset</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=0084h</td><td>BFA[15:0]=0000h</td></tr><tr><td>H/W Reset</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=0084h</td><td>BFA[15:0]=0000h</td></tr><tr><th>Status</th><th colspan="3">Default Value GM[1:0]= "00"</th></tr><tr><td>Power On Sequence</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=00A2h</td><td>BFA[15:0]=0000h</td></tr><tr><td>S/W Reset</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=00A2h</td><td>BFA[15:0]=0000h</td></tr><tr><td>H/W Reset</td><td>TFA[15:0]=0000h</td><td>VSA[15:0]=00A2h</td><td>BFA[15:0]=0000h</td></tr></table>	Status	Default Value GM[1:0]= "11"			Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h	S/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h	H/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h	Status	Default Value GM[1:0]= "01"			Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h	S/W Reset	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h	H/W Reset	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h	Status	Default Value GM[1:0]= "00"			Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h	S/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h	H/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h
	Status	Default Value GM[1:0]= "11"																																															
	Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h																																													
	S/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h																																													
	H/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A0h	BFA[15:0]=0000h																																													
	Status	Default Value GM[1:0]= "01"																																															
	Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h																																													
	S/W Reset	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h																																													
	H/W Reset	TFA[15:0]=0000h	VSA[15:0]=0084h	BFA[15:0]=0000h																																													
	Status	Default Value GM[1:0]= "00"																																															
	Power On Sequence	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h																																													
	S/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h																																													
H/W Reset	TFA[15:0]=0000h	VSA[15:0]=00A2h	BFA[15:0]=0000h																																														
1. TO Enter Vertical Scroll Mode: Normal Mode SCRLAR 1st parameter TFA[6:0] 2nd parameter VSA[6:0] 3rd parameter BFA[6:0] CASET 1st parameter XS[6:0] 2nd parameter XE[6:0] RASET 1st parameter YS[6:0] 2nd parameter YE[6:0] MADCTR Parameter RAMWR Scroll Video Data VSCSAD 1st parameter SSA[6:0] Scroll Mode Only required for non-rolling scrolling Redefines the Frame Memory Window that the scroll data will be written to. Optional - It may be necessary to redefine the frame memory write direction.																																																	
Legend Command Parameter Display Action Mode Sequential transfer																																																	

10.1.27 TEOFF (34h): Tearing Effect Line OFF

34H	TEOFF (Tearing Effect Line OFF)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)
Parameter	No Parameter												-
Description	-This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Default	Status						Default Value						
	Power On Sequence						OFF						
	S/W Reset						OFF						
	H/W Reset						OFF						
Flow Chart	TE Line Output ON ↓ TEOFF ↓ TE Line Output OFF Legend Command Parameter Display Action Mode Sequential transter												

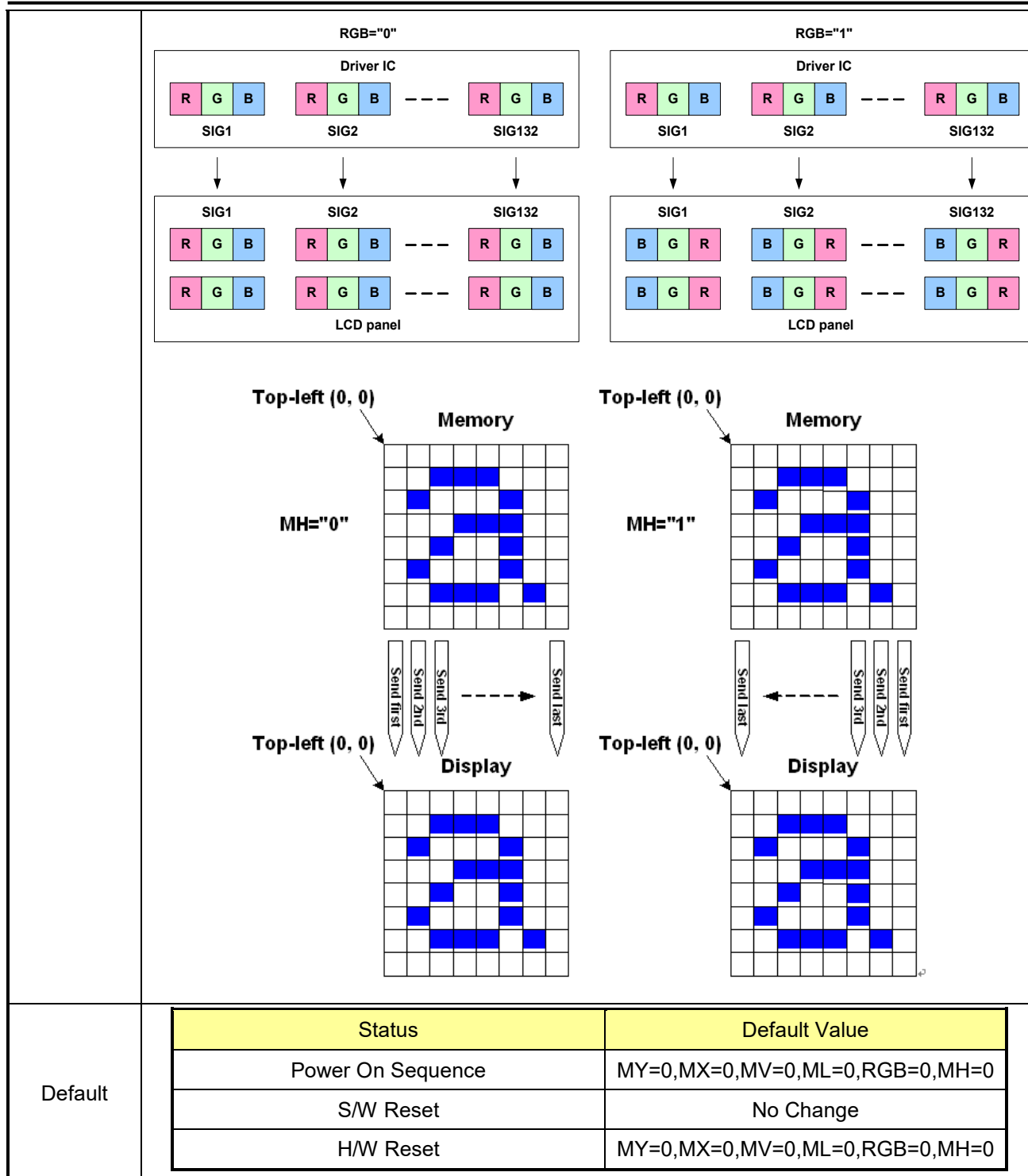
10.1.28 TEON (35h): Tearing Effect Line ON

35H	TEON (Tearing Effect Line ON)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)
Parameter	1	↑	1	-	0	0	0	0	0	0	0	TEM	
Description	-This command is used to turn ON the Tearing Effect output signal from the TE signal line. -This output is not affected by changing MADCTL bit ML. -The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line:												
	-When TEM = '0': The Tearing Effect output line consists of V-Blanking information only												
	Vertical time scale 												
	-When TEM = '1': The Tearing Effect output Line consists of both V-Blanking and H-Blanking information												
Vertical time scale 													
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.													
Default	Status						Default Value						
	Power On Sequence						Tearing effect off & TEM=0						
	S/W Reset						Tearing effect off & TEM=0						
	H/W Reset						Tearing effect off & TEM=0						

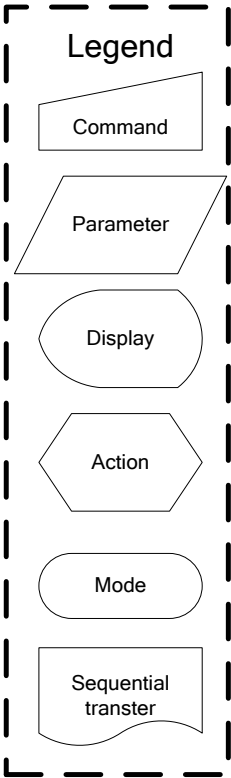
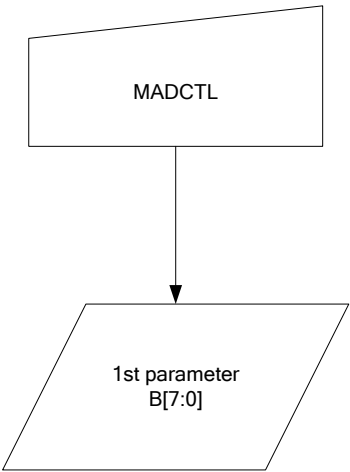


10.1.29 MADCTL (36h): Memory Data Access Control

36H		MADCTL (Memory Data Access Control)																														
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)																			
Parameter	1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-																				
Description	-This command defines read/ write scanning direction of frame memory.																															
	<table><tr><th>Bit</th><th>NAME</th><th>DESCRIPTION</th></tr><tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3bits controls MCU to memory Write / read direction.</td></tr><tr><td>MX</td><td>Column Address Order</td></tr><tr><td>MV</td><td>Row/Column Exchange</td></tr><tr><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top</td></tr><tr><td>RGB</td><td>RGB-BGR ORDER</td><td>Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)</td></tr><tr><td>MH</td><td>Horizontal Refresh Order</td><td>LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left</td></tr></table>													Bit	NAME	DESCRIPTION	MY	Row Address Order	These 3bits controls MCU to memory Write / read direction.	MX	Column Address Order	MV	Row/Column Exchange	ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top	RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)	MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left
	Bit	NAME	DESCRIPTION																													
	MY	Row Address Order	These 3bits controls MCU to memory Write / read direction.																													
	MX	Column Address Order																														
	MV	Row/Column Exchange																														
	ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top																													
	RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel)																													
	MH	Horizontal Refresh Order	LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left																													
	-Bit Assignment																															
Top-left (0, 0) Memory ML="0" Top-left (0, 0) Display Send first Send 2nd Send 3rd Send last																																
Top-left (0, 0) Memory ML="1" Top-left (0, 0) Display Send last Send 3rd Send 2nd Send first																																



Flow Chart



10.1.30 VSCSAD (37h): Vertical Scroll Start Address of RAM

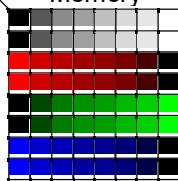
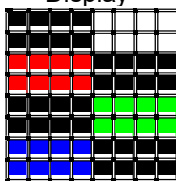
37H	SCRLAR (Scroll Area)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
VSCSAD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)												
Parameter1	1	↑	1	-	0	0	0	0	0	0	0	0													
Parameter2	1	↑	1	-	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	-												
Description	-This command is used together with Vertical Scrolling Definition (33h). -These two commands describe the scrolling area and the scrolling mode. -The Vertical Scrolling Start Address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: -This command Start the scrolling. -Exit from V-scrolling mode by commands Partial mode On (12h) or Normal mode On (13h) Memory (0,0) SSA [6:0] Scroll start address (0,161) Scan address 0 1 2 3 ... 160 161 → Display Memory (0,0) SSA [6:0] Scroll start address (0,161) Scan address 161 160 ... 3 2 1 0 → Display																								
	NOTE: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory line Pointer																								
Restriction	Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h))-otherwise undesirable image will be displayed on the Panel. SSA [6:0] is based on line unit. SSA [6:0] = 00h, 01h, 02h, 03h, ... , A1h																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	No																								
Partial Mode On, Idle Mode On, Sleep Out	No																								
Sleep In	Yes																								

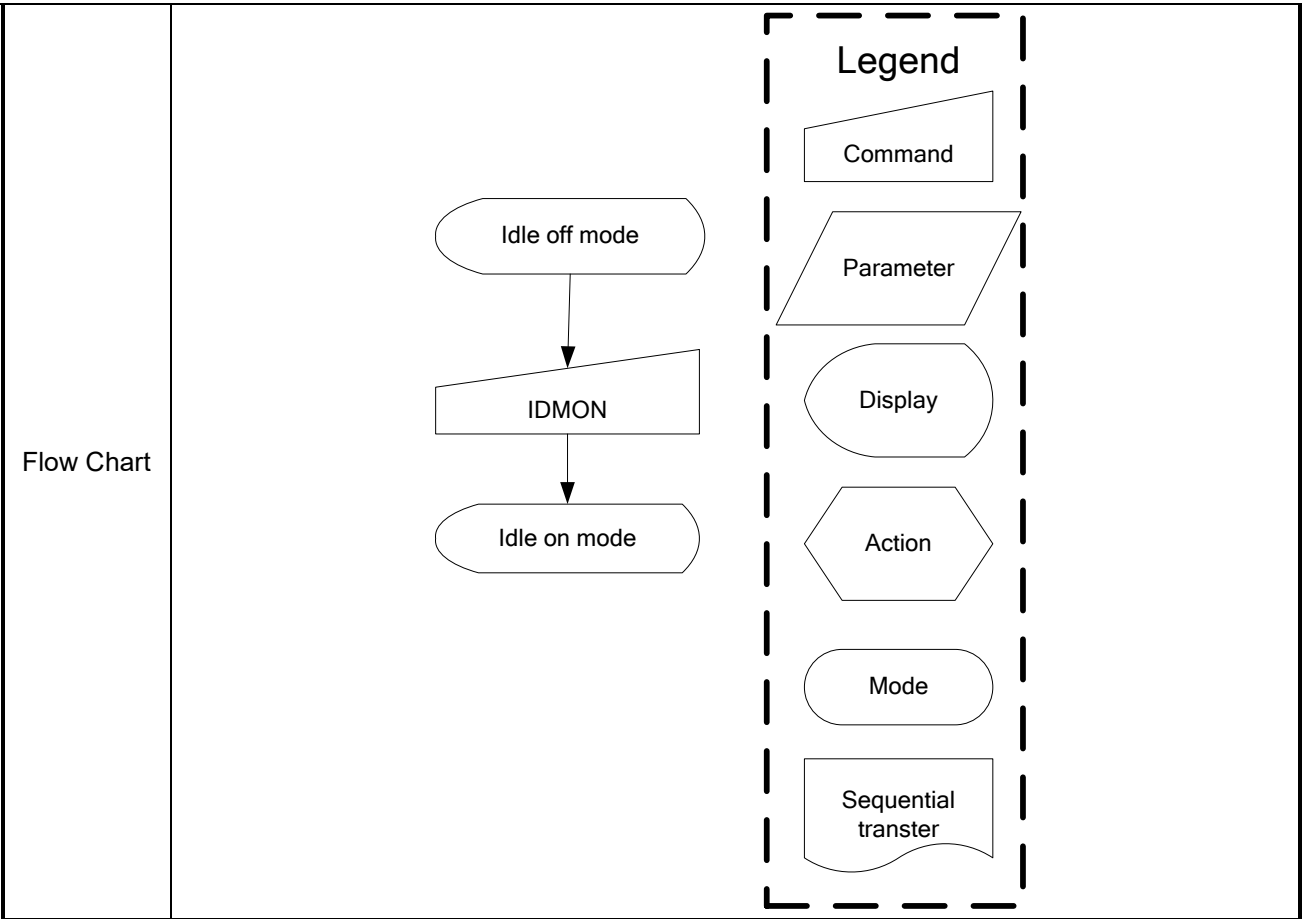
Default		
	Status	Default Value
	Power On Sequence	00h
	S/W Reset	00h
	H/W Reset	00h
Flow Chart	See Vertical Scrolling Definition (33h) description.	

10.1.31 IDMOFF (38h): Idle Mode Off

38H	IDMOFF (Idle Mode Off)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)
Parameter	No Parameter												-
Description	-This command is used to recover from Idle mode on. -In the idle off mode, 1. LCD can display 4096, 65k or 262k colors. 2. Normal frame frequency is applied.												
Default	Status						Default Value						
	Power On Sequence						Idle Mode Off						
	S/W Reset						Idle Mode Off						
	H/W Reset						Idle Mode Off						
Flow Chart	Idle on mode ↓ IDMOFF ↓ Idle off mode Legend Command Parameter Display Action Mode Sequential transfer												

10.1.32 IDMON (39h) : Idle Mode On

39H		IDMON (Idle Mode On)																																															
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)																																				
Parameter	No Parameter												-																																				
Description	-This command is used to enter into Idle mode on. -There will be no abnormal visible effect on the display mode change transition. -In the idle on mode, 1. Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed. 2. 8-Color mode frame frequency is applied. 3. Exit from IDMON by Idle Mode Off (38h) command (Example) Top-Left (0,0) Memory  Display 																																																
	<table><tr><th>Color</th><th>R5 R4 R3 R2 R1 R0</th><th>G5 G4 G3 G2 G1 G0</th><th>B5 B4 B3 B4 B1 B0</th></tr><tr><td>Black</td><td>0xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr><tr><td>Blue</td><td>0xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr><tr><td>Red</td><td>1xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr><tr><td>Magenta</td><td>1xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr><tr><td>Green</td><td>0xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr><tr><td>Cyan</td><td>0xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr><tr><td>Yellow</td><td>1xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr><tr><td>White</td><td>1xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr></table>													Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0	Black	0xxxxx	0xxxxx	0xxxxx	Blue	0xxxxx	0xxxxx	1xxxxx	Red	1xxxxx	0xxxxx	0xxxxx	Magenta	1xxxxx	0xxxxx	1xxxxx	Green	0xxxxx	1xxxxx	0xxxxx	Cyan	0xxxxx	1xxxxx	1xxxxx	Yellow	1xxxxx	1xxxxx	0xxxxx	White	1xxxxx	1xxxxx	1xxxxx
	Color	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B4 B1 B0																																													
	Black	0xxxxx	0xxxxx	0xxxxx																																													
	Blue	0xxxxx	0xxxxx	1xxxxx																																													
	Red	1xxxxx	0xxxxx	0xxxxx																																													
	Magenta	1xxxxx	0xxxxx	1xxxxx																																													
	Green	0xxxxx	1xxxxx	0xxxxx																																													
	Cyan	0xxxxx	1xxxxx	1xxxxx																																													
	Yellow	1xxxxx	1xxxxx	0xxxxx																																													
White	1xxxxx	1xxxxx	1xxxxx																																														
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes																								
	Status	Availability																																															
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																																															
	Normal Mode On, Idle Mode On, Sleep Out	Yes																																															
	Partial Mode On, Idle Mode Off, Sleep Out	No																																															
	Partial Mode On, Idle Mode On, Sleep Out	No																																															
Sleep In	Yes																																																
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></table>													Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off																												
	Status	Default Value																																															
	Power On Sequence	Idle Mode Off																																															
	S/W Reset	Idle Mode Off																																															
H/W Reset	Idle Mode Off																																																



10.1.33 COLMOD (3Ah): Interface Pixel Format

3AH	COLMOD (3Ah): Interface Pixel Format												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)
Parameter	1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0	
Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:												
	IFPF[2:0]			MCU Interface Color Format									
	011		3	12-bit/pixel									
	101		5	16-bit/pixel									
	110		6	18-bit/pixel									
111		7	No used										
Note1: In 12-bit/Pixel, 16-bit/Pixel or 18-bit/Pixel mode, the LUT is applied to transfer data into the Frame Memory.													
Note2: The Command 3Ah should be set at 55h when writing 16-bit/pixel data into frame memory, but 3Ah should be re-set to 66h when reading pixel data from frame memory. Please check the LUT in chapter 9.17 when using memory read function.													
Register Availability	Status									Availability			
	Normal Mode On, Idle Mode Off, Sleep Out									Yes			
	Normal Mode On, Idle Mode On, Sleep Out									Yes			
	Partial Mode On, Idle Mode Off, Sleep Out									No			
	Partial Mode On, Idle Mode On, Sleep Out									No			
	Sleep In									Yes			
Default	Status			Default Value									
				IFPF[2:0]					VIPF[3:0]				
	Power On Sequence			0110(18-bit/Pixel)					0110(18-bit/Pixel)				
	S/W Reset			No Change					No Change				
	H/W Reset			0110(18-bit/Pixel)					0110(18-bit/Pixel)				
Flow Chart	18-bit/Pixel Mode COLMOD 1st Parameter 16-bit/Pixel Mode Legend Command Parameter Display Action Mode Sequential transfer												

10.1.34 RDID1 (Dah): Read ID1 Value

DAH	RDID1 (Read ID1 Value)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-												
2 nd Parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10													
Description	-This read byte returns 8-bit LCD module's manufacturer ID -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. NOTE: See command RDDID (04h), 2nd parameter.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	No																								
Partial Mode On, Idle Mode On, Sleep Out	No																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>NV Value</td></tr><tr><td>S/W Reset</td><td>NV Value</td></tr><tr><td>H/W Reset</td><td>NV Value</td></tr></tbody></table>													Status	Default Value	Power On Sequence	NV Value	S/W Reset	NV Value	H/W Reset	NV Value				
Status	Default Value																								
Power On Sequence	NV Value																								
S/W Reset	NV Value																								
H/W Reset	NV Value																								
Flow Chart	Serial I/F Mode Read ID1 ↓ Send 2nd parameter Parallel I/F Mode Read ID1 ↓ Dummy Read ↓ Send 2nd parameter Legend Command Parameter Display Action Mode Sequential transter																								

10.1.35 RDID2 (DBh): Read ID2 Value

DBH	RDID2 (Read ID2 Value)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-												
2 nd Parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20													
Description	-This read byte returns 8-bit LCD module/driver version ID -The 1st parameter is dummy data -The 2nd parameter (ID27 to ID20): LCD module/driver version ID NOTE: See command RDDID (04h), 3rd parameter.																								
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	No																								
Partial Mode On, Idle Mode On, Sleep Out	No																								
Sleep In	Yes																								
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>NV Value</td></tr><tr><td>S/W Reset</td><td>NV Value</td></tr><tr><td>H/W Reset</td><td>NV Value</td></tr></table>													Status	Default Value	Power On Sequence	NV Value	S/W Reset	NV Value	H/W Reset	NV Value				
Status	Default Value																								
Power On Sequence	NV Value																								
S/W Reset	NV Value																								
H/W Reset	NV Value																								
Flow Chart	Serial I/F Mode Read ID2 ↓ Send 2nd parameter Parallel I/F Mode Read ID2 ↓ Dummy Read ↓ Send 2nd parameter Host Display Legend Command Parameter Display Action Mode Sequential transter																								

10.1.36 RDID3 (DCh): Read ID3 Value

DCH	RDID3 (Read ID2 Value)																								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)												
1 st Parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-												
2 nd Parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30													
Description	-This read byte returns 8-bit LCD module/driver ID. -The 1st parameter is dummy data -The 2nd parameter (ID37 to ID30): LCD module/driver ID. NOTE: See command RDDID (04h), 4th parameter.																								
Register Availability	<table><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></tbody></table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	No																								
Partial Mode On, Idle Mode On, Sleep Out	No																								
Sleep In	Yes																								
Default	<table><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>NV Value</td></tr><tr><td>S/W Reset</td><td>NV Value</td></tr><tr><td>H/W Reset</td><td>NV Value</td></tr></tbody></table>													Status	Default Value	Power On Sequence	NV Value	S/W Reset	NV Value	H/W Reset	NV Value				
Status	Default Value																								
Power On Sequence	NV Value																								
S/W Reset	NV Value																								
H/W Reset	NV Value																								
Flow Chart	Serial I/F Mode Read ID3 ↓ Send 2nd parameter Parallel I/F Mode Read ID3 ↓ Dummy Read ↓ Send 2nd parameter Host Display Legend Command Parameter Display Action Mode Sequential transfer																								

10.2 Panel Function Command List and Description

Table 18 Panel Function Command List (1)

Instruction	Refer	D/CX	WRX	RDX	D23-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
FRMCTR1	10.2.1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)	In Normal Mode (Full
		1	↑	1	-					RTNA3	RTNA2	RTNA1	RTNA0		RTNA Set
		1	↑	1	-			FPA5	FPA4	FPA3	FPA2	FPA1	FPA0		
		1	↑	1	-			BPA5	BPA4	BPA3	BPA2	BPA1	BPA0		
FRMCTR2	10.2.2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)	In Idle Mode (8-colors)
		1	↑	1	-					RTNB3	RTNB2	RTNB1	RTNB0		RTNB: Set
		1	↑	1	-			FPB5	FPB4	FPB3	FPB2	FPB1	FPB0		
		1	↑	1	-			BPB5	BPB4	BPB3	BPB2	BPB1	BPB0		
FRMCTR3	10.2.3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)	In Partial Mode + Full
		1	↑	1	-					RTNC3	RTNC2	RTNC1	RTNC0		RTNC,RTND:
		1	↑	1	-			FPC5	FPC4	FPC3	FPC2	FPC1	FPC0		
		1	↑	1	-			BPC5	BPC4	BPC3	BPC2	BPC1	BPC0		
		1	↑	1	-					RTND3	RTND2	RTND1	RTND0		
		1	↑	1	-			FPD5	FPD4	FPD3	FPD2	FPD1	FPD0		
		1	↑	1	-			BPD5	BPD4	BPD3	BPD2	BPD1	BPD0		
INVCTR	010.2.4	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)	Display Inversion
		1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC		NLA,NLB,NLC Set Inversion

Table 19 Panel Function Command List (2)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PWCTR1	10.2.5	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)	Power Control Setting
		1	↑	1	-	AVDD [2]	AVDD [1]	AVDD[0]	VRHP4	VRHP3	VRHP2	VRH P1	VRH P0		VRH: Set the GVDD Voltage
		1	↑	1	-	0	0	0	VRHN4	VRHN3	VRHN2	VRH N1	VRH N0		
PWCTR2	10.2.6	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)	Power Control Setting
		1	↑	1	-	VGH2 5[1]	VGH2 5[0]	VGLSEL [1]	VGLSEL [0]	VGLSEL [1]	VGLSEL [0]	VGH BT[1]	VGH BT[0]		BT: Set VGH/ VGL Voltage
PWCTR3	10.2.7	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)	In Normal Mode (Full Colors)
		1	↑	1	-	DCA9	DCA8	SAPA2	SAPA1	SAPA0	APA2	APA1	APA0		APA: Adjust the Operational Amplifier
					-	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA 1	DCA 0		DCA: Adjust the Booster Voltage
PWCTR4	10.2.8	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)	In Idle Mode (8-colors)
		1	↑	1	-	DCB9	DCB8	SAPB2	SAPB1	SAPB0	APB2	APB1	APB0		APB: Adjust the Operational Amplifier
					-	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB 1	DCB 0		DCB: Adjust the Booster Voltage
PWCTR5	10.2.9	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)	In Partial Mode + Full
		1	↑	1	-	DCC9	DCC8	SAPC2	SAPC1	SAPC0	APC2	APC 1	APC 0		APC: Adjust the
		1	↑	1	-	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC 1	DCC 0		
VMCTR	10.2.10	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)	VCOM Control
		1	↑	1	-	-	-	VCOMS 5	VCOM S4	VCOM S3	VCOM S2	VCO MS1	VCO MS0		VCOM Voltage Control
VMOFCT R	10.2.11	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)	Set VCOM Offset control
		1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF 1	VMF 0		
NVFCTR1	10.2.12	0	↑	1	-	1	1	0	1	0	1	1	1	(D7h)	NVM Enable Command
		1	↑	1	-	0	1	1	1	0	1	1	1		
		1	↑	1	-	0	0	1	1	0	1	0	1		
		1	↑	1	-	1	1	1	0	1	1	1	0		
		1	↑	1	-	VPPIN TMD	0	0	0	0	NV_EN	0	0		

“-”: Don't care

Note 1: C0h to C7h are fixed for about power controller

Table 20 Panel Function Command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NVFCTR2	10.2.13	0	↑	1	-	1	1	0	1	1	0	0	0	(D8h)	Set Address for NVM
		1	↑	1	-	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0		
NVFCTR3	10.2.14	0	↑	1	-	1	1	0	1	1	0	0	1	(D9h)	Set Data for NVM
		1	↑	1	-	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0		
NVFCTR4	10.2.15	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)	NVM Write Command Action Code
		1	↑	1	-	NVM_CMD7	NVM_CMD6	NVM_CMD5	NVM_CMD4	NVM_CMD3	NVM_CMD2	NVM_CMD1	NVM_CMD0		
NVFCTR5	10.2.16	0	↑	1	-	1	1	1	1	1	1	0	1	(FDh)	Custom Mode Enable Command
		1	↑	1	-	0	1	1	0	CTSM MD	0	0	0		

“-”: Don't care

Note 1: The D7h, D8h, D9 and DFh registers are used for NV Memory function controller. (Ex: write, clear, etc.)

Table 21 Panel Function Command List (4)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
GAMCTRP	10.2.16	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)	Set
		1	↑	1	-	-	-	VRFP[5]	VRFP[4]	VRFP[3]	VRFP[2]	VRFP[1]	VRFP[0]		Gamma Adjustment (+ Polarity)
		1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]		
		1	↑	1	-	-	-	PKP0[5]	PKP0[4]	PKP0[3]	PKP0[2]	PKP0[1]	PKP0[0]		
		1	↑	1	-	-	-	PKP1[5]	PKP1[4]	PKP1[3]	PKP1[2]	PKP1[1]	PKP1[0]		
		1	↑	1	-	-	-	PKP2[5]	PKP2[4]	PKP2[3]	PKP2[2]	PKP2[1]	PKP2[0]		
		1	↑	1	-	-	-	PKP3[5]	PKP3[4]	PKP3[3]	PKP3[2]	PKP3[1]	PKP3[0]		
		1	↑	1	-	-	-	PKP4[5]	PKP4[4]	PKP4[3]	PKP4[2]	PKP4[1]	PKP4[0]		
		1	↑	1	-	-	-	PKP5[5]	PKP5[4]	PKP5[3]	PKP5[2]	PKP5[1]	PKP5[0]		
		1	↑	1	-	-	-	PKP6[5]	PKP6[4]	PKP6[3]	PKP6[2]	PKP6[1]	PKP6[0]		
		1	↑	1	-	-	-	PKP7[5]	PKP7[4]	PKP7[3]	PKP7[2]	PKP7[1]	PKP7[0]		
		1	↑	1	-	-	-	PKP8[5]	PKP8[4]	PKP8[3]	PKP8[2]	PKP8[1]	PKP8[0]		
		1	↑	1	-	-	-	PKP9[5]	PKP9[4]	PKP9[3]	PKP9[2]	PKP9[1]	PKP9[0]		
		1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]		
		1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]		
		1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]		
		1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]		
GAMCTRN	10.2.17	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)	Set
		1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VRF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]		Gamma Adjustment (- Polarity)
		1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]		
		1	↑	1	-	-	-	PKN0[5]	PKN0[4]	PKN0[3]	PKN0[2]	PKN0[1]	PKN0[0]		
		1	↑	1	-	-	-	PKN1[5]	PKN1[4]	PKN1[3]	PKN1[2]	PKN1[1]	PKN1[0]		
		1	↑	1	-	-	-	PKN2[5]	PKN2[4]	PKN2[3]	PKN2[2]	PKN2[1]	PKN2[0]		
		1	↑	1	-	-	-	PKN3[5]	PKN3[4]	PKN3[3]	PKN3[2]	PKN3[1]	PKN3[0]		
		1	↑	1	-	-	-	PKN4[5]	PKN4[4]	PKN4[3]	PKN4[2]	PKN4[1]	PKN4[0]		
		1	↑	1	-	-	-	PKN5[5]	PKN5[4]	PKN5[3]	PKN5[2]	PKN5[1]	PKN5[0]		
		1	↑	1	-	-	-	PKN6[5]	PKN6[4]	PKN6[3]	PKN6[2]	PKN6[1]	PKN6[0]		
		1	↑	1	-	-	-	PKN7[5]	PKN7[4]	PKN7[3]	PKN7[2]	PKN7[1]	PKN7[0]		
		1	↑	1	-	-	-	PKN8[5]	PKN8[4]	PKN8[3]	PKN8[2]	PKN8[1]	PKN8[0]		
		1	↑	1	-	-	-	PKN9[5]	PKN9[4]	PKN9[3]	PKN9[2]	PKN9[1]	PKN9[0]		
		1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]		
		1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]		
		1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]		
		1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]		
GCV	10.2.18	1	↑	1	-	1	1	0	1	1	0	0	0	(FCh)	Gate clock
		1	↑	1	-	GCV Enable1	GCV Enable0	0	Clk Variable	Clk Variable		0	0		Variable

“-”: Don't care

Note 1: E0-E1 registers are fixed for adjusting Gamma

10.2.1 FRMCTR1 (B1h): Frame Rate Control (In normal mode/ Full colors)

B1H	FRMCTR1 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR1	0	↑	1	-	1	0	1	1	0	0	0	1	(B1h)
1 st Parameter	1	↑	1	-	-	-	-	-	RTNA 3	RTNA 2	RTNA 1	RTNA 0	
2 nd Parameter	1	↑	1	-	-	-	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0	
3 rd Parameter	1	↑	1	-	-	-	BPA5	BPA4	BPA3	BPA2	BPA1	BPA0	
Description	-Set the frame frequency of the full colors normal mode. - Frame rate=fosc/(((RTNA x 2 + 40) x (LINE + FPA + BPA +2)) -fosc = 850kHz -FPA > 0, BPA > 0												
Default	Status		Default Value										
			GM[1:0] = “00”				GM[1:0] = “01”				GM[1:0] = “11”		
	Power On Sequence		05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch		
	S/W Reset		05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch		
	H/W Reset		05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch		
Flow Chart	FRMCTR1 ↓ 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transfer												

10.2.2 FRMCTR2 (B2h): Frame Rate Control (In Idle mode/ 8-colors)

B2H	FRMCTR2 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR2	0	↑	1	-	1	0	1	1	0	0	1	0	(B2h)
1 st parameter	1	↑	1	-	-	-	-	-	RTNB 3	RTNB 2	RTNB 1	RTNB 0	
2 nd parameter	1	↑	1	-	-	-	FPB5	FPB4	FPB3	FPB2	FPB1	FPB0	
3 rd parameter	1	↑	1	-	-	-	BPB5	BPB4	BPB3	BPB2	BPB1	BPB0	
Description	-Set the frame frequency of the Idle mode. - Frame rate=fosc/((RTNA x 2 + 40) x (LINE + FPB + BPB + 2)) -fosc = 850kHz -FPB > 0, BPB > 0												
Default	Status				Default Value								
					GM[1:0] = “00”			GM[1:0] = “01”			GM[1:0] = “11”		
	Power On Sequence				05h/3Ah/3Ah			08h/3Bh/3Bh			05h/3Ch/3Ch		
	S/W Reset				05h/3Ah/3Ah			08h/3Bh/3Bh			05h/3Ch/3Ch		
	H/W Reset				05h/3Ah/3Ah			08h/3Bh/3Bh			05h/3Ch/3Ch		
Flow Chart	FRMCTR2 ↓ 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transfer												

10.2.3 FRMCTR3 (B3h): Frame Rate Control (In Partial mode/ full colors)

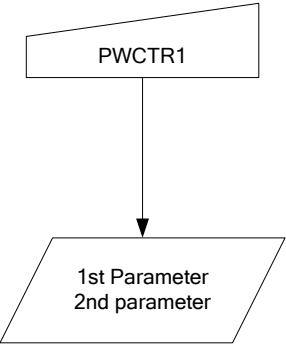
B3H	FRMCTR3 (Frame Rate Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FRMCTR3	0	↑	1	-	1	0	1	1	0	0	1	1	(B3h)
1 st parameter	1	↑	1	-	-	-	-	-	RTNC	RTNC	RTNC	RTNC	
2 nd parameter	1	↑	1	-	-	-	FPC5	FPC4	FPC3	FPC2	FPC1	FPC0	
3 rd parameter	1	↑	1	-	-	-	BPC5	BPC4	BPC3	BPC2	BPC1	BPC0	
4 th parameter	1	↑	1	-	-	-	-	-	RTND	RTND	RTND	RTND	
5 th parameter	1	↑	1	-	-	-	FPD5	FPD4	FPD3	FPD2	FPD1	FPD0	
6 th parameter	1	↑	1	-	-	-	BPD5	BPD4	BPD3	BPD2	BPD1	BPD0	
Description	-Set the frame frequency of the Partial mode/ full colors. - 1st parameter to 3rd parameter are used in dot inversion mode. - 4th parameter to 6th parameter are used in column inversion mode. - Frame rate=fosc/((RTNA x 2 + 40) x (LINE + FPC + BPC +2)) -fosc = 850kHz -FPC > 0, BPC > 0												
Default	Status		Default Value										
			GM[1:0] = “00”				GM[1:0] = “01”				GM[1:0] = “11”		
	Power On Sequence	05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch			
		05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch			
	S/W Reset	05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch			
		05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch			
	H/W Reset	05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch			
		05h/3Ah/3Ah				08h/3Bh/3Bh				05h/3Ch/3Ch			
Flow Chart	FRMCTR3 ↓ 1st Parameter 6nd parameter Legend Command Parameter Display Action Mode Sequential transter												

10.2.4 INVCTR (B4h): Display Inversion Control

B4H	INVCTR (Display Inversion Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
INVCTR	0	↑	1	-	1	0	1	1	0	1	0	0	(B4h)
Parameter	1	↑	1	-	0	0	0	0	0	NLA	NLB	NLC	
Description	-Display Inversion mode control -NLA: Inversion setting in full colors normal mode (Normal mode on)												
	NLA			Inversion setting in full Colors normal mode									
	0			Dot Inversion									
	1			Column Inversion									
	-NLB: Inversion setting in Idle mode (Idle mode on)												
	NLB			Inversion setting in Idle mode									
	0			Dot Inversion									
	1			Column Inversion									
	-NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)												
	NLC			Inversion setting in full Colors partial mode									
	0			Dot Inversion									
	1			Column Inversion									
Default			Status					Default Value					
								B4h					
			Power On Sequence					07h					
			S/W Reset					07h					
			H/W Reset					07h					
Flow Chart	INVCTR ↓ 1st Parameter Legend Command Parameter Display Action Mode Sequential transfer												

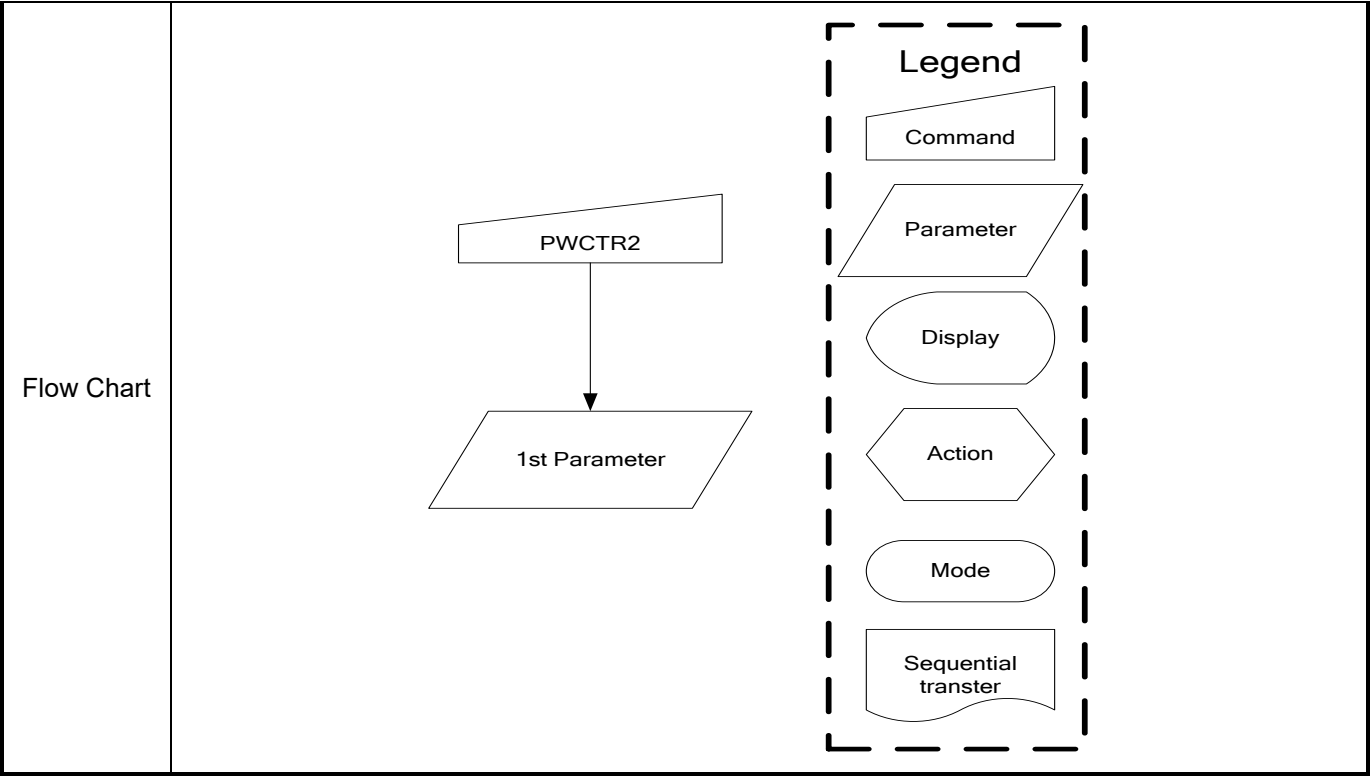
10.2.5 PWCTR1 (C0h): Power Control 1

C0H	PWCTR1 (Power Control 1)																																																																																																																																																
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																				
PWCTR1	0	↑	1	-	1	1	0	0	0	0	0	0	(C0h)																																																																																																																																				
1 st parameter	1	↑	1	-	AVDD[2]	AVDD[1]	AVDD[0]	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0																																																																																																																																					
2 nd parameter	1	↑	1	-	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0																																																																																																																																					
Description	<table><tr><th colspan="2">AVDD[2:0]</th><th colspan="2">AVDD</th></tr><tr><td colspan="2">000</td><td colspan="2">4.5</td></tr><tr><td colspan="2">001</td><td colspan="2">4.6</td></tr><tr><td colspan="2">010</td><td colspan="2">4.7</td></tr><tr><td colspan="2">011</td><td colspan="2">4.8</td></tr><tr><td colspan="2">100</td><td colspan="2">4.9</td></tr><tr><td colspan="2">101</td><td colspan="2">5.0</td></tr><tr><td colspan="2">110</td><td colspan="2">5.1</td></tr><tr><td colspan="2">111</td><td colspan="2">5.2</td></tr></table>													AVDD[2:0]		AVDD		000		4.5		001		4.6		010		4.7		011		4.8		100		4.9		101		5.0		110		5.1		111		5.2																																																																																																	
	AVDD[2:0]		AVDD																																																																																																																																														
	000		4.5																																																																																																																																														
	001		4.6																																																																																																																																														
	010		4.7																																																																																																																																														
	011		4.8																																																																																																																																														
	100		4.9																																																																																																																																														
	101		5.0																																																																																																																																														
	110		5.1																																																																																																																																														
	111		5.2																																																																																																																																														
	<table><tr><th colspan="2">VRHP[4:0]</th><th colspan="2">GVDD</th></tr><tr><td>00000</td><td>4.7</td><td></td><td></td></tr><tr><td>00001</td><td>4.65</td><td></td><td></td></tr><tr><td>00010</td><td>4.6</td><td></td><td></td></tr><tr><td>00011</td><td>4.55</td><td></td><td></td></tr><tr><td>00100</td><td>4.5</td><td></td><td></td></tr><tr><td>00101</td><td>4.45</td><td></td><td></td></tr><tr><td>00110</td><td>4.4</td><td></td><td></td></tr><tr><td>00111</td><td>4.35</td><td></td><td></td></tr><tr><td>01000</td><td>4.3</td><td></td><td></td></tr><tr><td>01001</td><td>4.25</td><td></td><td></td></tr><tr><td>01010</td><td>4.2</td><td></td><td></td></tr><tr><td>01011</td><td>4.15</td><td></td><td></td></tr><tr><td>01100</td><td>4.1</td><td></td><td></td></tr><tr><td>01101</td><td>4.05</td><td></td><td></td></tr><tr><td>01110</td><td>4</td><td></td><td></td></tr><tr><td>01111</td><td>3.95</td><td></td><td></td></tr><tr><td>10000</td><td>3.9</td><td></td><td></td></tr><tr><td>10001</td><td>3.85</td><td></td><td></td></tr><tr><td>10010</td><td>3.8</td><td></td><td></td></tr><tr><td>10011</td><td>3.75</td><td></td><td></td></tr><tr><td>10100</td><td>3.7</td><td></td><td></td></tr><tr><td>10101</td><td>3.65</td><td></td><td></td></tr><tr><td>10110</td><td>3.6</td><td></td><td></td></tr><tr><td>10111</td><td>3.55</td><td></td><td></td></tr><tr><td>11000</td><td>3.5</td><td></td><td></td></tr><tr><td>11001</td><td>3.45</td><td></td><td></td></tr><tr><td>11010</td><td>3.4</td><td></td><td></td></tr><tr><td>11011</td><td>3.35</td><td></td><td></td></tr><tr><td>11100</td><td>3.3</td><td></td><td></td></tr><tr><td>11101</td><td>3.25</td><td></td><td></td></tr><tr><td>11110</td><td>3.2</td><td></td><td></td></tr><tr><td>11111</td><td>3.15</td><td></td><td></td></tr></table>													VRHP[4:0]		GVDD		00000	4.7			00001	4.65			00010	4.6			00011	4.55			00100	4.5			00101	4.45			00110	4.4			00111	4.35			01000	4.3			01001	4.25			01010	4.2			01011	4.15			01100	4.1			01101	4.05			01110	4			01111	3.95			10000	3.9			10001	3.85			10010	3.8			10011	3.75			10100	3.7			10101	3.65			10110	3.6			10111	3.55			11000	3.5			11001	3.45			11010	3.4			11011	3.35			11100	3.3			11101	3.25			11110	3.2			11111	3.15		
	VRHP[4:0]		GVDD																																																																																																																																														
	00000	4.7																																																																																																																																															
	00001	4.65																																																																																																																																															
	00010	4.6																																																																																																																																															
	00011	4.55																																																																																																																																															
	00100	4.5																																																																																																																																															
	00101	4.45																																																																																																																																															
	00110	4.4																																																																																																																																															
	00111	4.35																																																																																																																																															
	01000	4.3																																																																																																																																															
	01001	4.25																																																																																																																																															
	01010	4.2																																																																																																																																															
	01011	4.15																																																																																																																																															
	01100	4.1																																																																																																																																															
	01101	4.05																																																																																																																																															
	01110	4																																																																																																																																															
	01111	3.95																																																																																																																																															
	10000	3.9																																																																																																																																															
	10001	3.85																																																																																																																																															
	10010	3.8																																																																																																																																															
	10011	3.75																																																																																																																																															
	10100	3.7																																																																																																																																															
	10101	3.65																																																																																																																																															
	10110	3.6																																																																																																																																															
	10111	3.55																																																																																																																																															
	11000	3.5																																																																																																																																															
	11001	3.45																																																																																																																																															
	11010	3.4																																																																																																																																															
	11011	3.35																																																																																																																																															
	11100	3.3																																																																																																																																															
	11101	3.25																																																																																																																																															
	11110	3.2																																																																																																																																															
	11111	3.15																																																																																																																																															
	<table><tr><th colspan="2">VRHN[4:0]</th><th colspan="2">GVCL</th></tr><tr><td>00000</td><td>-4.7</td><td></td><td></td></tr><tr><td>00001</td><td>-4.65</td><td></td><td></td></tr><tr><td>00010</td><td>-4.6</td><td></td><td></td></tr><tr><td>00011</td><td>-4.55</td><td></td><td></td></tr><tr><td>00100</td><td>-4.5</td><td></td><td></td></tr><tr><td>00101</td><td>-4.45</td><td></td><td></td></tr><tr><td>00110</td><td>-4.4</td><td></td><td></td></tr><tr><td>00111</td><td>-4.35</td><td></td><td></td></tr><tr><td>01000</td><td>-4.3</td><td></td><td></td></tr><tr><td>01001</td><td>-4.25</td><td></td><td></td></tr><tr><td>01010</td><td>-4.2</td><td></td><td></td></tr><tr><td>01011</td><td>-4.15</td><td></td><td></td></tr><tr><td>01100</td><td>-4.1</td><td></td><td></td></tr><tr><td>01101</td><td>-4.05</td><td></td><td></td></tr><tr><td>01110</td><td>-4</td><td></td><td></td></tr><tr><td>01111</td><td>-3.95</td><td></td><td></td></tr><tr><td>10000</td><td>-3.9</td><td></td><td></td></tr><tr><td>10001</td><td>-3.85</td><td></td><td></td></tr><tr><td>10010</td><td>-3.8</td><td></td><td></td></tr><tr><td>10011</td><td>-3.75</td><td></td><td></td></tr><tr><td>10100</td><td>-3.7</td><td></td><td></td></tr><tr><td>10101</td><td>-3.65</td><td></td><td></td></tr><tr><td>10110</td><td>-3.6</td><td></td><td></td></tr><tr><td>10111</td><td>-3.55</td><td></td><td></td></tr><tr><td>11000</td><td>-3.5</td><td></td><td></td></tr><tr><td>11001</td><td>-3.45</td><td></td><td></td></tr><tr><td>11010</td><td>-3.4</td><td></td><td></td></tr><tr><td>11011</td><td>-3.35</td><td></td><td></td></tr><tr><td>11100</td><td>-3.3</td><td></td><td></td></tr><tr><td>11101</td><td>-3.25</td><td></td><td></td></tr><tr><td>11110</td><td>-3.2</td><td></td><td></td></tr><tr><td>11111</td><td>-3.15</td><td></td><td></td></tr></table>													VRHN[4:0]		GVCL		00000	-4.7			00001	-4.65			00010	-4.6			00011	-4.55			00100	-4.5			00101	-4.45			00110	-4.4			00111	-4.35			01000	-4.3			01001	-4.25			01010	-4.2			01011	-4.15			01100	-4.1			01101	-4.05			01110	-4			01111	-3.95			10000	-3.9			10001	-3.85			10010	-3.8			10011	-3.75			10100	-3.7			10101	-3.65			10110	-3.6			10111	-3.55			11000	-3.5			11001	-3.45			11010	-3.4			11011	-3.35			11100	-3.3			11101	-3.25			11110	-3.2			11111	-3.15		
	VRHN[4:0]		GVCL																																																																																																																																														
	00000	-4.7																																																																																																																																															
	00001	-4.65																																																																																																																																															
	00010	-4.6																																																																																																																																															
	00011	-4.55																																																																																																																																															
00100	-4.5																																																																																																																																																
00101	-4.45																																																																																																																																																
00110	-4.4																																																																																																																																																
00111	-4.35																																																																																																																																																
01000	-4.3																																																																																																																																																
01001	-4.25																																																																																																																																																
01010	-4.2																																																																																																																																																
01011	-4.15																																																																																																																																																
01100	-4.1																																																																																																																																																
01101	-4.05																																																																																																																																																
01110	-4																																																																																																																																																
01111	-3.95																																																																																																																																																
10000	-3.9																																																																																																																																																
10001	-3.85																																																																																																																																																
10010	-3.8																																																																																																																																																
10011	-3.75																																																																																																																																																
10100	-3.7																																																																																																																																																
10101	-3.65																																																																																																																																																
10110	-3.6																																																																																																																																																
10111	-3.55																																																																																																																																																
11000	-3.5																																																																																																																																																
11001	-3.45																																																																																																																																																
11010	-3.4																																																																																																																																																
11011	-3.35																																																																																																																																																
11100	-3.3																																																																																																																																																
11101	-3.25																																																																																																																																																
11110	-3.2																																																																																																																																																
11111	-3.15																																																																																																																																																

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th>Default Value</th></tr> <tr> <td>C0h</td></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>A8h/08h/84h</td></tr> <tr> <td>S/W Reset</td><td>A8h/08h/84h</td></tr> <tr> <td>H/W Reset</td><td>A8h/08h/84h</td></tr> </tbody> </table>	Status	Default Value	C0h	Power On Sequence	A8h/08h/84h	S/W Reset	A8h/08h/84h	H/W Reset	A8h/08h/84h			
Status	Default Value												
	C0h												
Power On Sequence	A8h/08h/84h												
S/W Reset	A8h/08h/84h												
H/W Reset	A8h/08h/84h												
Flow Chart	 <pre> graph TD PWCTR1[PWCTR1] --> Param[1st Parameter
2nd parameter] </pre> Legend - Command - Parameter - Display - Action - Mode - Sequential transter												

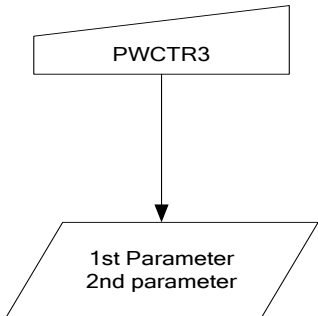
10.2.6 PWCTR2 (C1h): Power Control 2

C1H	PWCTR2 (Power Control 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWCTR2	0	↑	1	-	1	1	0	0	0	0	0	1	(C1h)
1 st parameter	1	↑	1		VGH25[1]	VGH25[0]	VGLSEL[1]	VGLSEL[0]	VGLSEL[1]	VGLSEL[0]	VGHBT[1]	VGHBT[0]	
Description	-Set the VGH and VGL supply power level												
						VGH25[1:0]		V25					
						00		2.1					
						01		2.2					
						10		2.3					
						11		2.4					
						VGHBT[1:0]		VGH					
						00		2*AVDD+VGH25-0.5					
						01		3*AVDD-0.5					
					10		3*AVDD+VGH25-0.5						
					11		Don't use this setting, reserve for testing.						
					VGLSEL[1:0]		VGL						
					00		-7.5						
					01		-10						
					10		-12						
					11		-12.5						
Restriction	-The deviation value of VGH/ VGL between with Measurement and Specification: Max <= 1V -VGH-VGL <= 32V												
Register Availability													
	Status							Availability					
	Normal Mode On, Idle Mode Off, Sleep Out							Yes					
	Normal Mode On, Idle Mode On, Sleep Out							Yes					
	Partial Mode On, Idle Mode Off, Sleep Out							Yes					
	Partial Mode On, Idle Mode On, Sleep Out							Yes					
Sleep In							Yes						
Default													
	Status							Default Value					
								C1h					
	Power On Sequence							C0h					
	S/W Reset							C0h					
	H/W Reset							C0h					



10.2.7 PWCTR3 (C2h): Power Control 3 (in Normal mode/ Full colors)

C2H	PWCTR3 (Power Control 3)																																									
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
PWCTR3	0	↑	1	-	1	1	0	0	0	0	1	0	(C2h)																													
1 st	1	↑	1	-	DCA9	DCA8	SAPA2	SAPA1	SAPA0	APA2	APA1	APA0																														
2 nd	1	↑	1	-	DCA7	DCA6	DCA5	DCA4	DCA3	DCA2	DCA1	DCA0																														
Description	-Set the amount of current in Operational amplifier in normal mode/full colors. -Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.																																									
	<table><tr><th>AP[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>Small</td></tr><tr><td>010</td><td>Medium Low</td></tr><tr><td>011</td><td>Medium</td></tr><tr><td>100</td><td>Medium High</td></tr><tr><td>101</td><td>Large</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table>													AP[2:0]	Amount of Current in Operational Amplifier	000	Operation of the operational amplifier stops	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved											
	AP[2:0]	Amount of Current in Operational Amplifier																																								
	000	Operation of the operational amplifier stops																																								
	001	Small																																								
	010	Medium Low																																								
	011	Medium																																								
	100	Medium High																																								
	101	Large																																								
	110	Reserved																																								
111	Reserved																																									
<table><tr><th>SAP[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>Small</td></tr><tr><td>010</td><td>Medium Low</td></tr><tr><td>011</td><td>Medium</td></tr><tr><td>100</td><td>Medium High</td></tr><tr><td>101</td><td>Large</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table>													SAP[2:0]	Amount of Current in Operational Amplifier	000	Operation of the operational amplifier stops	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved												
SAP[2:0]	Amount of Current in Operational Amplifier																																									
000	Operation of the operational amplifier stops																																									
001	Small																																									
010	Medium Low																																									
011	Medium																																									
100	Medium High																																									
101	Large																																									
110	Reserved																																									
111	Reserved																																									
-Set the Booster circuit Step-up cycle in Normal mode/ full colors.																																										
<table><tr><th></th><th>DCA[9:8]</th><th>DCA[7:6]</th><th>DCA[5:4]</th><th>DCA[3:2]</th><th>DCA[1:0]</th></tr><tr><td>00</td><td>BCLK/2.5</td><td>BCLK/6</td><td>BCLK/4</td><td>BCLK/2.5</td><td>BCLK/2.5</td></tr><tr><td>01</td><td>BCLK/4</td><td>BCLK/4</td><td>BCLK/6</td><td>BCLK/4</td><td>BCLK/4</td></tr><tr><td>10</td><td>BCLK/3</td><td>BCLK/8</td><td>BCLK/5</td><td>BCLK/3</td><td>BCLK/3</td></tr><tr><td>11</td><td>BCLK/5</td><td>BCLK/6</td><td>BCLK/8</td><td>BCLK/5</td><td>BCLK/5</td></tr></table>														DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]	00	BCLK/2.5	BCLK/6	BCLK/4	BCLK/2.5	BCLK/2.5	01	BCLK/4	BCLK/4	BCLK/6	BCLK/4	BCLK/4	10	BCLK/3	BCLK/8	BCLK/5	BCLK/3	BCLK/3	11	BCLK/5	BCLK/6	BCLK/8	BCLK/5	BCLK/5
	DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]																																					
00	BCLK/2.5	BCLK/6	BCLK/4	BCLK/2.5	BCLK/2.5																																					
01	BCLK/4	BCLK/4	BCLK/6	BCLK/4	BCLK/4																																					
10	BCLK/3	BCLK/8	BCLK/5	BCLK/3	BCLK/3																																					
11	BCLK/5	BCLK/6	BCLK/8	BCLK/5	BCLK/5																																					
DCA[9:8]=AVDD ; DCA[7:6]=VGH ; DCA[5:4]=VGL ; DCA[3:2]=AVCL ; DCA[1:0]=VCOM Note: BCLK is Clock frequency for Booster circuit																																										

Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
Partial Mode On, Idle Mode Off, Sleep Out	Yes												
Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th>Default Value</th></tr> <tr> <th>C2h</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>0Ah/00h</td></tr> <tr> <td>S/W Reset</td><td>0Ah/00h</td></tr> <tr> <td>H/W Reset</td><td>0Ah/00h</td></tr> </tbody> </table>	Status	Default Value	C2h	Power On Sequence	0Ah/00h	S/W Reset	0Ah/00h	H/W Reset	0Ah/00h			
Status	Default Value												
	C2h												
Power On Sequence	0Ah/00h												
S/W Reset	0Ah/00h												
H/W Reset	0Ah/00h												
Flow Chart	 <pre> graph TD PWCTR3[PWCTR3] --> ParamBox[/1st Parameter
2nd parameter/] </pre> Legend Command Parameter Display Action Mode Sequential transfer												

10.2.8 PWCTR4 (C3h): Power Control 4 (in Idle mode/ 8-colors)

C3H	PWCTR4 (Power Control 4)																																									
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
PWCTR4	0	↑	1	-	1	1	0	0	0	0	1	1	(C3h)																													
1 st parameter	1	↑	1	-	DCB9	DCB8	SAPB2	SAPB1	SAPB0	APB2	APB1	APB0																														
2 nd parameter	1	↑	1	-	DCB7	DCB6	DCB5	DCB4	DCB3	DCB2	DCB1	DCB0																														
Description	-Set the amount of current in Operational amplifier in Idle mode/8 colors or column inversion.																																									
	-Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver.																																									
	<table><tr><th>AP[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>Small</td></tr><tr><td>010</td><td>Medium Low</td></tr><tr><td>011</td><td>Medium</td></tr><tr><td>100</td><td>Medium High</td></tr><tr><td>101</td><td>Large</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table>													AP[2:0]	Amount of Current in Operational Amplifier	000	Operation of the operational amplifier stops	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved											
	AP[2:0]	Amount of Current in Operational Amplifier																																								
	000	Operation of the operational amplifier stops																																								
	001	Small																																								
	010	Medium Low																																								
	011	Medium																																								
	100	Medium High																																								
	101	Large																																								
110	Reserved																																									
111	Reserved																																									
<table><tr><th>SAP[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>Small</td></tr><tr><td>010</td><td>Medium Low</td></tr><tr><td>011</td><td>Medium</td></tr><tr><td>100</td><td>Medium High</td></tr><tr><td>101</td><td>Large</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table>													SAP[2:0]	Amount of Current in Operational Amplifier	000	Operation of the operational amplifier stops	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved												
SAP[2:0]	Amount of Current in Operational Amplifier																																									
000	Operation of the operational amplifier stops																																									
001	Small																																									
010	Medium Low																																									
011	Medium																																									
100	Medium High																																									
101	Large																																									
110	Reserved																																									
111	Reserved																																									
-Set the Booster circuit Step-up cycle in Idle mode/8 colors.																																										
<table><tr><th></th><th>DCA[9:8]</th><th>DCA[7:6]</th><th>DCA[5:4]</th><th>DCA[3:2]</th><th>DCA[1:0]</th></tr><tr><td>00</td><td>BCLK/2.5</td><td>BCLK/6</td><td>BCLK/4</td><td>BCLK/2.5</td><td>BCLK/2.5</td></tr><tr><td>01</td><td>BCLK/4</td><td>BCLK/4</td><td>BCLK/6</td><td>BCLK/4</td><td>BCLK/4</td></tr><tr><td>10</td><td>BCLK/3</td><td>BCLK/8</td><td>BCLK/5</td><td>BCLK/3</td><td>BCLK/3</td></tr><tr><td>11</td><td>BCLK/5</td><td>BCLK/6</td><td>BCLK/8</td><td>BCLK/5</td><td>BCLK/5</td></tr></table>														DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]	00	BCLK/2.5	BCLK/6	BCLK/4	BCLK/2.5	BCLK/2.5	01	BCLK/4	BCLK/4	BCLK/6	BCLK/4	BCLK/4	10	BCLK/3	BCLK/8	BCLK/5	BCLK/3	BCLK/3	11	BCLK/5	BCLK/6	BCLK/8	BCLK/5	BCLK/5
	DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]																																					
00	BCLK/2.5	BCLK/6	BCLK/4	BCLK/2.5	BCLK/2.5																																					
01	BCLK/4	BCLK/4	BCLK/6	BCLK/4	BCLK/4																																					
10	BCLK/3	BCLK/8	BCLK/5	BCLK/3	BCLK/3																																					
11	BCLK/5	BCLK/6	BCLK/8	BCLK/5	BCLK/5																																					
DCA[9:8]=AVDD ; DCA[7:6]=VGH ; DCA[5:4]=VGL ; DCA[3:2]=AVCL ; DCA[1:0]=VCOM																																										
Note: BCLK is Clock frequency for Booster circuit																																										

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><td>C3h</td></tr><tr><td>Power On Sequence</td><td>8Ah/26h</td></tr><tr><td>S/W Reset</td><td>8Ah/26h</td></tr><tr><td>H/W Reset</td><td>8Ah/26h</td></tr></table>		Status	Default Value	C3h	Power On Sequence	8Ah/26h	S/W Reset	8Ah/26h	H/W Reset	8Ah/26h			
	Status	Default Value												
		C3h												
	Power On Sequence	8Ah/26h												
	S/W Reset	8Ah/26h												
H/W Reset	8Ah/26h													
Flow Chart	PWCTR4 ↓ 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transfer													

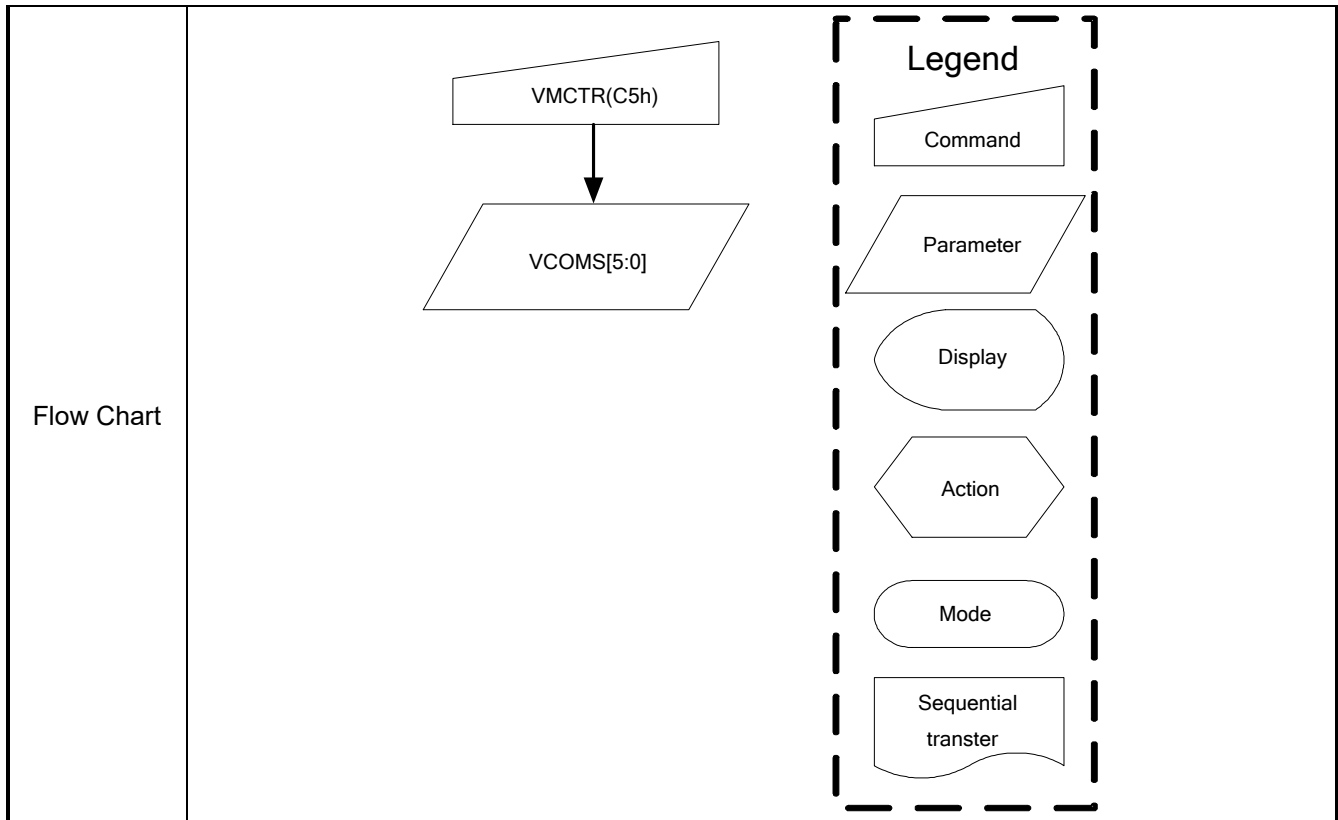
10.2.9 PWCTR5 (C4h): Power Control 5 (in Partial mode/ full-colors)

C4H	PWCTR5 (Power Control 5)																																																
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
PWCTR5	0	↑	1	-	1	1	0	0	0	1	0	0	(C4h)																																				
1 st parameter	1	↑	1	-	DCC9	DCC8	SAPC2	SAPC1	SAPC0	APC2	APC1	APC0																																					
2 nd parameter	1	↑	1	-	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1	DCC0																																					
Description	-Set the amount of current in Operational amplifier in Partial mode/ full-colors. -Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver. <table><tr><th>AP[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>Small</td></tr><tr><td>010</td><td>Medium Low</td></tr><tr><td>011</td><td>Medium</td></tr><tr><td>100</td><td>Medium High</td></tr><tr><td>101</td><td>Large</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table> <table><tr><th>SAP[2:0]</th><th>Amount of Current in Operational Amplifier</th></tr><tr><td>000</td><td>Operation of the operational amplifier stops</td></tr><tr><td>001</td><td>Small</td></tr><tr><td>010</td><td>Medium Low</td></tr><tr><td>011</td><td>Medium</td></tr><tr><td>100</td><td>Medium High</td></tr><tr><td>101</td><td>Large</td></tr><tr><td>110</td><td>Reserved</td></tr><tr><td>111</td><td>Reserved</td></tr></table>													AP[2:0]	Amount of Current in Operational Amplifier	000	Operation of the operational amplifier stops	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved	SAP[2:0]	Amount of Current in Operational Amplifier	000	Operation of the operational amplifier stops	001	Small	010	Medium Low	011	Medium	100	Medium High	101	Large	110	Reserved	111	Reserved
	AP[2:0]	Amount of Current in Operational Amplifier																																															
	000	Operation of the operational amplifier stops																																															
	001	Small																																															
	010	Medium Low																																															
	011	Medium																																															
	100	Medium High																																															
	101	Large																																															
	110	Reserved																																															
	111	Reserved																																															
SAP[2:0]	Amount of Current in Operational Amplifier																																																
000	Operation of the operational amplifier stops																																																
001	Small																																																
010	Medium Low																																																
011	Medium																																																
100	Medium High																																																
101	Large																																																
110	Reserved																																																
111	Reserved																																																
-Set the Booster circuit Step-up cycle in Partial mode/ full-colors. <table><tr><th></th><th>DCA[9:8]</th><th>DCA[7:6]</th><th>DCA[5:4]</th><th>DCA[3:2]</th><th>DCA[1:0]</th></tr><tr><td>00</td><td>BCLK/2.5</td><td>BCLK/6</td><td>BCLK/4</td><td>BCLK/2.5</td><td>BCLK/2.5</td></tr><tr><td>01</td><td>BCLK/4</td><td>BCLK/4</td><td>BCLK/6</td><td>BCLK/4</td><td>BCLK/4</td></tr><tr><td>10</td><td>BCLK/3</td><td>BCLK/8</td><td>BCLK/5</td><td>BCLK/3</td><td>BCLK/3</td></tr><tr><td>11</td><td>BCLK/5</td><td>BCLK/6</td><td>BCLK/8</td><td>BCLK/5</td><td>BCLK/5</td></tr></table> DCA[9:8]=AVDD ; DCA[7:6]=VGH ; DCA[5:4]=VGL ; DCA[3:2]=AVCL ; DCA[1:0]=VCOM <i>Note: BCLK is Clock frequency for Booster circuit</i>														DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]	00	BCLK/2.5	BCLK/6	BCLK/4	BCLK/2.5	BCLK/2.5	01	BCLK/4	BCLK/4	BCLK/6	BCLK/4	BCLK/4	10	BCLK/3	BCLK/8	BCLK/5	BCLK/3	BCLK/3	11	BCLK/5	BCLK/6	BCLK/8	BCLK/5	BCLK/5							
	DCA[9:8]	DCA[7:6]	DCA[5:4]	DCA[3:2]	DCA[1:0]																																												
00	BCLK/2.5	BCLK/6	BCLK/4	BCLK/2.5	BCLK/2.5																																												
01	BCLK/4	BCLK/4	BCLK/6	BCLK/4	BCLK/4																																												
10	BCLK/3	BCLK/8	BCLK/5	BCLK/3	BCLK/3																																												
11	BCLK/5	BCLK/6	BCLK/8	BCLK/5	BCLK/5																																												

Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability												
	Normal Mode On, Idle Mode Off, Sleep Out	Yes												
	Normal Mode On, Idle Mode On, Sleep Out	Yes												
	Partial Mode On, Idle Mode Off, Sleep Out	Yes												
	Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In	Yes													
Default	<table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><td>C4h</td></tr><tr><td>Power On Sequence</td><td>8Ah/Eah</td></tr><tr><td>S/W Reset</td><td>8Ah/Eah</td></tr><tr><td>H/W Reset</td><td>8Ah/Eah</td></tr></table>		Status	Default Value	C4h	Power On Sequence	8Ah/Eah	S/W Reset	8Ah/Eah	H/W Reset	8Ah/Eah			
	Status	Default Value												
		C4h												
	Power On Sequence	8Ah/Eah												
	S/W Reset	8Ah/Eah												
H/W Reset	8Ah/Eah													
Flow Chart	PWCTR5 ↓ 1st Parameter 2nd parameter Legend Command Parameter Display Action Mode Sequential transfer													

10.2.10 VMCTR (C5h): VCOM Control

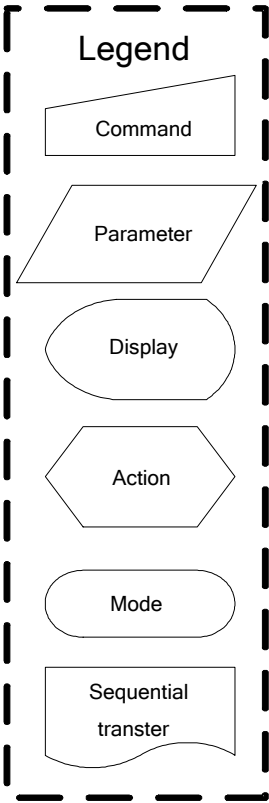
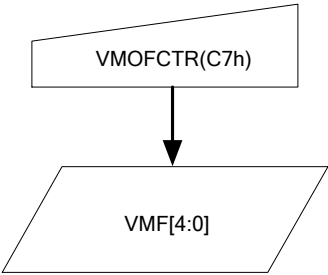
C5H	VMCTR (VCOM Control)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VMCTR1	0	↑	1	-	1	1	0	0	0	1	0	1	(C5h)
1 st parameter	1	↑	1	-	-	-	VCOMS 5	VCOMS 4	VCOMS 3	VCOMS 2	VCOMS 1	VCOMS 0	
Description	VCOM voltage setting.												
		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM		VCOMS [5:0]	VCOM	
	0	000000	-0.425	16	010000	-0.825	32	100000	-1.225	48	110000	-1.625	
	1	000001	-0.450	17	010001	-0.850	33	100001	-1.250	49	110001	-1.650	
	2	000010	-0.475	18	010010	-0.875	34	100010	-1.275	50	110010	-1.675	
	3	000011	-0.500	19	010011	-0.900	35	100011	-1.300	51	110011	-1.700	
	4	000100	-0.525	20	010100	-0.925	36	100100	-1.325	52	110100	-1.725	
	5	000101	-0.550	21	010101	-0.950	37	100101	-1.350	53	110101	-1.750	
	6	000110	-0.575	22	010110	-0.975	38	100110	-1.375	54	110110	-1.775	
	7	000111	-0.600	23	010111	-1.000	39	100111	-1.400	55	110111	-1.800	
	8	001000	-0.625	24	011000	-1.025	40	101000	-1.425	56	111000	-1.825	
	9	001001	-0.650	25	011001	-1.050	41	101001	-1.450	57	111001	-1.850	
	10	001010	-0.675	26	011010	-1.075	42	101010	-1.475	58	111010	-1.875	
	11	001011	-0.700	27	011011	-1.100	43	101011	-1.500	59	111011	-1.900	
	12	001100	-0.725	28	011100	-1.125	44	101100	-1.525	60	111100	-1.925	
	13	001101	-0.750	29	011101	-1.150	45	101101	-1.550	61	111101	-1.950	
	14	001110	-0.775	30	011110	-1.175	46	101110	-1.575	62	111110	-1.975	
	15	001111	-0.800	31	011111	-1.200	47	101111	-1.600	63	111111	-2.000	
Register Availability	Status						Availability						
	Normal Mode On, Idle Mode Off, Sleep Out						Yes						
	Normal Mode On, Idle Mode On, Sleep Out						Yes						
	Partial Mode On, Idle Mode Off, Sleep Out						Yes						
	Partial Mode On, Idle Mode On, Sleep Out						Yes						
	Sleep In						Yes						
Default	Status						Default Value						
							C5h						
	Power On Sequence												
	S/W Reset												
	H/W Reset												



10.2.11 VMOFCTR (C7h): VCOM Offset Control

C7H	VMOFCTR (VCOM Offset Control)																																																																																										
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																														
VMOFCTR	0	↑	1	-	1	1	0	0	0	1	1	1	(C7h)																																																																														
Parameter	1	↑	1	-	-	-	-	VMF4	VMF3	VMF2	VMF1	VMF0																																																																															
Description	-Set VCOM Voltage level for reduce the flicker issue																																																																																										
	<table><tr><th>VMF[4]</th><th>VMF[3:0]</th><th>VCOM Output Level</th></tr><tr><td>0</td><td>0000</td><td>“VCOMS”+16d</td></tr><tr><td>0</td><td>0001</td><td>“VCOMS”+15d</td></tr><tr><td>0</td><td> </td><td> </td></tr><tr><td>0</td><td>1110</td><td>“VCOMS”+2d</td></tr><tr><td>0</td><td>1111</td><td>“VCOMS”+1d</td></tr><tr><td>1</td><td>0000</td><td>“VCOMS”</td></tr><tr><td>1</td><td>0001</td><td>“VCOMS”-1d</td></tr><tr><td>1</td><td>0010</td><td>“VCOMS”-2d</td></tr><tr><td>1</td><td> </td><td> </td></tr><tr><td>1</td><td>1110</td><td>“VCOMS”-14d</td></tr><tr><td>1</td><td>1111</td><td>“VCOMS”-15d</td></tr></table>													VMF[4]	VMF[3:0]	VCOM Output Level	0	0000	“VCOMS”+16d	0	0001	“VCOMS”+15d	0			0	1110	“VCOMS”+2d	0	1111	“VCOMS”+1d	1	0000	“VCOMS”	1	0001	“VCOMS”-1d	1	0010	“VCOMS”-2d	1			1	1110	“VCOMS”-14d	1	1111	“VCOMS”-15d																																										
	VMF[4]	VMF[3:0]	VCOM Output Level																																																																																								
	0	0000	“VCOMS”+16d																																																																																								
	0	0001	“VCOMS”+15d																																																																																								
	0																																																																																										
	0	1110	“VCOMS”+2d																																																																																								
	0	1111	“VCOMS”+1d																																																																																								
	1	0000	“VCOMS”																																																																																								
	1	0001	“VCOMS”-1d																																																																																								
	1	0010	“VCOMS”-2d																																																																																								
	1																																																																																										
	1	1110	“VCOMS”-14d																																																																																								
	1	1111	“VCOMS”-15d																																																																																								
	- 1d=25mV, 2d=50mV 3d=75mv....																																																																																										
Register Availability	<table><tr><th colspan="9">Status</th><th colspan="4">Availability</th></tr><tr><td colspan="9">Normal Mode On, Idle Mode Off, Sleep Out</td><td colspan="4">Yes</td></tr><tr><td colspan="9">Normal Mode On, Idle Mode On, Sleep Out</td><td colspan="4">Yes</td></tr><tr><td colspan="9">Partial Mode On, Idle Mode Off, Sleep Out</td><td colspan="4">Yes</td></tr><tr><td colspan="9">Partial Mode On, Idle Mode On, Sleep Out</td><td colspan="4">Yes</td></tr><tr><td colspan="9">Sleep In</td><td colspan="4">Yes</td></tr></table>													Status									Availability				Normal Mode On, Idle Mode Off, Sleep Out									Yes				Normal Mode On, Idle Mode On, Sleep Out									Yes				Partial Mode On, Idle Mode Off, Sleep Out									Yes				Partial Mode On, Idle Mode On, Sleep Out									Yes				Sleep In									Yes			
	Status									Availability																																																																																	
	Normal Mode On, Idle Mode Off, Sleep Out									Yes																																																																																	
	Normal Mode On, Idle Mode On, Sleep Out									Yes																																																																																	
	Partial Mode On, Idle Mode Off, Sleep Out									Yes																																																																																	
	Partial Mode On, Idle Mode On, Sleep Out									Yes																																																																																	
Sleep In									Yes																																																																																		
Default	<table><tr><th rowspan="2">Status</th><th colspan="12">Default Value</th></tr><tr><th colspan="12">C7h</th></tr><tr><td>Power On Sequence</td><td colspan="12">10h</td></tr><tr><td>S/W Reset</td><td colspan="12">10h</td></tr><tr><td>H/W Reset</td><td colspan="12">10h</td></tr></table>													Status	Default Value												C7h												Power On Sequence	10h												S/W Reset	10h												H/W Reset	10h																									
	Status	Default Value																																																																																									
		C7h																																																																																									
	Power On Sequence	10h																																																																																									
	S/W Reset	10h																																																																																									
H/W Reset	10h																																																																																										

Flow Chart



10.2.12 NVFCTR1 (D7h): NVM Enable Command

D7H	NVFCTR1 (NV Memory Function Controller 1)												
Inst / Para	D/C X	WR X	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR1	0	↑	1	-	1	1	0	1	0	1	1	1	(D7h)
1 st parameter	1	↑	1	-	0	1	1	1	0	1	1	1	(77h)
2 nd parameter	1	↑	1	-	0	0	1	1	0	1	0	1	(35h)
3 rd parameter	1	↑	1	-	1	1	1	0	1	1	1	0	(Eeh)
4 th parameter	1	↑	1	-	VPPINTMD	0	0	0	0	NV_EN	0	0	
Description	- NV_EN=0, NVM can not be programmed; NV_EN=1, NVM can be programmed. -VPPINTMD=0, Use external VPP=7.5V; VPPINTMD=1, Use internal VPP.												
Flow Chart	NVFCTR1(D7h) ↓ 77h 35h EEh 4th parameter Legend Command Parameter Display Action Mode Sequential transfer												

10.2.13 NVFCTR2 (D8h): Set Address for NVM

D8H	NVFCTR2 (NV Memory Function Controller 2)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR2	0	↑	1	-	1	1	0	1	1	0	0	0	(D8h)
Parameter	1	↑	1	-	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	-
Description	-AD[7:0]: set address for NVM programming.												
Flow Chart	NVFCTR2(D8h) ↓ AD[7:0] Legend Command Parameter Display Action Mode Sequential transfer												

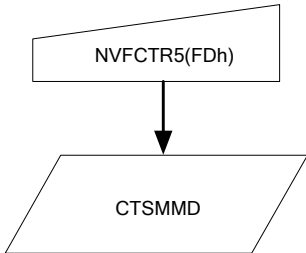
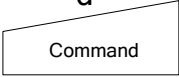
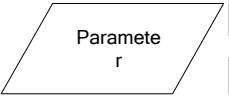
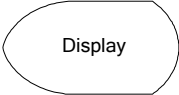
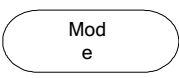
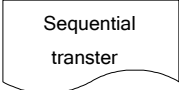
10.2.14 NVFCTR3 (D9h): Set Data for NVM

D9H	NVFCTR3 (NV Memory Function Controller 3)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR3	0	↑	1	-	1	1	0	0	1	0	0	1	(D9h)
Parameter	1	↑	1	-	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
Description	-PD[7:0]: set data for NVM programming.												
Flow Chart	<pre> graph TD A[NVFCTR3(D9h)] --> B[/PD[7:0]/] </pre> Legend												

10.2.15 NVFCTR4 (DFh): NVM Write Command

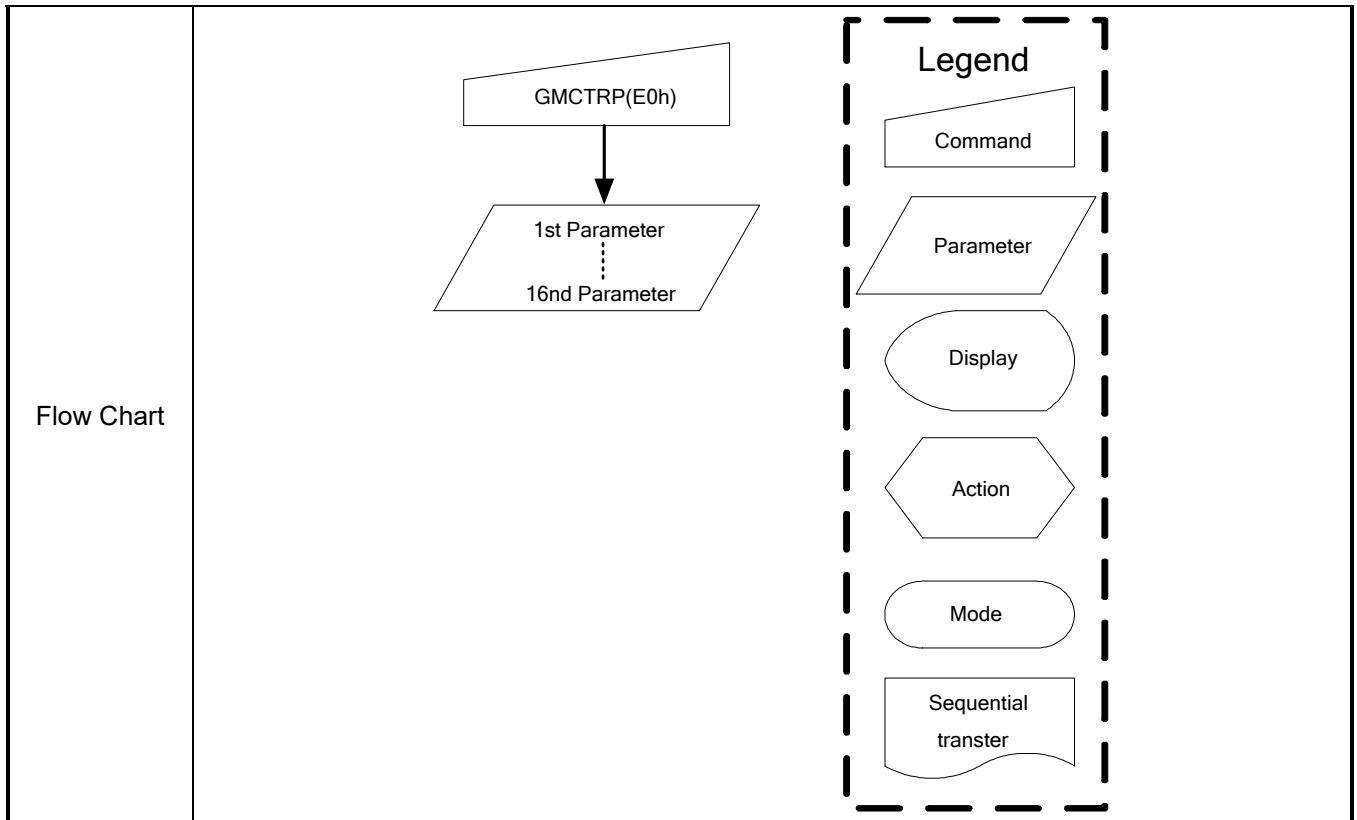
DFH	NVFCTR1 (NV Memory Function Controller 4)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR4	0	↑	1	-	1	1	0	1	1	1	1	1	(DFh)
Parameter	1	↑	1	-	NVM_CMD7	NVM_CMD6	NVM_CMD5	NVM_CMD4	NVM_CMD3	NVM_CMD2	NVM_CMD1	NVM_CMD0	
Description	-NVM Write Command -NVM_CMD[7:0] : Program command : CAh NOTE: “-” Don't care												
Flow Chart	<pre> graph TD A[NVFCTR4(DFh)] --> B[/CAh/] </pre> Legend - Command - Parameter - Display - Action - Mode - Sequential transfer												

10.2.16 NVFCTR5 (FDh): Custom Mode Enable Command

FDH	NVCTR5 (NV Memory Function Controller 5)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NVFCTR5	0	↑	1	-	1	1	0	1	1	1	1	1	(FDh)
Parameter	1	↑	1	-	0	1	1	0	CTSMMD	0	0	0	
Description	-Custom Mode Enable Command CTSMMD=0,custom mode off ; CTSMMD=1, custom mode on.												
Flow Chart	 <pre> graph TD A[NVFCTR5(FDh)] --> B[CTSMMD] </pre> Legend  Command  Parameter  Display  Action  Mode  Sequential transfer												

10.2.17 GMCTRP (E0h): Gamma ('+'polarity) Correction Characteristics Setting

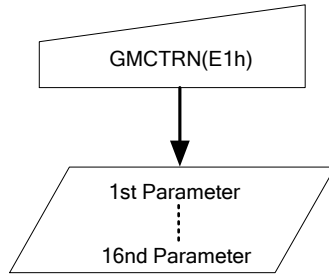
E0H	GMCTRP (Gamma '+'Polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GMCTRP	0	↑	1	-	1	1	1	0	0	0	0	0	(E0h)
1 st Parameter	1	↑	1	-	-	-	VRF0P[5]	VRF0P[4]	VF0P[3]	VRF0P[2]	VRF0P[1]	VRF0P[0]	
2 nd Parameter	1	↑	1	-	-	-	VOS0P[5]	VOS0P[4]	VOS0P[3]	VOS0P[2]	VOS0P[1]	VOS0P[0]	
3 rd Parameter	1	↑	1	-	-	-	PK0P[5]	PK0P[4]	PK0P[3]	PK0P[2]	PK0P[1]	PK0P[0]	
4 th Parameter	1	↑	1	-	-	-	PK1P[5]	PK1P[4]	PK1P[3]	PK1P[2]	PK1P[1]	PK1P[0]	
5 th Parameter	1	↑	1	-	-	-	PK2P[5]	PK2P[4]	PK2P[3]	PK2P[2]	PK2P[1]	PK2P[0]	
6 th Parameter	1	↑	1	-	-	-	PK3P[5]	PK3P[4]	PK3P[3]	PK3P[2]	PK3P[1]	PK3P[0]	
7 th Parameter	1	↑	1	-	-	-	PK4P[5]	PK4P[4]	PK4P[3]	PK4P[2]	PK4P[1]	PK4P[0]	
8 th Parameter	1	↑	1	-	-	-	PK5P[5]	PK5P[4]	PK5P[3]	PK5P[2]	PK5P[1]	PK5P[0]	
9 th Parameter	1	↑	1	-	-	-	PK6P[5]	PK6P[4]	PK6P[3]	PK6P[2]	PK6P[1]	PK6P[0]	
10 th Parameter	1	↑	1	-	-	-	PK7P[5]	PK7P[4]	PK7P[3]	PK7P[2]	PK7P[1]	PK7P[0]	
11 th Parameter	1	↑	1	-	-	-	PK8P[5]	PK8P[4]	PK8P[3]	PK8P[2]	PK8P[1]	PK8P[0]	
12 th Parameter	1	↑	1	-	-	-	PK9P[5]	PK9P[4]	PK9P[3]	PK9P[2]	PK9P[1]	PK9P[0]	
13 th Parameter	1	↑	1	-	-	-	SELV0P[5]	SELV0P[4]	SELV0P[3]	SELV0P[2]	SELV0P[1]	SELV0P[0]	
14 th Parameter	1	↑	1	-	-	-	SELV1P[5]	SELV1P[4]	SELV1P[3]	SELV1P[2]	SELV1P[1]	SELV1P[0]	
15 th Parameter	1	↑	1	-	-	-	SELV62P[5]	SELV62P[4]	SELV62P[3]	SELV62P[2]	SELV62P[1]	SELV62P[0]	
16 th Parameter	1	↑	1	-	-	-	SELV63P[5]	SELV63P[4]	SELV63P[3]	SELV63P[2]	SELV63P[1]	SELV63P[0]	
Description	Register Group		Positive Polarity		Set-up Contents								
	High Level adjustment		VRF0P[5:0]		Variable resistor VRHP								
	Mid Level Adjustment		SELV0P[5:0]		The voltage of V0 grayscale is selected by the 64 to 1								
			SELV1P[5:0]		The voltage of V1 grayscale is selected by the 64 to 1								
			PK0P[5:0]		The voltage of V3 grayscale is selected by the 64 to 1								
			PK1P[5:0]		The voltage of V4 grayscale is selected by the 64 to 1								
			PK2P[5:0]		The voltage of V12 grayscale is selected by the 64 to 1								
			PK3P[5:0]		The voltage of V20 grayscale is selected by the 64 to 1								
			PK4P[5:0]		The voltage of V28 grayscale is selected by the 64 to 1								
			PK5P[5:0]		The voltage of V36 grayscale is selected by the 64 to 1								
			PK6P[5:0]		The voltage of V44 grayscale is selected by the 64 to 1								
			PK7P[5:0]		The voltage of V52 grayscale is selected by the 64 to 1								
			PK8P[5:0]		The voltage of V56 grayscale is selected by the 64 to 1								
			PK9P[5:0]		The voltage of V60 grayscale is selected by the 64 to 1								
			SELV62P[5:0]		The voltage of V62 grayscale is selected by the 64 to 1								
			SELV63P[5:0]		The voltage of V63 grayscale is selected by the 64 to 1								
	Low Level Adjustment		VOS0P[5:0]		Variable Resistor VRLP								



10.2.18 GMCTRN (E1h): Gamma '-'polarity Correction Characteristics Setting

E1H	GMCTRN (Gamma '+'Polarity Correction Characteristics Setting)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GMCTRN	0	↑	1	-	1	1	1	0	0	0	0	1	(E1h)
1 st Parameter	1	↑	1	-	-	-	VRF0N[5]	VRF0N[4]	VF0N[3]	VRF0N[2]	VRF0N[1]	VRF0N[0]	
2 nd Parameter	1	↑	1	-	-	-	VOS0N[5]	VOS0N[4]	VOS0N[3]	VOS0N[2]	VOS0N[1]	VOS0N[0]	
3 rd Parameter	1	↑	1	-	-	-	PK0N[5]	PK0N[4]	PK0N[3]	PK0N[2]	PK0N[1]	PK0N[0]	
4 th Parameter	1	↑	1	-	-	-	PK1N[5]	PK1N[4]	PK1N[3]	PK1N[2]	PK1N[1]	PK1N[0]	
5 th Parameter	1	↑	1	-	-	-	PK2N[5]	PK2N[4]	PK2N[3]	PK2N[2]	PK2N[1]	PK2N[0]	
6 th Parameter	1	↑	1	-	-	-	PK3N[5]	PK3N[4]	PK3N[3]	PK3N[2]	PK3N[1]	PK3N[0]	
7 th Parameter	1	↑	1	-	-	-	PK4N[5]	PK4N[4]	PK4N[3]	PK4N[2]	PK4N[1]	PK4N[0]	
8 th Parameter	1	↑	1	-	-	-	PK5N[5]	PK5N[4]	PK5N[3]	PK5N[2]	PK5N[1]	PK5N[0]	
9 th Parameter	1	↑	1	-	-	-	PK6N[5]	PK6N[4]	PK6N[3]	PK6N[2]	PK6N[1]	PK6N[0]	
10 th Parameter	1	↑	1	-	-	-	PK7N[5]	PK7N[4]	PK7N[3]	PK7N[2]	PK7N[1]	PK7N[0]	
11 th Parameter	1	↑	1	-	-	-	PK8N[5]	PK8N[4]	PK8N[3]	PK8N[2]	PK8N[1]	PK8N[0]	
12 th Parameter	1	↑	1	-	-	-	PK9[5]	PK9N[4]	PK9N[3]	PK9N[2]	PK9N[1]	PK9N[0]	
13 th Parameter	1	↑	1	-	-	-	SELV0N[5]	SELV0N[4]	SELV0N[3]	SELV0N[2]	SELV0N[1]	SELV0N[0]	
14 th Parameter	1	↑	1	-	-	-	SELV1N[5]	SELV1N[4]	SELV1N[3]	SELV1N[2]	SELV1N[1]	SELV1N[0]	
15 th Parameter	1	↑	1	-	-	-	SELV62N[5]	SELV62N[4]	SELV62N[3]	SELV62N[2]	SELV62N[1]	SELV62N[0]	
16 th Parameter	1	↑	1	-	-	-	SELV63N[5]	SELV63N[4]	SELV63N[3]	SELV63N[2]	SELV63N[1]	SELV63N[0]	
Description	Register Group		Negative Polarity		Set-up Contents								
	High level adjustment		VRF0N[5:0]		Variable resistor VRHN								
	Mid Level Adjustment		SELV0N[5:0]		The voltage of V0 grayscale is selected by the 64 to 1								
			SELV1N[5:0]		The voltage of V1 grayscale is selected by the 64 to 1								
			PK0N[5:0]		The voltage of V3 grayscale is selected by the 64 to 1								
			PK1N[5:0]		The voltage of V4 grayscale is selected by the 64 to 1								
			PK2N[5:0]		The voltage of V12 grayscale is selected by the 64 to 1								
			PK3N[5:0]		The voltage of V20 grayscale is selected by the 64 to 1								
			PK4N[5:0]		The voltage of V28 grayscale is selected by the 64 to 1								
			PK5N[5:0]		The voltage of V36 grayscale is selected by the 64 to 1								
			PK6N[5:0]		The voltage of V44 grayscale is selected by the 64 to 1								
			PK7N[5:0]		The voltage of V52 grayscale is selected by the 64 to 1								
			PK8N[5:0]		The voltage of V56 grayscale is selected by the 64 to 1								
			PK9N[5:0]		The voltage of V60 grayscale is selected by the 64 to 1								
			SELV62N[5:0]		The voltage of V62 grayscale is selected by the 64 to 1								
			SELV63N[5:0]		The voltage of V63 grayscale is selected by the 64 to 1								
	Low Level Adjustment		VOS0N[5:0]		Variable Resistor VRLN								

Flow Chart



Legend

Command

Parameter

Display

Action

Mode

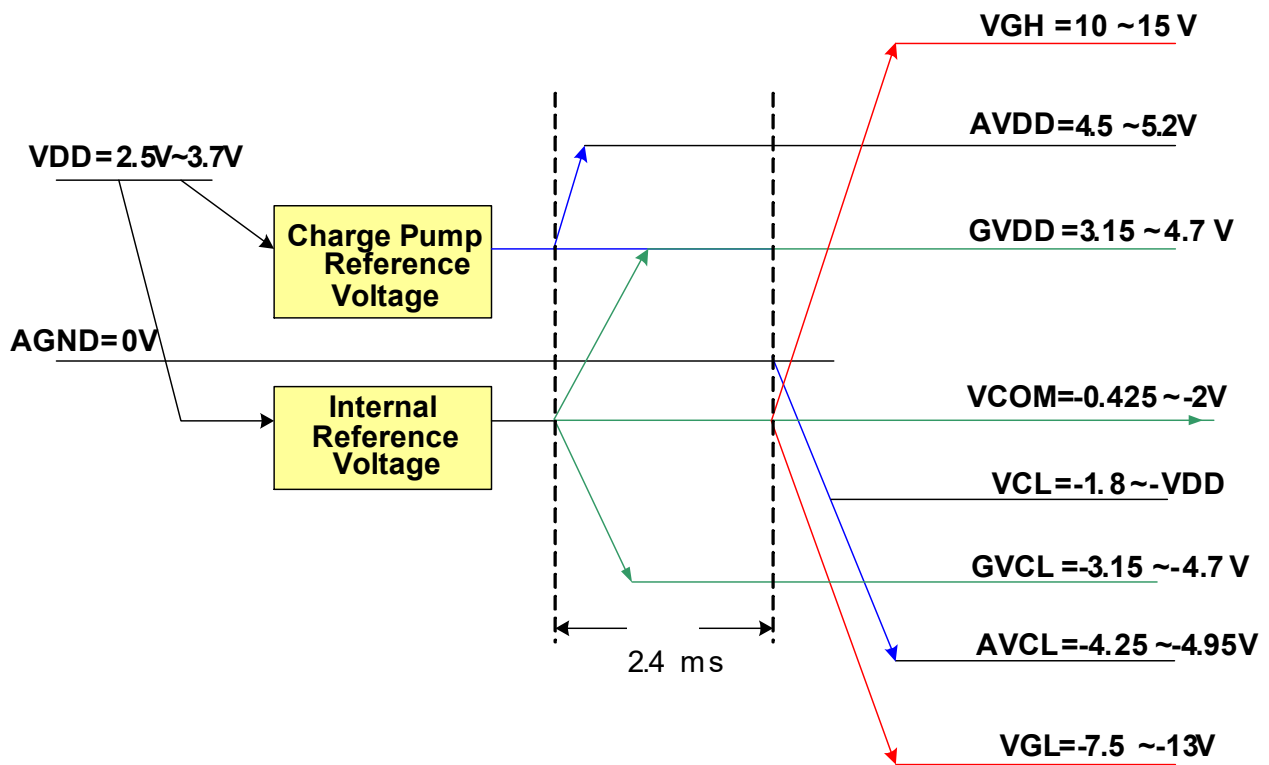
Sequential
transfer

10.2.19 GCV(FCh): Gate Pump Clock Frequency Variable

FCH	Gate Pump Clock Frequency Variable																						
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
NVFCTR1	0	↑	1	-	1	1	0	1	1	0	0	1	(FCh)										
Parameter	1	1	↑	-	GCV_Enable1	GCV_Enable0	0	0	Clk_Variable1	Clk_Variable0	0	0											
Description	-Automatic adjust gate pumping clock for saving power consumption.																						
	<table><tr><th>GCV_Enable[1:0]</th><th>Gate Pump Clock Frequency</th></tr><tr><td>00</td><td>Reserved</td></tr><tr><td>01</td><td>Reserved</td></tr><tr><td>10</td><td>Disable</td></tr><tr><td>11</td><td>Enable</td></tr></table>													GCV_Enable[1:0]	Gate Pump Clock Frequency	00	Reserved	01	Reserved	10	Disable	11	Enable
	GCV_Enable[1:0]	Gate Pump Clock Frequency																					
	00	Reserved																					
	01	Reserved																					
	10	Disable																					
	11	Enable																					
	<table><tr><th>Clk_Variable[1:0]</th><th>Save Power Ability</th></tr><tr><td>00</td><td>Small</td></tr><tr><td>01</td><td>Medium</td></tr><tr><td>10</td><td>High</td></tr><tr><td>11</td><td>Large</td></tr></table>													Clk_Variable[1:0]	Save Power Ability	00	Small	01	Medium	10	High	11	Large
	Clk_Variable[1:0]	Save Power Ability																					
	00	Small																					
01	Medium																						
10	High																						
11	Large																						
Default	<table><tr><th>Status</th><th>Default Value (FCh)</th></tr><tr><td>Power On Sequence</td><td></td></tr><tr><td>S/W Reset</td><td></td></tr><tr><td>H/W Reset</td><td></td></tr></table>													Status	Default Value (FCh)	Power On Sequence		S/W Reset		H/W Reset			
	Status	Default Value (FCh)																					
	Power On Sequence																						
	S/W Reset																						
	H/W Reset																						
Flow Chart	GCV(FCh) ↓ GCV_Enable[1:0] Clk_Variable[1:0] Legend Command Parameter Display Action Mode Sequential transter																						

11 Power Structure

11.1 Driver IC Operating Voltage Specification

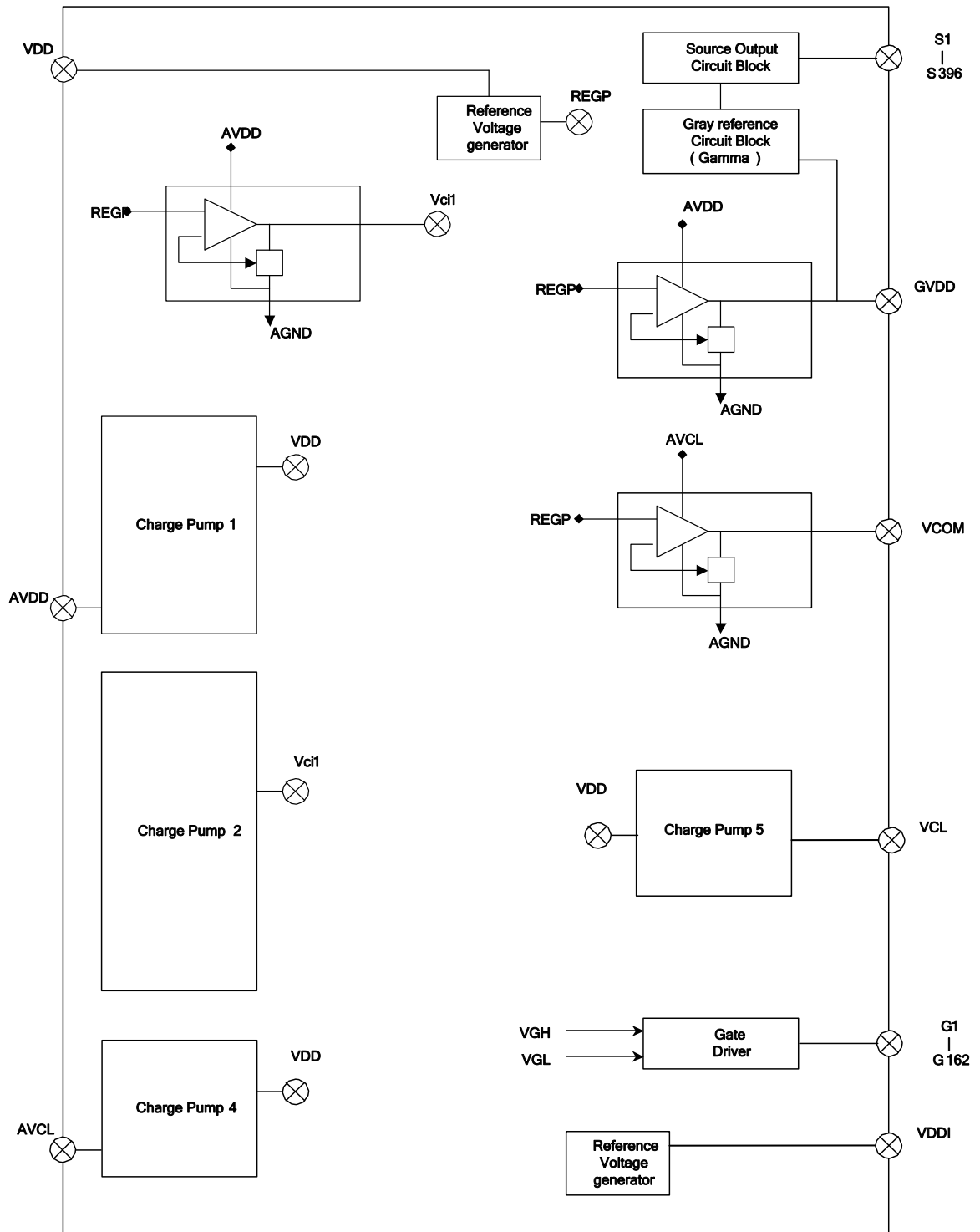


Note:

Sleep out flow: $AVDD$, $GVDD$, $GVCL$, $VCOM$ switch on $\rightarrow 2.4ms \rightarrow AVCL$, VGH , VGL , VCL switch on $\rightarrow 78.6ms \rightarrow$ scan 2 blank frames

Sleep in flow: Scan 2 blank frames $\rightarrow$ All analog power

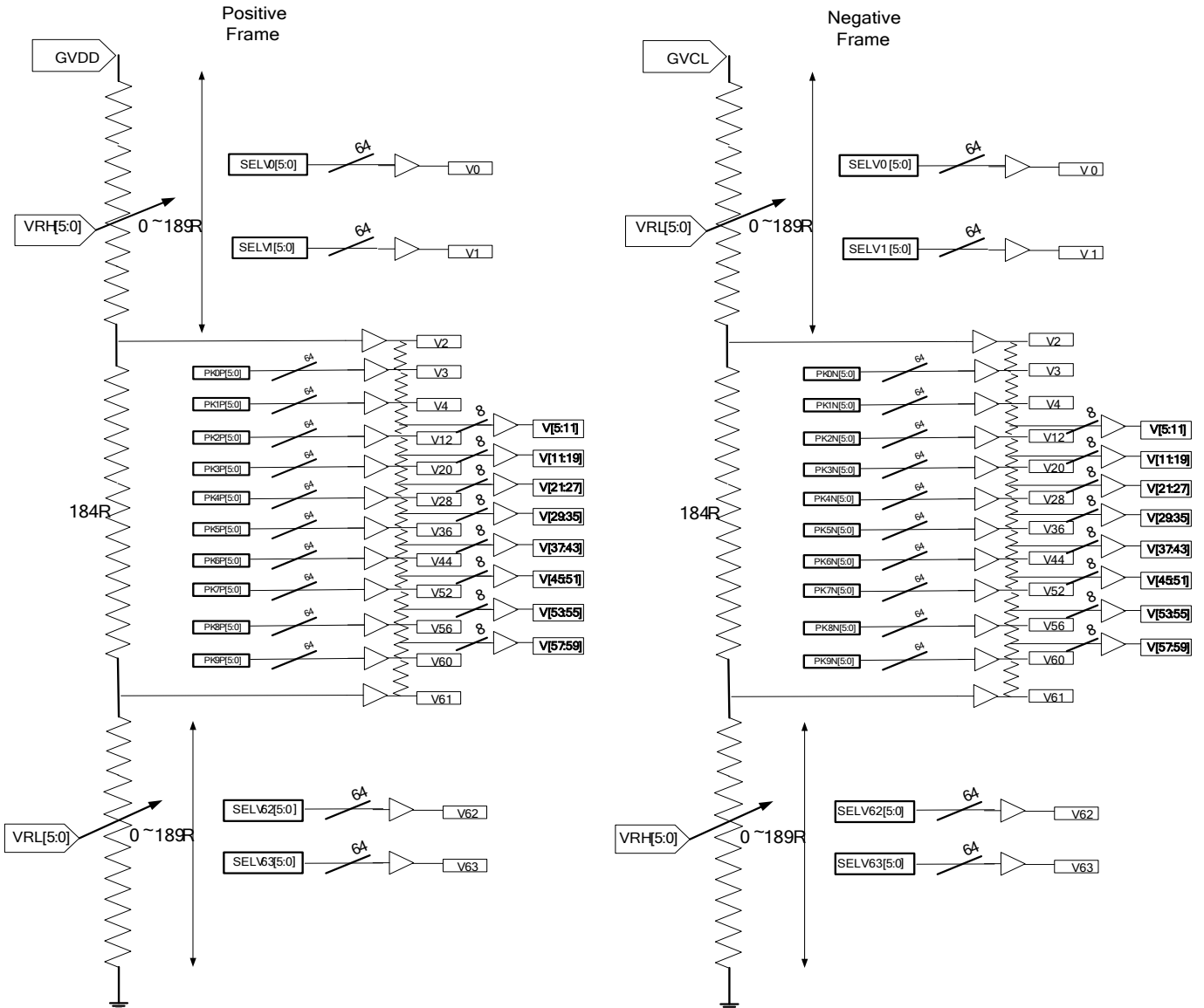
11.2 Power Booster Circuit



12 Gamma Structure

12.1 Structure of Grayscale Amplifier

16 voltage levels (VIN0-VIN15) between GVDD (GVCL) and VSS are determined by the high/ mid/ low level adjustment registers. Each mid-adjustment level is split into 64 levels again by the internal ladder resistor network. As a result, grayscale amplifier generates 64 voltage levels ranging from V0 to V63 and outputs one of 64 levels.



12.2 Gamma Voltage Formula (Positive/ Negative Polarity)

Gray Level	Voltage Formula (Positive)	Voltage Formula (Negative)
0	VINP0	VINP0
1	VINP1	VINP1
2	VINP2	VINP2
3	VINP3	VINP3
4	VINP4	VINP4
5	$V4-(V4-V12)*(4/32)$	$V4-(V4-V12)*(4/32)$
6	$V4-(V4-V12)*(8/32)$	$V4-(V4-V12)*(8/32)$
7	$V4-(V4-V12)*(12/32)$	$V4-(V4-V12)*(12/32)$
8	$V4-(V4-V12)*(16/32)$	$V4-(V4-V12)*(16/32)$
9	$V4-(V4-V12)*(20/32)$	$V4-(V4-V12)*(20/32)$
10	$V4-(V4-V12)*(24/32)$	$V4-(V4-V12)*(24/32)$
11	$V4-(V4-V12)*(28/32)$	$V4-(V4-V12)*(28/32)$
12	VINP5	VINP5
13	$V12-(V12-V20)*(4/32)$	$V12-(V12-V20)*(4/32)$
14	$V12-(V12-V20)*(8/32)$	$V12-(V12-V20)*(8/32)$
15	$V12-(V12-V20)*(12/32)$	$V12-(V12-V20)*(12/32)$
16	$V12-(V12-V20)*(16/32)$	$V12-(V12-V20)*(16/32)$
17	$V12-(V12-V20)*(20/32)$	$V12-(V12-V20)*(20/32)$
18	$V12-(V12-V20)*(24/32)$	$V12-(V12-V20)*(24/32)$
19	$V12-(V12-V20)*(28/32)$	$V12-(V12-V20)*(28/32)$
20	VINP6	VINP6
21	$V20-(V20-V28)*(4/32)$	$V20-(V20-V28)*(4/32)$
22	$V20-(V20-V28)*(8/32)$	$V20-(V20-V28)*(8/32)$
23	$V20-(V20-V28)*(12/32)$	$V20-(V20-V28)*(12/32)$
24	$V20-(V20-V28)*(16/32)$	$V20-(V20-V28)*(16/32)$
25	$V20-(V20-V28)*(20/32)$	$V20-(V20-V28)*(20/32)$
26	$V20-(V20-V28)*(24/32)$	$V20-(V20-V28)*(24/32)$
27	$V20-(V20-V28)*(28/32)$	$V20-(V20-V28)*(28/32)$
28	VINP7	VINP7
29	$V28-(V28-V36)*(4/32)$	$V28-(V28-V36)*(4/32)$
30	$V28-(V28-V36)*(8/32)$	$V28-(V28-V36)*(8/32)$
31	$V28-(V28-V36)*(12/32)$	$V28-(V28-V36)*(12/32)$
32	$V28-(V28-V36)*(16/32)$	$V28-(V28-V36)*(16/32)$
33	$V28-(V28-V36)*(20/32)$	$V28-(V28-V36)*(20/32)$
34	$V28-(V28-V36)*(24/32)$	$V28-(V28-V36)*(24/32)$
35	$V28-(V28-V36)*(28/32)$	$V28-(V28-V36)*(28/32)$

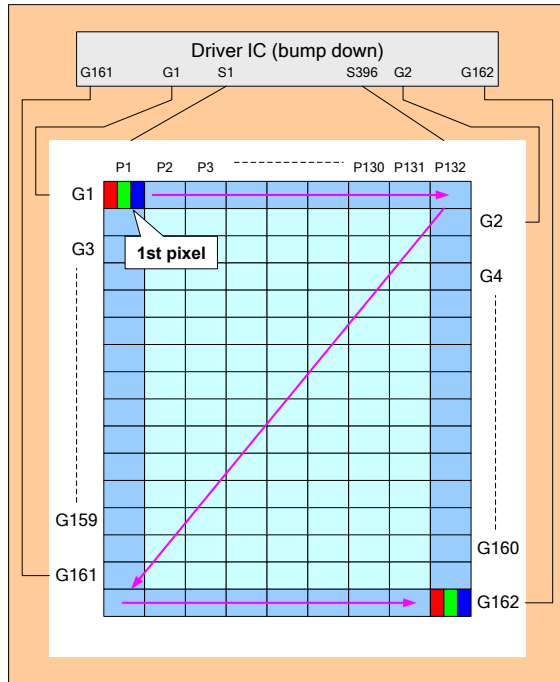
36	VINP8	VINP8
37	V36-(V36-V44)*(4/32)	V36-(V36-V44)*(4/32)
38	V36-(V36-V44)*(8/32)	V36-(V36-V44)*(8/32)
39	V36-(V36-V44)*(12/32)	V36-(V36-V44)*(12/32)
40	V36-(V36-V44)*(16/32)	V36-(V36-V44)*(16/32)
41	V36-(V36-V44)*(20/32)	V36-(V36-V44)*(20/32)
42	V36-(V36-V44)*(24/32)	V36-(V36-V44)*(24/32)
43	V36-(V36-V44)*(28/32)	V36-(V36-V44)*(28/32)
44	VINP9	VINP9
45	V44-(V44-V52)*(4/32)	V44-(V44-V52)*(4/32)
46	V44-(V44-V52)*(8/32)	V44-(V44-V52)*(8/32)
47	V44-(V44-V52)*(12/32)	V44-(V44-V52)*(12/32)
48	V44-(V44-V52)*(16/32)	V44-(V44-V52)*(16/32)
49	V44-(V44-V52)*(20/32)	V44-(V44-V52)*(20/32)
50	V44-(V44-V52)*(24/32)	V44-(V44-V52)*(24/32)
51	V44-(V44-V52)*(28/32)	V44-(V44-V52)*(28/32)
52	VINP10	VINP10
53	V52-(V52-V56)*(1/4)	V52-(V52-V56)*(1/4)
54	V52-(V52-V56)*(2/4)	V52-(V52-V56)*(2/4)
55	V52-(V52-V56)*(3/4)	V52-(V52-V56)*(3/4)
56	VINP11	VINP11
57	V56-(V56-V60)*(1/4)	V56-(V56-V60)*(1/4)
58	V56-(V56-V60)*(2/4)	V56-(V56-V60)*(2/4)
59	V56-(V56-V60)*(3/4)	V56-(V56-V60)*(3/4)
60	VINP12	VINP12
61	VINP13	VINP13
62	VINP14	VINP14
63	VINP15	VINP15

13 Example Connection with Panel Direction and Different Resolution

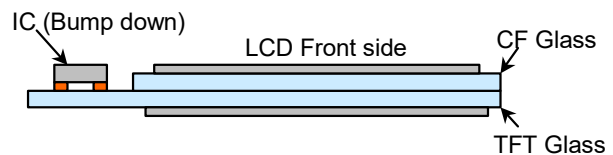
13.1 Application of Connection with Panel Direction

Case 1: (This is default case)

- 1st Pixel is at Left Top of the panel
- RGB Filter Order = RGB

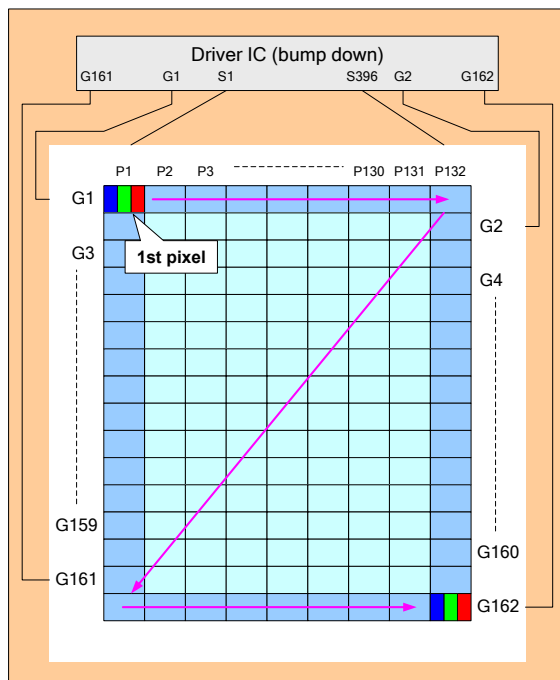


- Direction default setting (H/W)
- SMX = '0'
- SMY = '0'
- SRGB = '0'
- S1 = Filter R
- S2 = Filter G
- S3 = Filter B
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

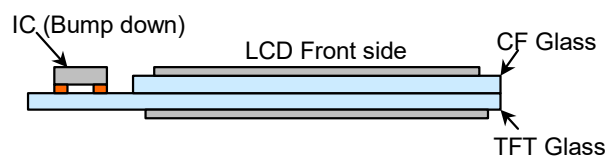


Case 2:

- 1st Pixel is at Left Top of the panel
- RGB Filter Order = BGR

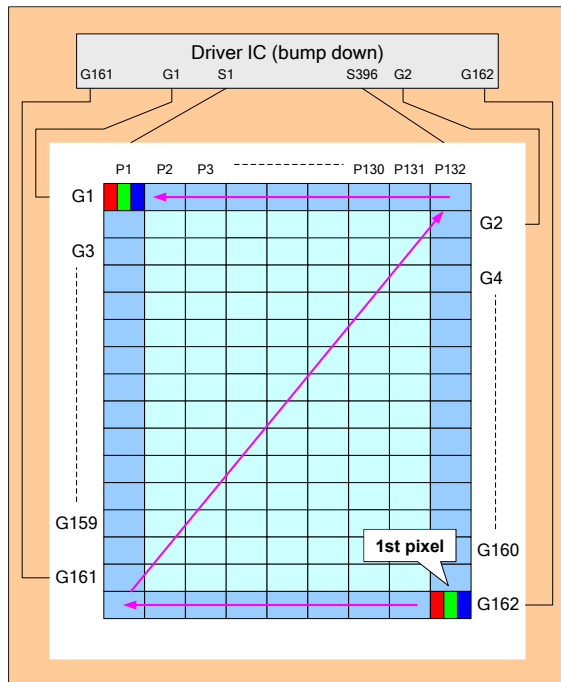


- Direction default setting (H/W)
- SMX = '0'
- SMY = '0'
- SRGB = '1'
- S1 = Filter B
- S2 = Filter G
- S3 = Filter R
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

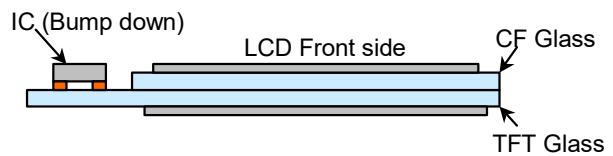


Case 3:

- 1st Pixel is at Right Bottom of the panel
- RGB Filter Order = RGB

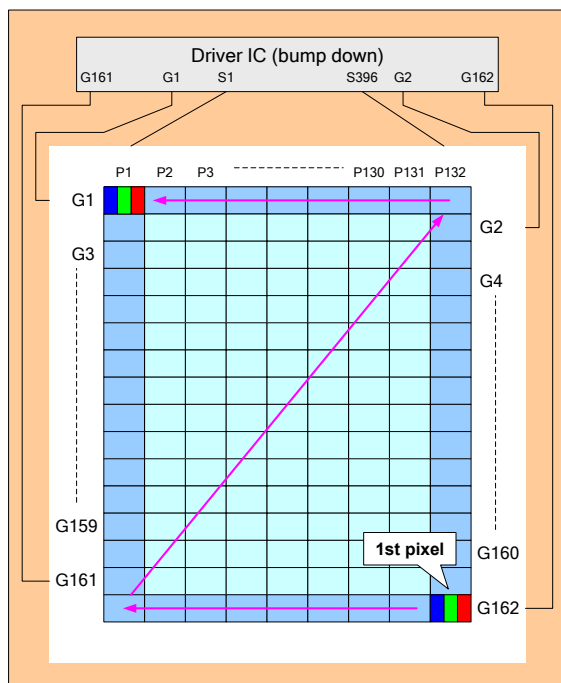


- Direction default setting (H/W)
- SMX = '1'
- SMY = '1'
- SRGB = '0'
- S1 = Filter **R**
- S2 = Filter **G**
- S3 = Filter **B**
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV

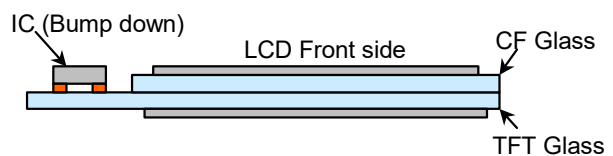


Case 4:

- 1st Pixel is at Right Bottom of the panel
- RGB Filter Order = BGR



- Direction default setting (H/W)
- SMX = '1'
- SMY = '1'
- SRGB = '1'
- S1 = Filter **B**
- S2 = Filter **G**
- S3 = Filter **R**
- Display direction control (S/W)
- X-Mirror control by MX
- Y-Mirror control by MY
- XY-Exchange control by MV



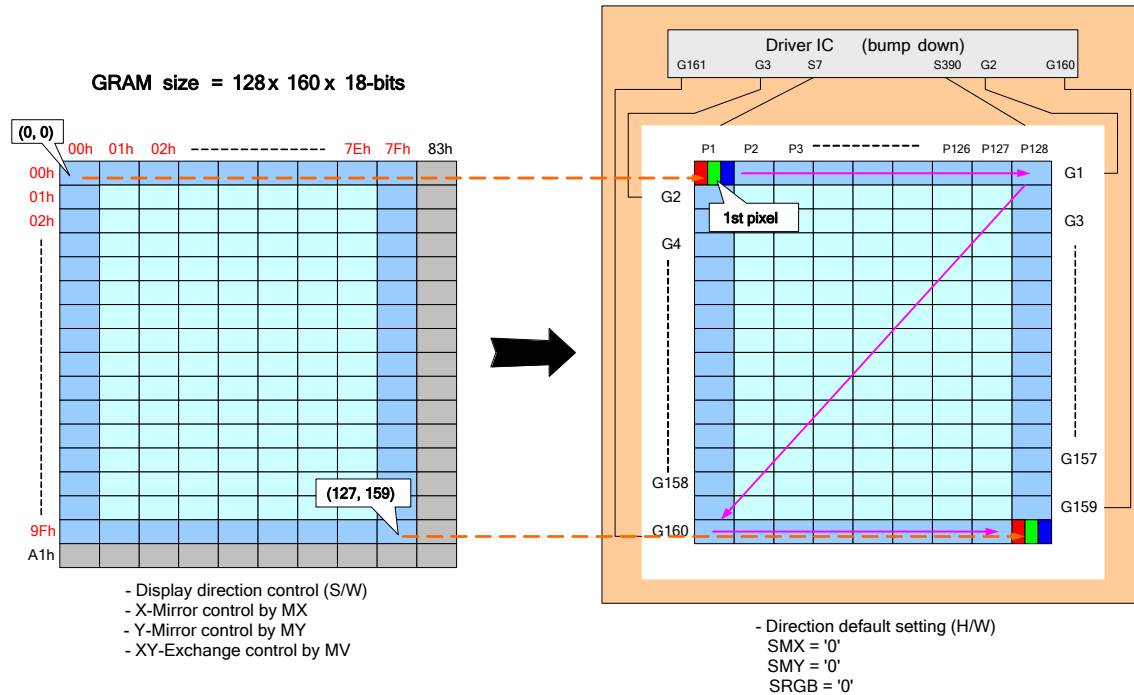
13.2 Application of Connection with Different Resolution

Case1 of Resolution (128RGB x 160) (GM [1:0] = "11")

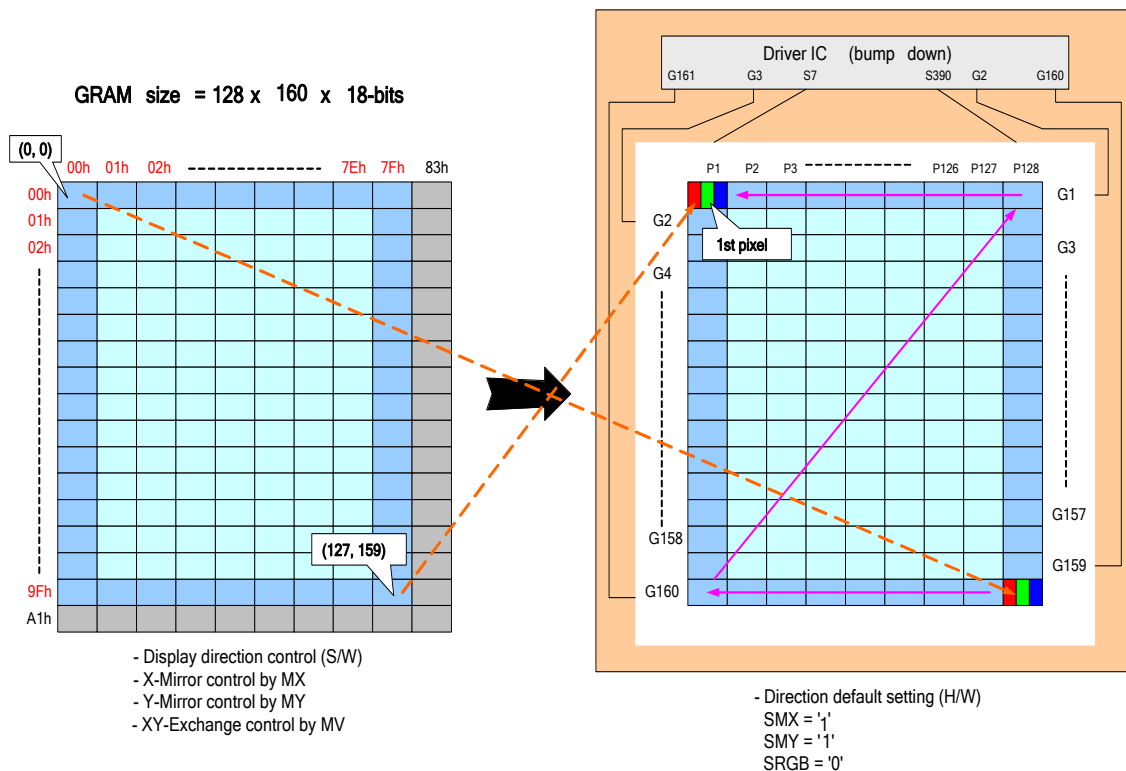
RAM Size=128 x 160 x 18-bit (Used)

Display Size = 128RGB x 160

1). Example for SMX=SMY='0'



2). Example for SMX=SMY='1'

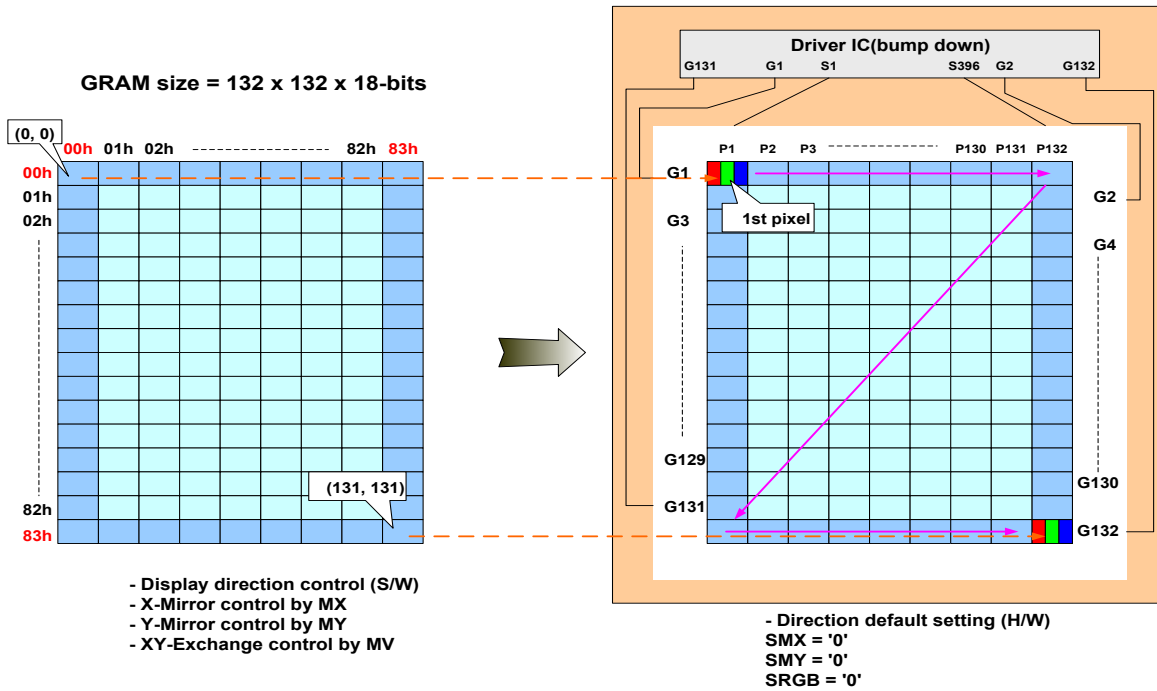


Case2 of Resolution (132RGB x 132) (GM [1:0] = "01")

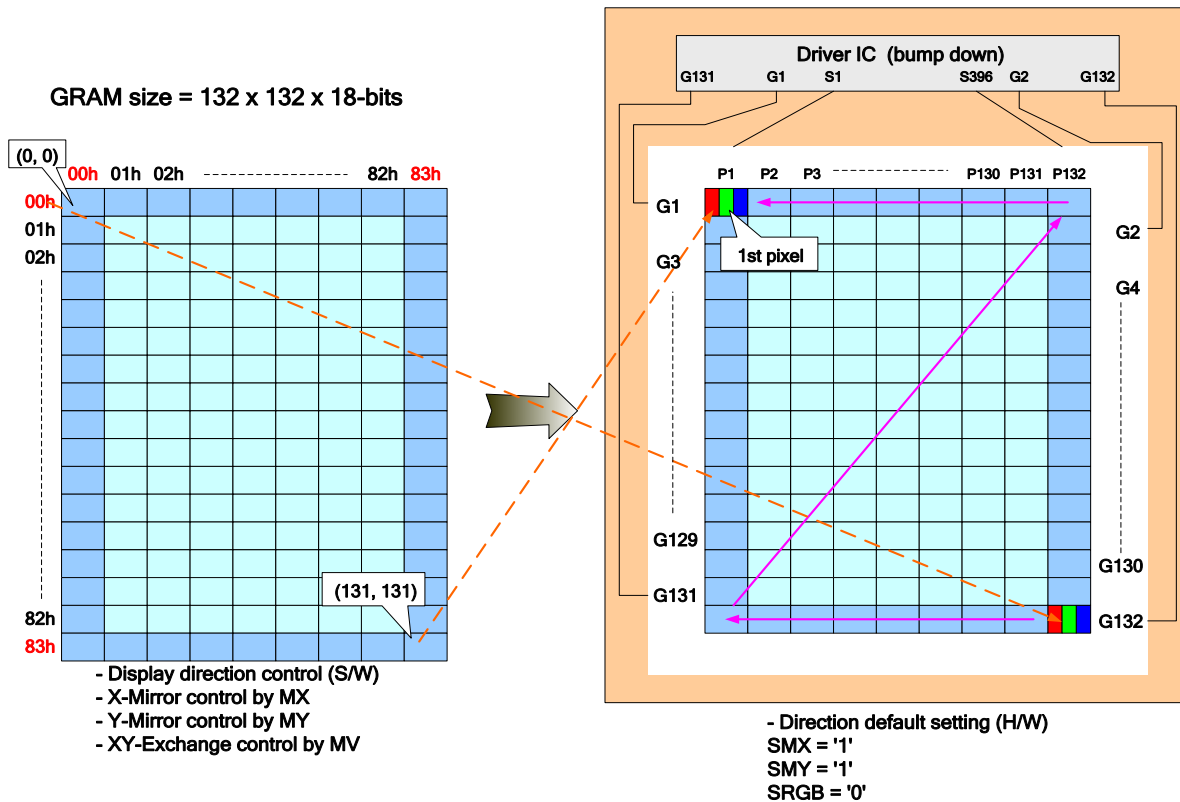
RAM size=132 x 132 x 18-bit (Used)

Display size = 132RGB x 132

1). Example for SMX=SMY='0'



2). Example for SMX=SMY='1'

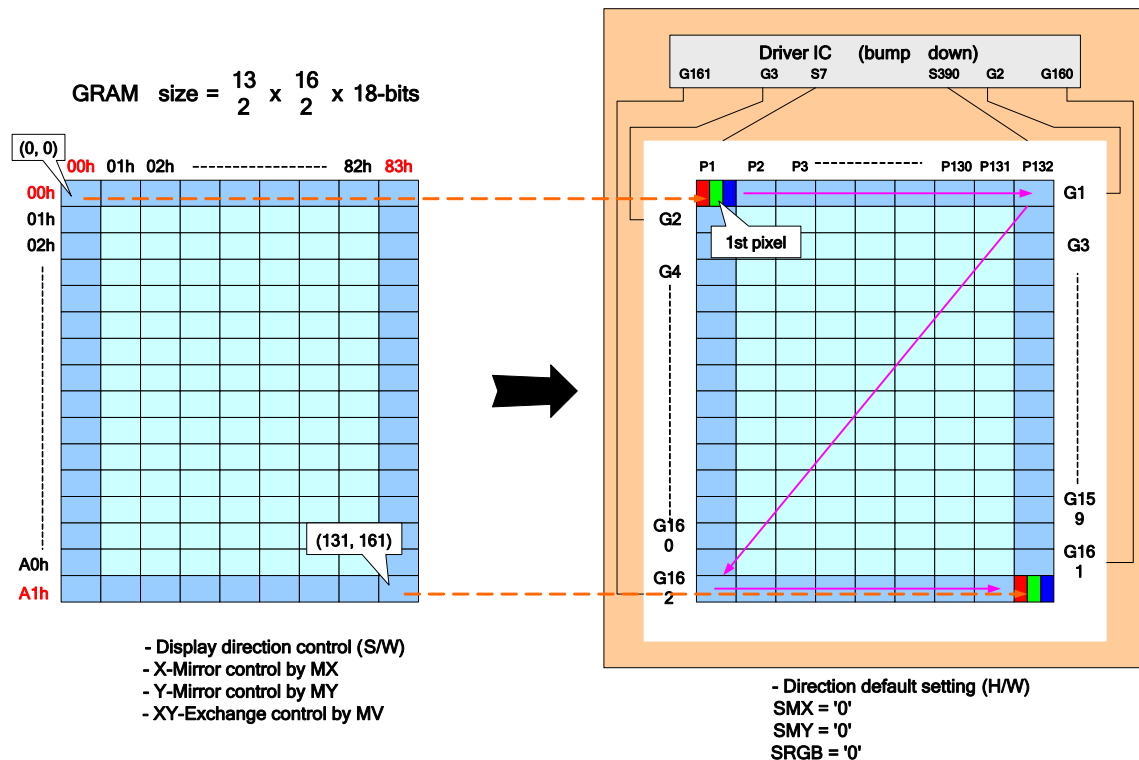


Case3 of Resolution (132RGB x 162) (GM [1:0] = "00")

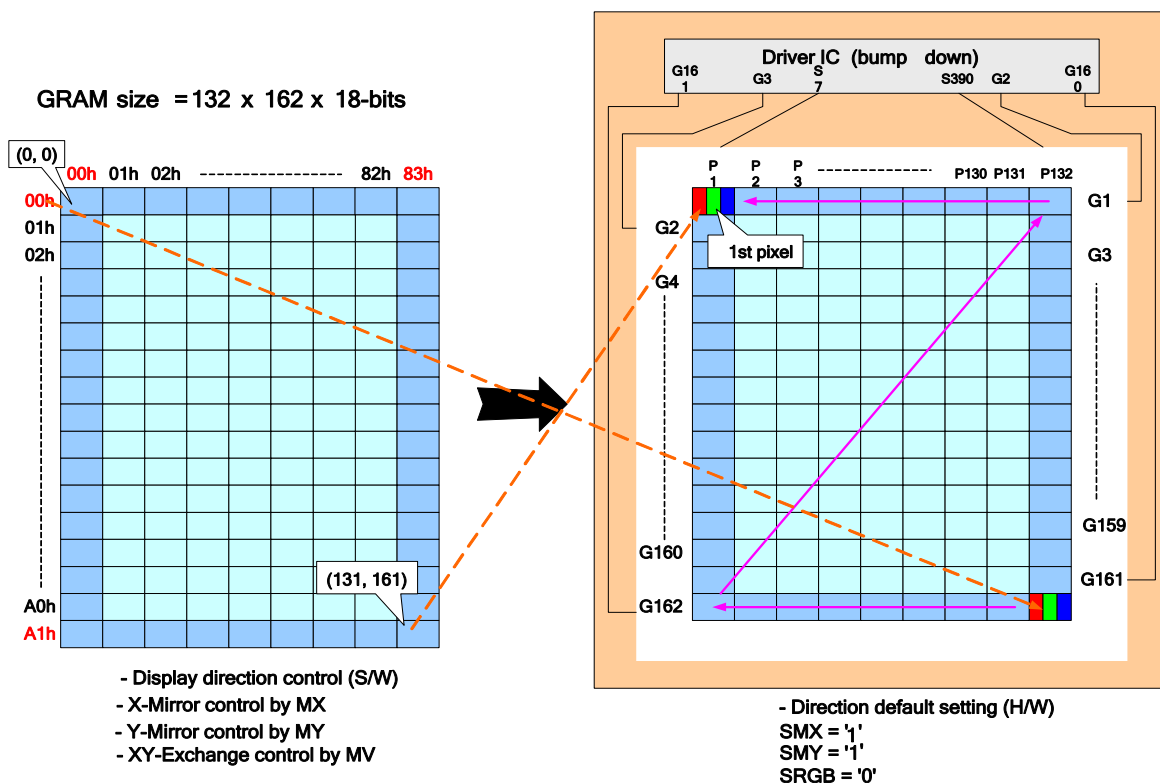
RAM Size=132 x 162 x 18-bit (Used)

Display Size = 132RGB x 162

1). Example for SMX=SMY='0'



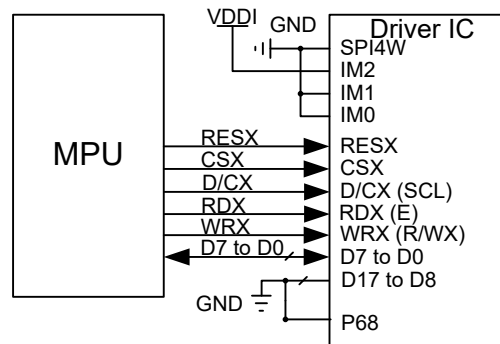
2). Example for SMX=SMY='1'



13.3 Microprocessor Interface Applications

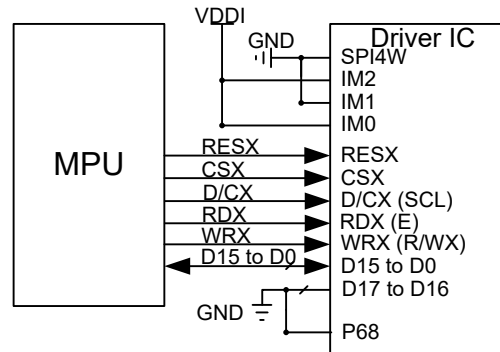
13.3.1 8080-Series MCU Interface for 8-bit Data Bus (P68=0, IM2, IM1, IM0="100")

80 Serial MPU 8-Bit Bus



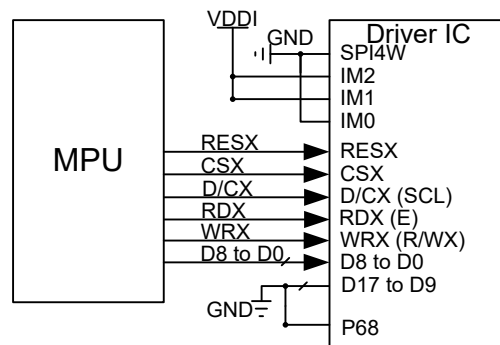
13.3.2 8080-Series MCU Interface for 16-bit Data Bus (P68=0, IM2, IM1, IM0="101")

80 Serial MPU 16-Bit Bus



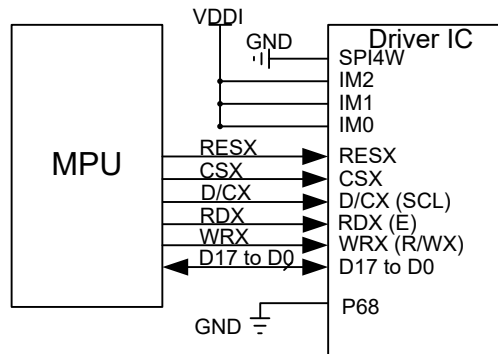
13.3.3 8080-Series MCU Interface for 9-bit Data Bus (P68=0, IM2, IM1, IM0="110")

80 Serial MPU 9-Bit Bus



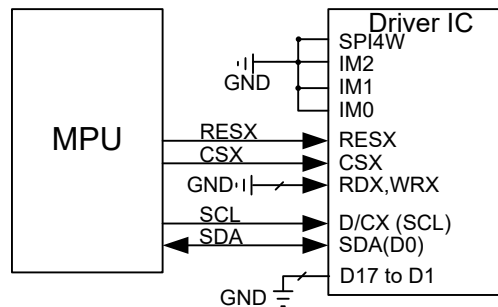
13.3.4 8080-Series MCU Interface for 18-bit Data Bus (P68=0, IM2, IM1, IM0="111")

80 Serial MPU 18-Bit Bus



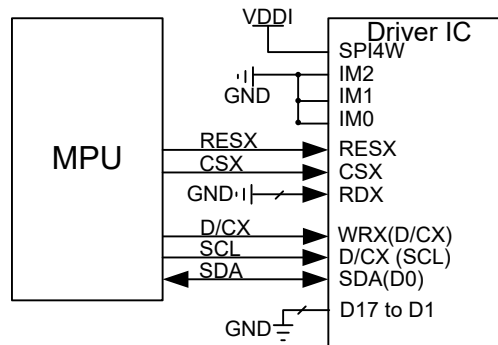
13.3.5 3-Line Serial MCU Interface (IM2, IM1, IM0="000", SPI4W=0)

3-Pin Serial Mode



13.3.6 4-Line Serial MCU Interface (IM2, IM1, IM0="000", SPI4W=1)

4-Pin Serial Mode



14 Revision History

ST7735P3 Specification Revision History		
Version	Date	Description
P0.1	2021/8	First issue.