SSD1333

Advance Information

176 RGB x 176 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Appendix: IC Revision history of SSD1333 Specification

Version	Change Items	Effective Date
1.0	1st Release	14-Feb-18
1.1	Updated ordering part number to SSD1333Z	27-Mar-18

CONTENTS

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FIGURES

1 GENERAL DESCRIPTION

SSD1333 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display. It consists of 528 segments and 176 commons output, supporting up to 176RGB x 176 dot matrix display. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1333 has embedded Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 8, 16 bits 6800-/8080-series compatible Parallel Interface, I2C Interface, or Serial Peripheral Interface. It supports 256-step contrast and 65K color control. SSD1333 is suitable for portable applications such as wearable electronics with vivid color OLED display.

2 FEATURES

- Resolution: 176RGB x 176 dot matrix panel
- Power supply
  - V_{DD} = 1.65V – 3.5V (MCU interface logic level & low voltage power supply)
  - V_{CC} = 8.0V – 18.0V (Panel driving power supply)
- Segment maximum source current: 320uA
- Common maximum sink current: 160mA
- Pin selectable MCU Interfaces:
  - 8/16 bits 6800/8080-series parallel Interface
  - 3/4 wire Serial Peripheral Interface
  - I2C Interface
- 256 step brightness current control for the each color component plus master current control
- Support color depth of 256 and 65k
- Support 3 individual Gamma Look Up Tables (GLUT) for R, G, B
- Color Swapping Function (RGB – BGR)
- Row re-mapping and Column re-mapping
- Screen saving infinite content scrolling function
- Programmable Frame Rate
- Power On Reset (POR)
- On-Chip Oscillator
- Chip layout for COG, COF
- Operating temperature range -40℃ to 85℃

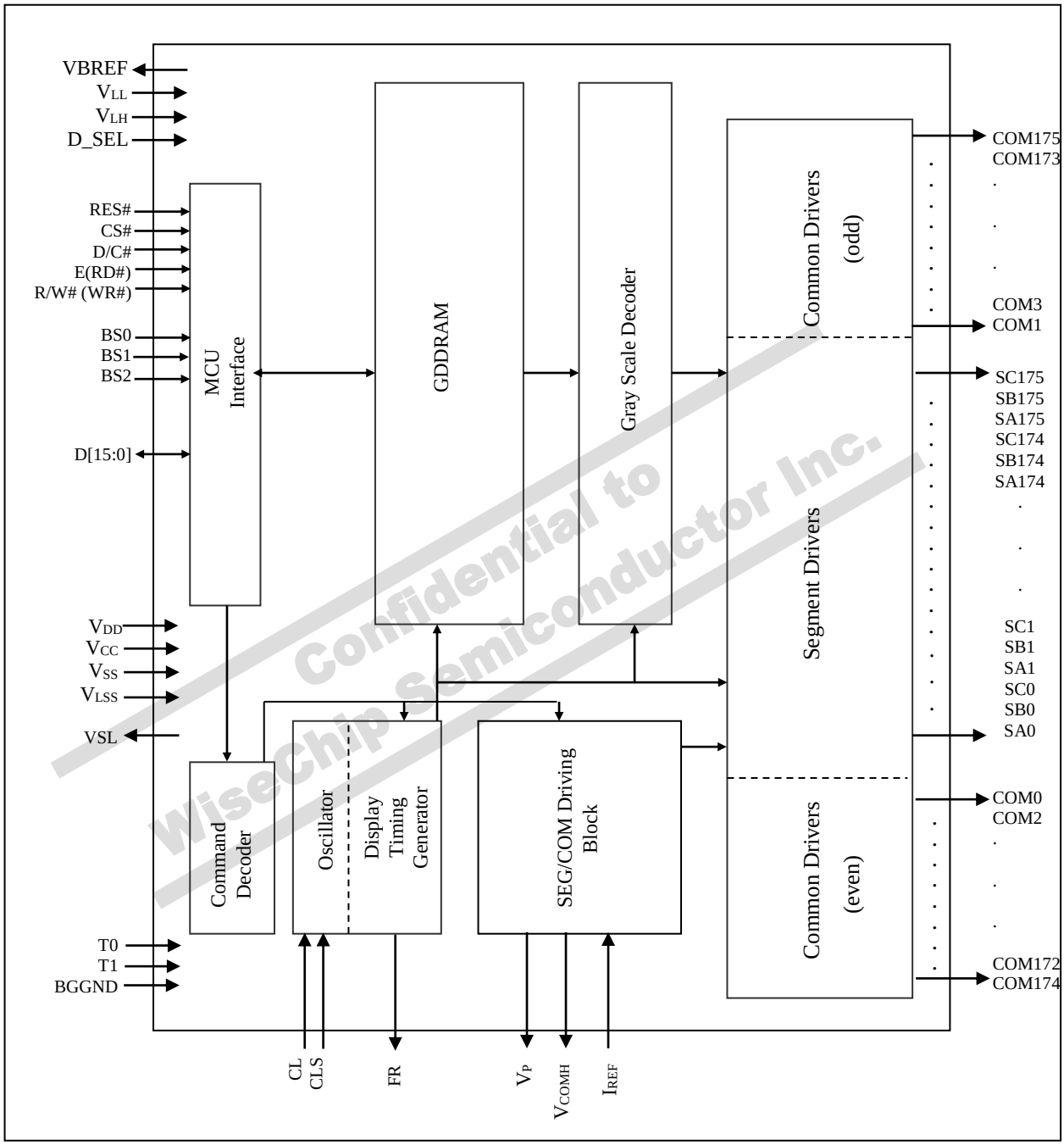
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1333Z	176RGB	176	COG	○ Min SEG pad pitch : 27um ○ Min COM pad pitch : 27um ○ Min I/O pad pitch : 55um ○ Die thickness: 250um ○ Bump height: nominal 12um

4 BLOCK DIAGRAM

Figure 4-1 –SSD1333 Block Diagram



5 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to V_{LL} / Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{LH} / V_{DD}
P = Power pin	

Table 5-1: Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation. A capacitor should be connected between this pin and V_{SS}.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. A capacitor should be connected between this pin and V_{SS}.
V_p	P	This pin is the segment pre-charge voltage reference pin. A capacitor can be connected between this pin and V_{SS} to improve visual performance. It can also be float per application. No external power supply is allowed to connect to this pin.
BGGND	P	Reserved pin. It must be connected to V_{SS}.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
VSL	P	This is segment voltage (output low level) reference pin. This pin has to be connected with resistor and diode to ground (details depends on application).
V_{LH}	P	Logic high (same voltage level as V_{DD}) for internal connection of input and I/O pins. No need to connect to external power source.
V_{LL}	P	Logic low (same voltage level as V_{SS}) for internal connection of input and I/O pins. No need to connect to external ground.
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
VBREF	O	This is a reserved pin. It should be kept NC.

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>BS[2:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select.

Table 5-2: Bus Interface selection
<table><tr><td>BS[2:0]</td><td>Interface</td></tr><tr><td>000</td><td>4 line SPI</td></tr><tr><td>001</td><td>3 line SPI</td></tr><tr><td>010</td><td>I^2C</td></tr><tr><td>100</td><td>8-bit 6800 parallel</td></tr><tr><td>101</td><td>16-bit 6800 parallel</td></tr><tr><td>110</td><td>8-bit 8080 parallel</td></tr><tr><td>111</td><td>16-bit 8080 parallel</td></tr></table>
Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}</td></tr>
<tr><td>I_{REF}</td><td>I</td><td>This pin is the segment output current reference pin.

I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA.</td></tr>
<tr><td>CL</td><td>I</td><td>This is external clock input pin.

When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{SS}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>This is internal clock enable pin.

When it is pulled HIGH (i.e. connect to V_{DD}), internal clock is enabled. When it is pulled LOW, the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU.

The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.

When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data at D[15:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[15:0] will be transferred to a command register.
In I^2C mode, this pin acts as SA0 for slave address selection.
When 3-wire serial interface is selected, this pin must be connected to V_{SS}.</td></tr>
</table>

Pin Name	Pin Type	Description
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[15:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
D_SEL	I	Should be connected to V_{LL}.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
TP[15:0]	-	Reserved pins. These pins should be kept NC.
T[1:0]	I	Reserved pin. This pin should be kept NC.
PT[1:0]	I/O	Reserved pin. This pin should be kept NC.
SA[175:0] SB[175:0] SC[175:0]	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF. The 540 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.
COM[175:0]	O	These pins provide the Common switch signals to the OLED panel.
NC	-	This is dummy pin. It should be kept NC.

6 FUNCTIONAL BLOCK DESCRIPTIONS

6.1 MCU Interface selection

SSD1333 MCU interface consist of 16 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 5-2: Bus Interface selection for BS[2:0] setting).

Table 6-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface																Control Signal				
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 8080	Tie Low								D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	Tie Low								D[7:0]								E	R/W#	CS#	D/C#	RES#
16-bit 8080	D[15:0]																RD#	WR#	CS#	D/C#	RES#
16-bit 6800	D[15:0]																E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie Low														SDIN	SCLK	Tie Low		CS#	Tie Low	RES#
4-wire SPI	Tie Low														SDIN	SCLK	Tie Low		CS#	D/C#	RES#
I^2C	Tie Low													SDA_{OUT}	SDA_{IN}	SCL	Tie Low			SA0	RES#

When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 and D2 should be tied together as the serial data input: SDIN.

6.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 16 bi-directional data pins (D[15:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

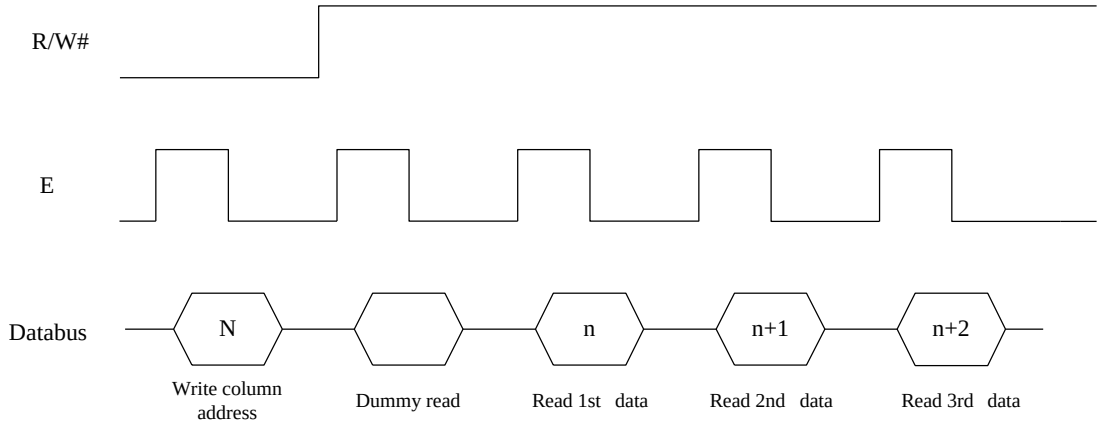
Table 6-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

Figure 6-1 : Data read back procedure - insertion of dummy read



6.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 16 bi-directional data pins (D[15:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6-2 : Example of Write procedure in 8080 parallel interface mode

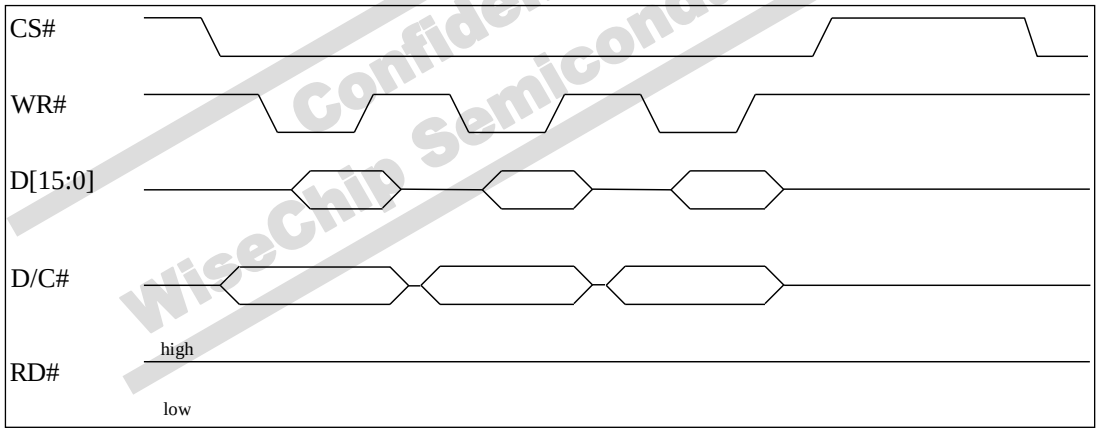


Figure 6-3 : Example of Read procedure in 8080 parallel interface mode

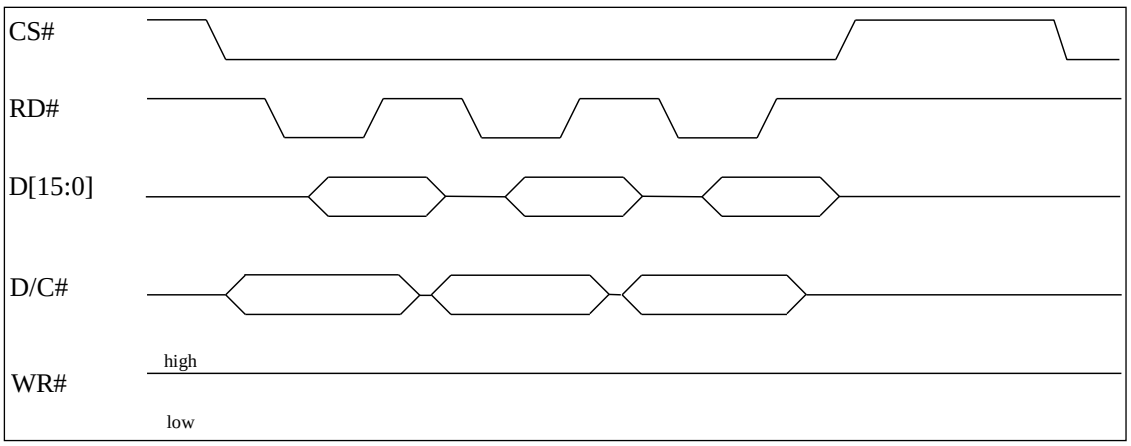


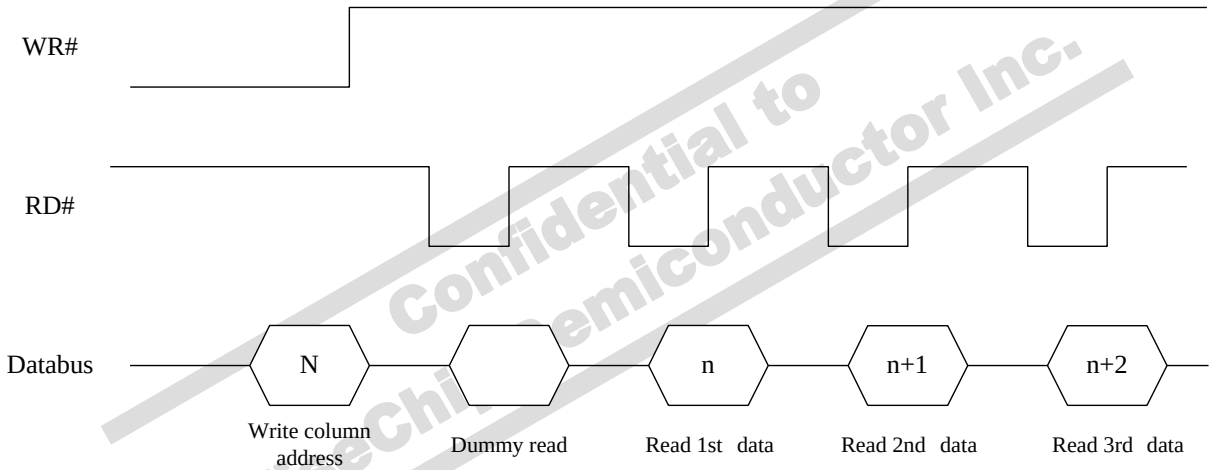
Table 6-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

Figure 6-4 : Display data read back procedure - insertion of dummy read



6.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D15, E(RD#) and R/W#(WR#) can be connected to an external ground.

Table 6-4 : Control pins of 4-wire Serial interface

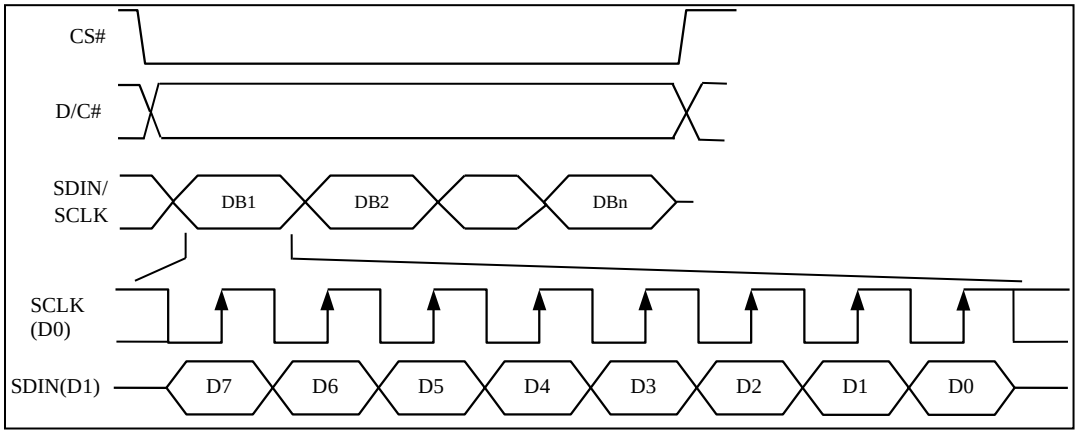
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eight clocks and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock. D/C# should keep its stage from the start to the end of operation.

Under serial mode, only write operations are allowed.

Figure 6-5 : Write procedure in 4-wire Serial interface mode



6.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D15, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

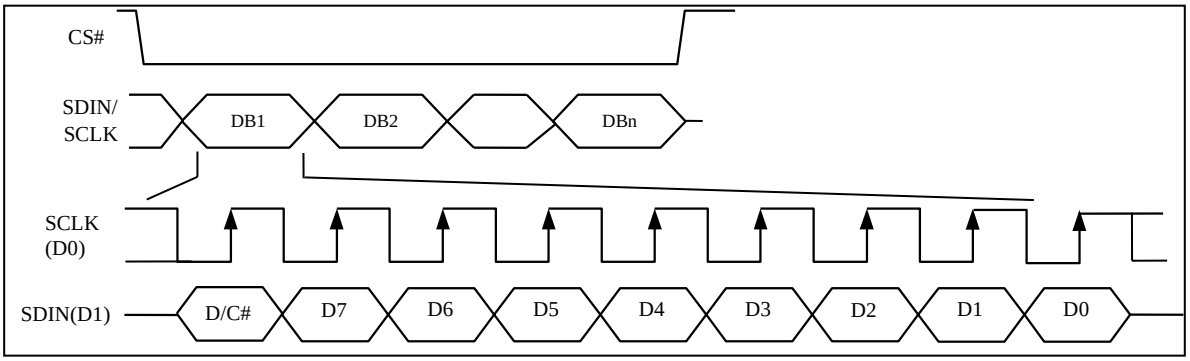
Under serial mode, only write operations are allowed.

Table 6-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 6-6 : Write procedure in 3-wire Serial interface mode



6.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1333 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1333. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

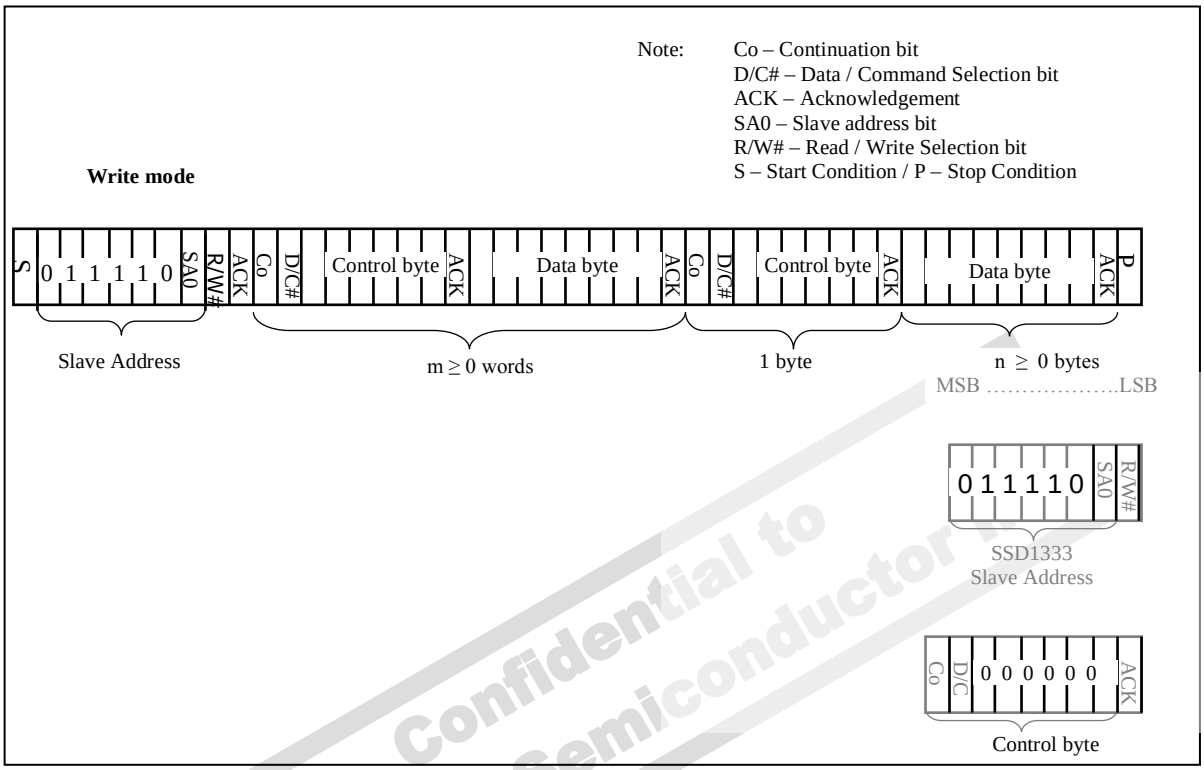
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 6-7 for the write mode of I²C-bus in chronological order.

Figure 6-7 : I²C-bus data format



6.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1333, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.

7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 6-8 : Definition of the Start and Stop Condition

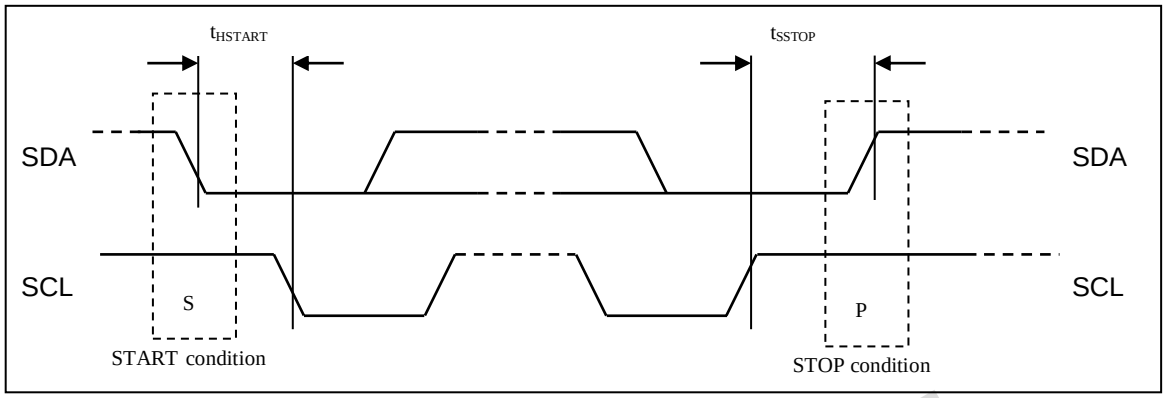
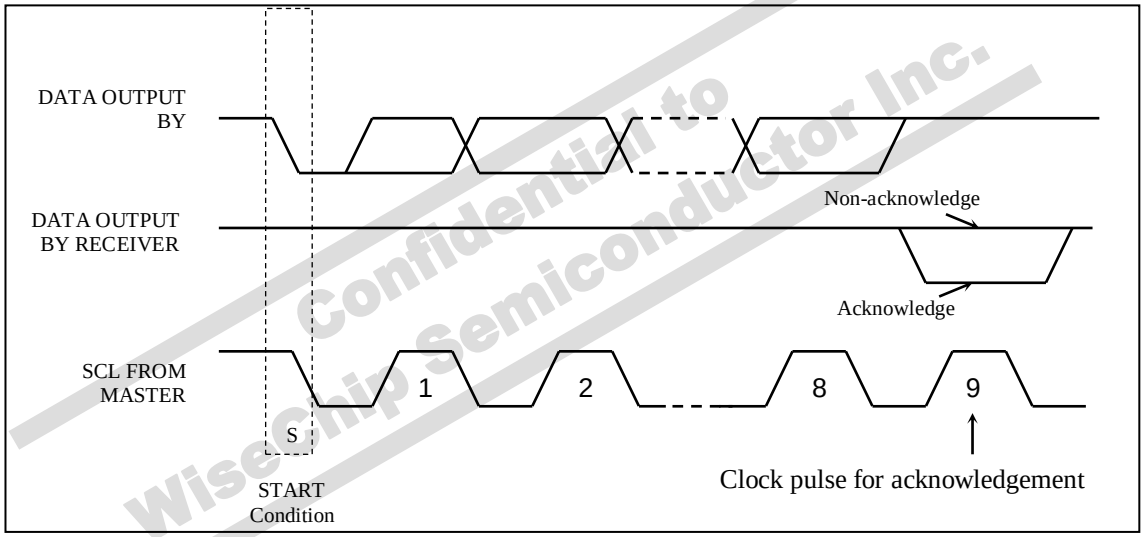


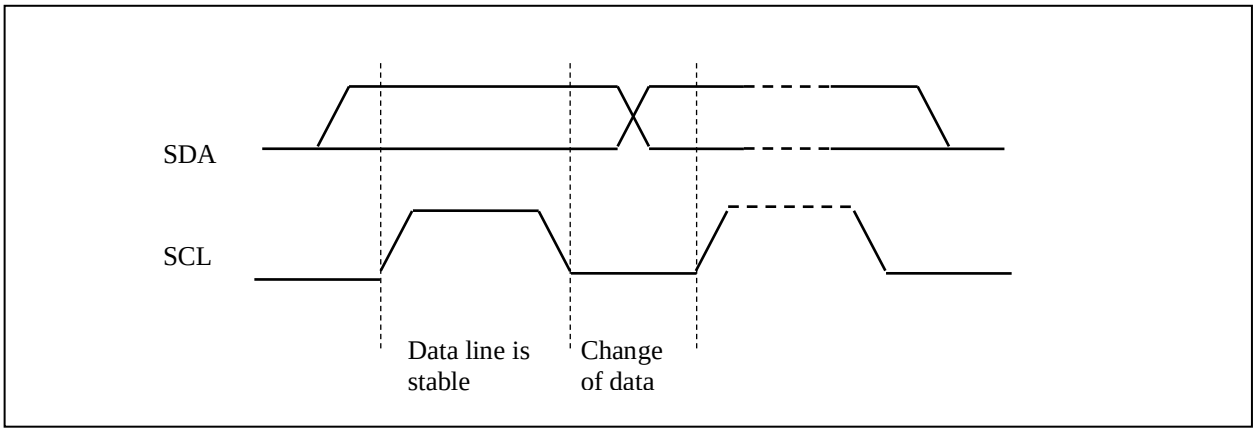
Figure 6-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure 6-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-10 : Definition of the data transfer condition



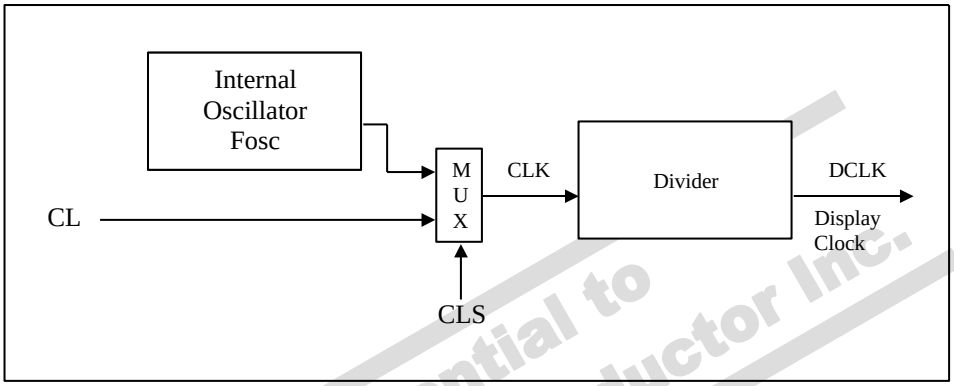
6.2 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

6.3 Oscillator Circuit and Display Time Generator

Figure 6-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{SS}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command B3h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The divide ratio "D" can be programmed from 1 to 256 by command B3h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\,of\ Mux}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 256.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  K_o = DCLKs in current drive period = 145.
  Default K is 8 + 16 + 145 = 169 at power on reset.
  Please refer to Section 6.7 "SEG / COM Drivers" for the details of the "Phase".
- Number of multiplex ratio is set by command CAh. The power on reset value is 175 (i.e. 176MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

6.4 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 176 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Default linear LUT (Equivalent to B9h command)
10. Normal display mode (Equivalent to A6h command)

6.5 GDDRAM

6.5.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 176 x 176 x 16bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 16-bit data. Sub-pixels for color A, C have 5 bits and B have 6 bits. The arrangement of data pixel in graphic display data RAM is shown in Table 6-6.

Table 6-6: 65k Color Depth Graphic Display Data RAM Structure

Segment	Normal	0			1			2	·····	·····	174	175			
Address	Remapped	175			174			173	·····	·····	1	0			
Color		A	B	C	A	B	C	A			C	A	B	C	
Data format			B5			B5			·····	·····			B5		
		A4	B4	C4	A4	B4	C4	A4	·····	·····	C4	A4	B4	C4	
		A3	B3	C3	A3	B3	C3	A3	·····	·····	C3	A3	B3	C3	
Common		A2	B2	C2	A2	B2	C2	A2	·····	·····	C2	A2	B2	C2	
Address		A1	B1	C1	A1	B1	C1	A1	·····	·····	C1	A1	B1	C1	
		A0	B0	C0	A0	B0	C0	A0	·····	·····	C0	A0	B0	C0	
Normal	Remapped														Common output
0	175	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM0
1	174	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM1
2	173	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM2
3	172	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM3
4	171	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM4
5	170	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM5
6	169	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM6
7	168	5	6	no. of bits in this cell			5	5	·····	·····	5	5	6	5	COM7
:	:	:	:	:	:	:	:	:	·····	·····	:	:	:	:	:
:	:	:	:	:	:	:	:	:	·····	·····	:	:	:	:	:
:	:	:	:	:	:	:	:	:	·····	·····	:	:	:	:	:
171	4	5	6	5	5	6	5	5	·····	·····	5	5	6	5	:
172	3	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM172
173	2	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM173
174	1	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM174
175	0	5	6	5	5	6	5	5	·····	·····	5	5	6	5	COM175

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	·····	·····	SC174	SA175	SB175	SC175

6.5.2 Data bus to RAM mapping under different input mode

Table 6-7 : Write Data bus usage under different bus width and color depth mode

Write data			Data bus															
Bus width	Color depth	Input order	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8bits / Serial	256		X	X	X	X	X	X	X	X	C4	C3	C2	B5	B4	B3	A4	A3
8bits / Serial	65k	1st	X	X	X	X	X	X	X	X	C4	C3	C2	C1	C0	B5	B4	B3
		2nd	X	X	X	X	X	X	X	X	B2	B1	B0	A4	A3	A2	A1	A0
8bits / Serial	Pseudo 262k	1st	X	X	X	X	X	X	X	X	X	X	C4	C3	C2	C1	C0	X
		2nd	X	X	X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0
		3rd	X	X	X	X	X	X	X	X	X	X	A4	A3	A2	A1	A0	X
16bits	65k		C4	C3	C2	C1	C0	B5	B4	B3	B2	B1	B0	A4	A3	A2	A1	A0
16bits	Pseudo 262k format 1	1st	X	X	X	X	X	X	X	X	X	X	C4	C3	C2	C1	C0	X
		2nd	X	X	B5	B4	B3	B2	B1	B0	X	X	A4	A3	A2	A1	A0	X
16bits	Pseudo 262k format 2	1st	X	X	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
		2nd	X	X	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	X	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$	X
		3rd	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$	X

Table 6-8 : Read Data bus usage under different bus width and color depth mode

Read data			Data bus															
Bus width	Color depth	Input order	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8bits	256		X	X	X	X	X	X	X	X	C4	C3	C2	B5	B4	B3	A4	A3
8bits	65k	1st	X	X	X	X	X	X	X	X	C4	C3	C2	C1	C0	B5	B4	B3
		2nd	X	X	X	X	X	X	X	X	B2	B1	B0	A4	A3	A2	A1	A0
8bits	Pseudo 262k	1st	X	X	X	X	X	X	X	X	X	X	C4	C3	C2	C1	C0	X
		2nd	X	X	X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0
		3rd	X	X	X	X	X	X	X	X	X	X	A4	A3	A2	A1	A0	X
16bits	65k		C4	C3	C2	C1	C0	B5	B4	B3	B2	B1	B0	A4	A3	A2	A1	A0
16bits	Pseudo 262k format 1	1st	X	X	X	X	X	X	X	X	X	X	C4	C3	C2	C1	C0	X
		2nd	X	X	B5	B4	B3	B2	B1	B0	X	X	A4	A3	A2	A1	A0	X
16bits	Pseudo 262k format 2	1st	X	X	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
		2nd	X	X	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	X	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$	X
		3rd	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$	X

6.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

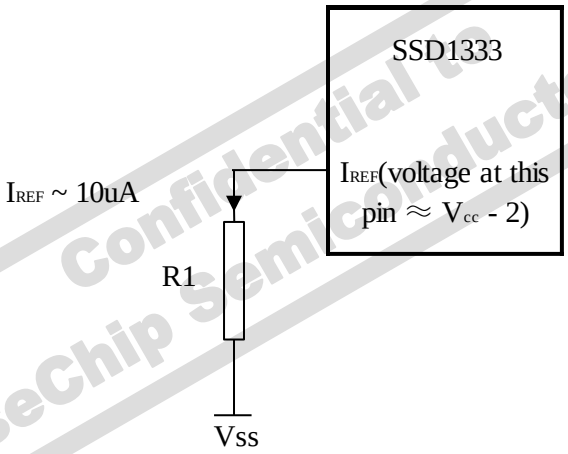
- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = Contrast / 8 x I_{REF}

  in which the contrast (1~255) is set by Set Contrast command C1h

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 6-12. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 320uA at maximum contrast 255.

Figure 6-12 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2V, the value of resistor R1 can be found as below:

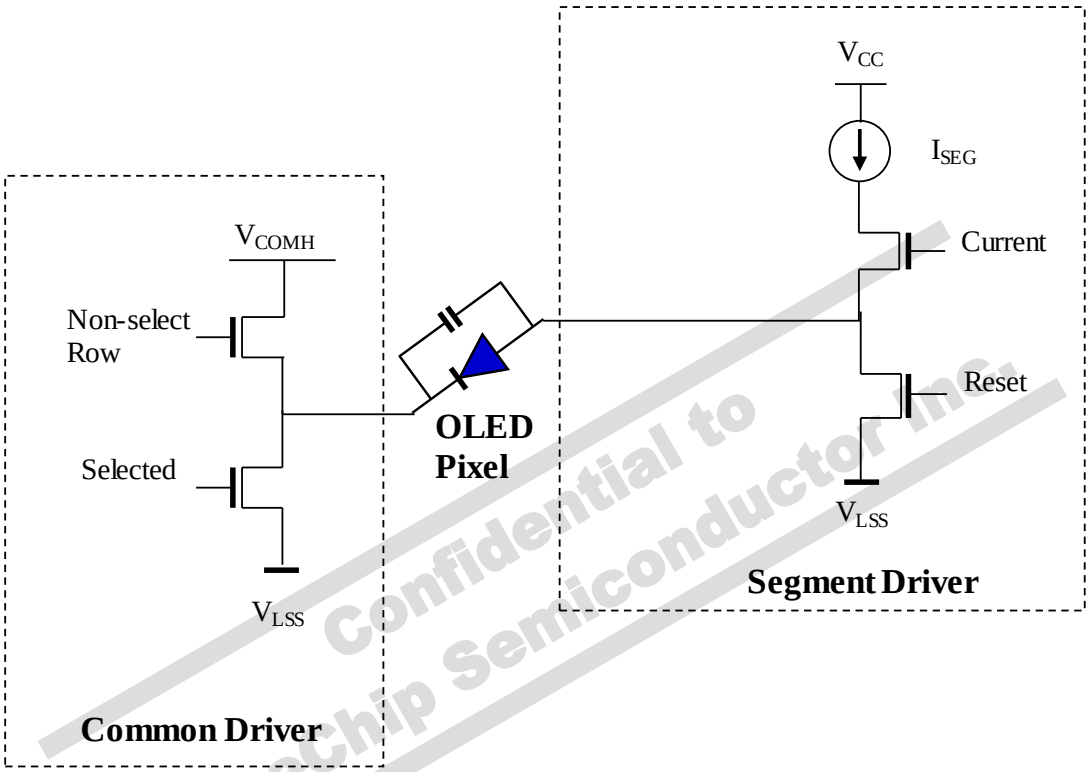
For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 2) / 10uA
= 1MΩ

6.7 SEG / COM Drivers

Segment drivers consist of 528 (176 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (C1h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

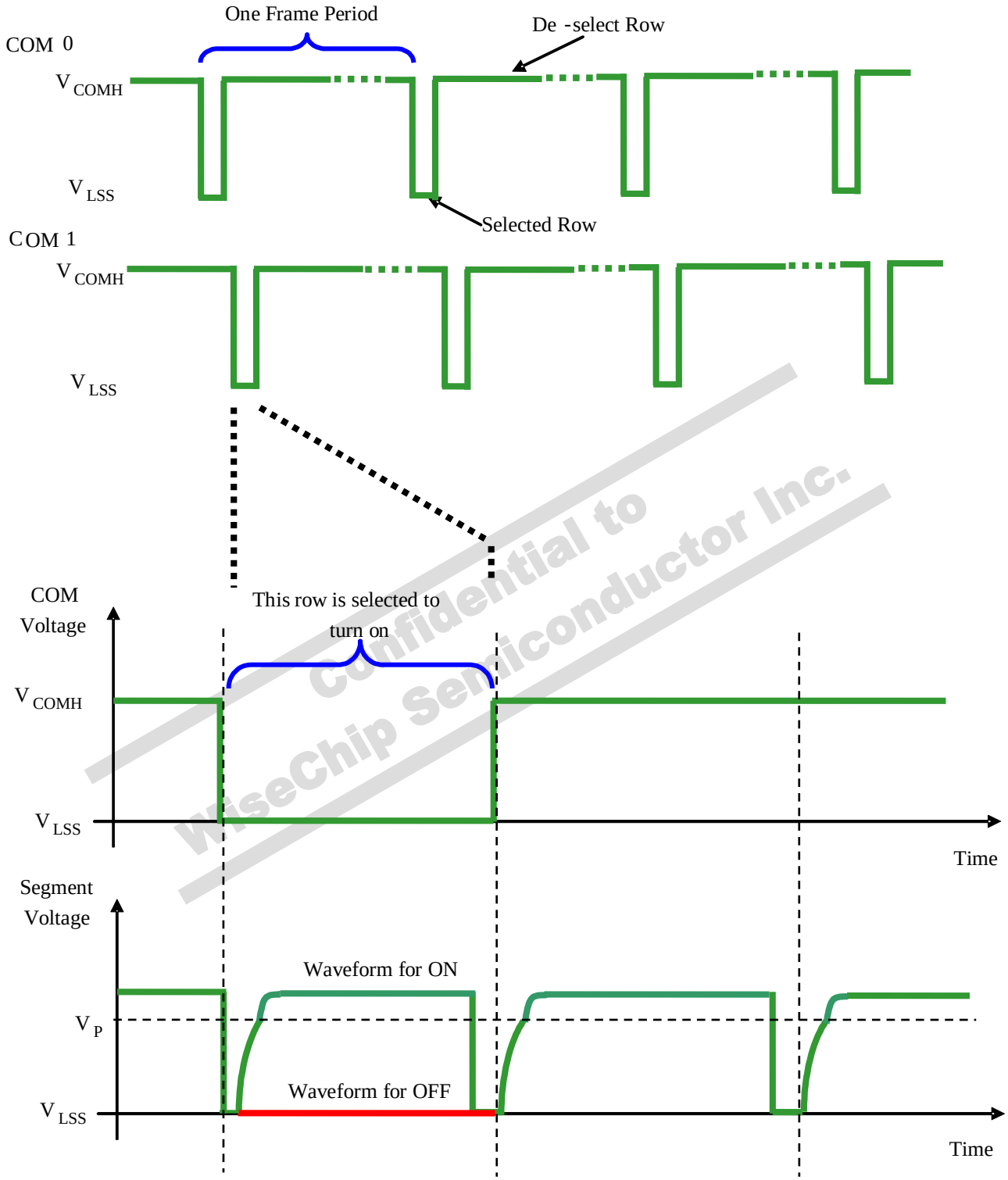
Figure 6-13 : Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 6-14.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is disabled and the Reset switch is enabled. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 6-14 : Segment and Common Driver Signal Waveform



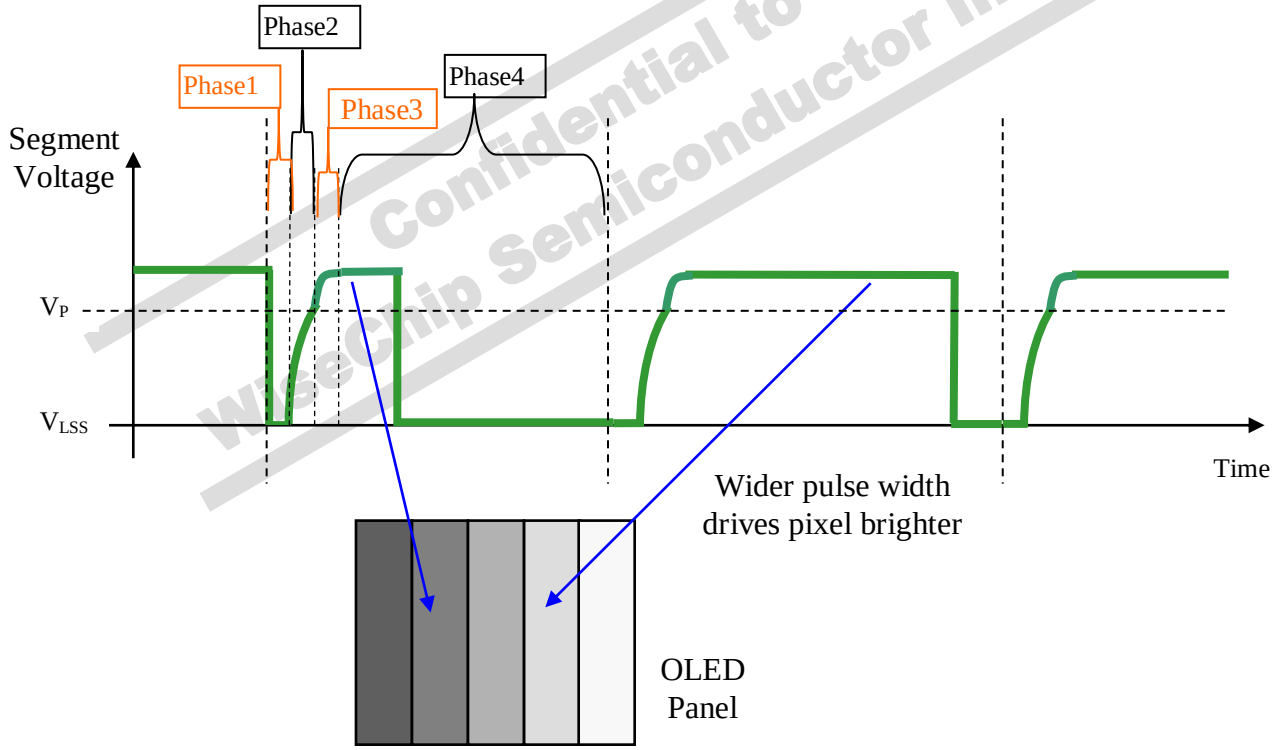
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B6h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h, BCh, BDh / B9h. The bigger gamma setting in the current drive stage results in brighter pixels and vice versa (Details refer to Section 6.8). This is shown in the following figure.

Figure 6-15 : Gray Scale Control in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h "Master Look Up Table for Gray Scale Pulse width (Color A,B,C)" or B9h "Use Built-in Linear LUT" or Individual Look Up Table for Gray Scale Pulse width (Color A/B/C) BCh, B8h, BDh. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

6.8 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width of segment drivers in current drive phase. The gray scale tables store the corresponding pulse widths of the 31 gray scale levels for Color A, C and 63 gray scale levels for Color B through the software commands B8h, B9h, BCh and BDh. The wider the pulse width, the brighter the pixel will be. The maximum pulse width setting is 124 DCLKS. Colors A, B and C are using 3 individual gray scale tables.

As shown in Figure 6-16, color A, C sub-pixel RAM data has 5 bits, represent the 31 gray scale levels from GS1 to GS31. And color B sub-pixel RAM data has 6 bits, represent the 63 gray scale levels from GS1 to GS63.

Figure 6-16 : Relation between GDDRAM content and gray scale table entry for three colors in 65K color mode

Color A, C			Color B		
RAM data (5 bits)	Gray Scale	Default pulse width of GS[1:31] in terms of DCLK	RAM data (6 bits)	Gray Scale	Default pulse width of GS[1:63] in terms of DCLK
00001	GS1	0	000001	GS1	0
00010	GS2	4	000010	GS2	2
00011	GS3	8	000011	GS3	4
00100	GS4	12	000100	GS4	6
:			:	:	:
:			:	:	:
11101	GS29	112	111101	GS61	120
11110	GS30	116	111110	GS62	122
11111	GS31	120	111111	GS63	124

GS1 has only pre-charge but no current drive stage. The duration of different GS are programmable by command B8h for color B, BCh for color A, BDh for color C and the maximum pulse width setting is 124 DCLKs.

When setting the Gray Scale Table (by B8h, BCh, BDh command), the rules below must follow:

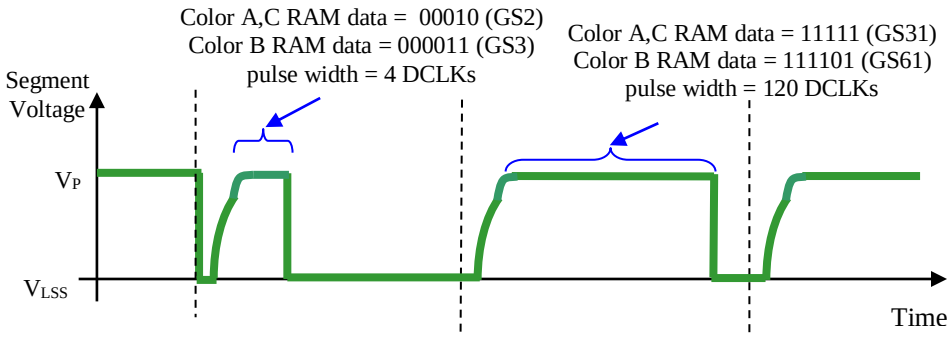
1) The 63 gray scale levels are entered after command B8h for color B. The 31 gray scale levels are entered after command BCh or BDh for color A, C. Note that command B8h has to be inputted before BCh and BDh command.
2) The gray scale is defined in incremental way, with reference to the length of previous table entry:

Setting of GS1 has to be >= 0
Setting of GS2 has to be > Setting of GS1
Setting of GS3 has to be > Setting of GS2
:
Setting of GS63 has to be > Setting of GS62

Figure 6-17 : Illustration of relation between graphic display RAM value and gray scale control

Gray scale table

Gray Scale		Value/DCLK	
A,C	B	A,C	B
GS1	GS1	0	0
GS2	GS2	4	2
GS3	GS3	8	4
:	:	:	:
GS29	GS61	112	120
GS30	GS62	116	122
GS31	GS63	120	124



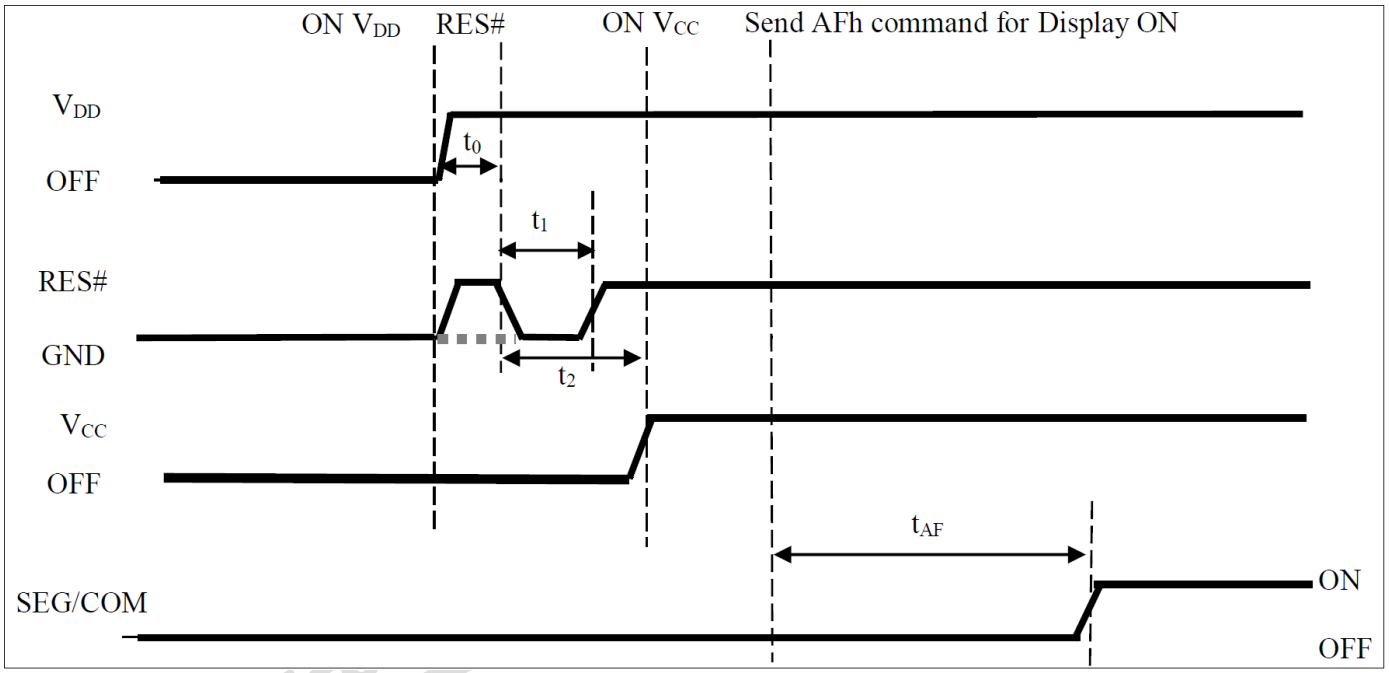
6.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1333.

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

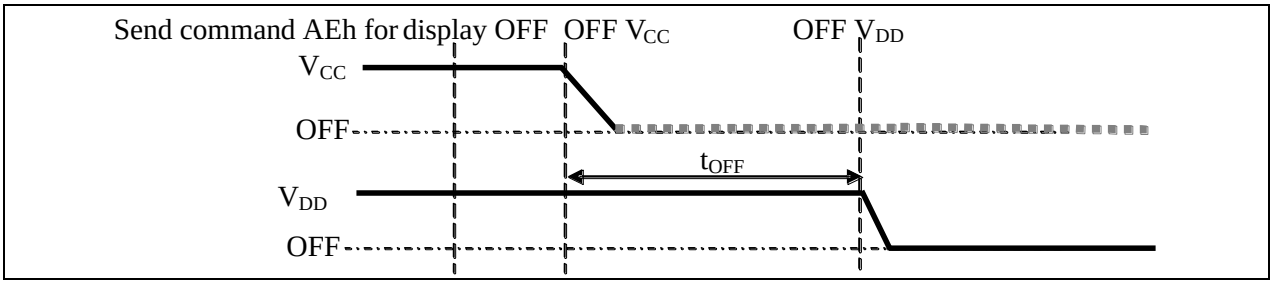
Figure 6-18 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Power OFF V_{DD} after t_{OFF}. [4] (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 6-19 : The Power OFF sequence



Note:

[1] V_{CC} should be kept float (i.e. disable) when it is OFF.
[2] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
[3] The register values are reset after t_1.
[4] V_{DD} should not be Power OFF before V_{CC} Power OFF.

7 MAXIMUM RATINGS

Table 7-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 19.0	V
V_{DD}		-0.3 to 4.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	Vss-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	℃
T_{stg}	Storage Temperature Range	-65 to +150	℃

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

8 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65 to 3.5V

T_A = 25°C

Table 8-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	8	-	18	V
V_{DD}	Low voltage power supply, power Supply for I/O pins	-	1.65	-	3.5	V
V_{OH}	High Logic Output Level	Iout = 100uA	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	Iout = 100uA	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2*V_{DD}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{DD} = 2.8V, V_{CC} = 16V Display OFF, No panel attached	-	-	10	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{DD} = 2.8V, V_{CC} = 16V, Display OFF, No panel attached	-	-	10	uA
I_{DD}	V_{DD} Supply Current	V_{DD} = 2.8V, V_{CC} = 16V, Display ON, No panel attached, contrast = FFh	-	840	930	uA
I_{CC}	V_{CC} Supply Current	V_{DD} = 2.8V, V_{CC} = 16V, Display ON, No panel attached, contrast = FFh	-	2.8	3.1	mA
I_{SEG}	Segment Output Current Setting V_{CC}=18V, I_{REF}=10uA	Contrast = FF	-	320	-	uA
		Contrast = 7F	-	160	-	uA
		Contrast = 3F	-	80	-	uA
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID}) / I_{MID} I_{MID} = (I_{MAX} + I_{MIN}) / 2 I_{SEG} = Segment current at contrast FF	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

9 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

T_A = 25°C

Table 9-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} =2.8V	2.8	3.12	3.45	MHz
F_{FRM}	Frame Frequency for 176 MUX Mode	176x176 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1/(D*K*176) (2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value, and B3h A[3:0] is in [0000].

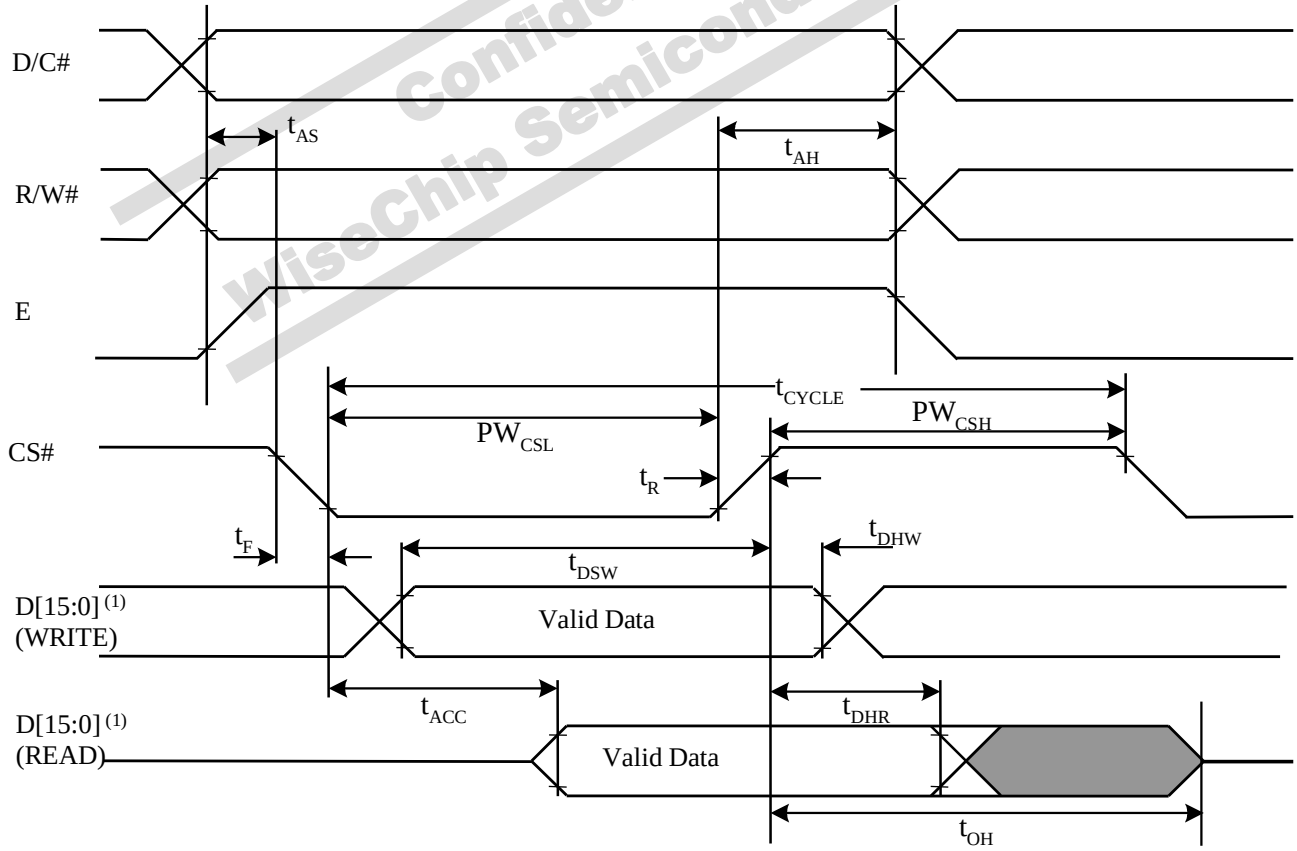
(2) D: divide ratio set by command B3h A[3:0]
K: Phase 1 period +Phase 2 period + X
X: DCLKs in current drive period

Table 9-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (write)	300	-	-	ns
t_{AS}	Address Setup Time	24	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	160 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 9-1 : 6800-series MCU parallel interface characteristics



Note

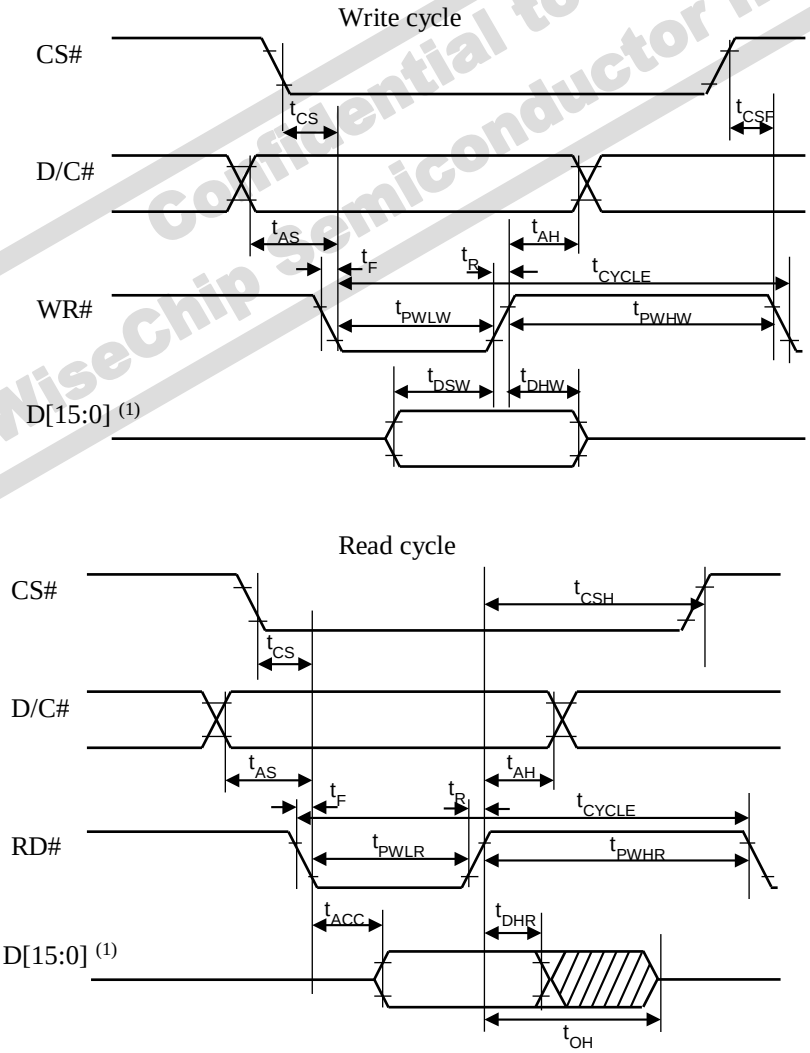
(1) when 8 bit used: D[7:0] instead; when 16 bit used: D[15:0] instead.

Table 9-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (write)	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	46	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	160	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 9-2 : 8080-series MCU parallel interface characteristics



Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead.

Table 9-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	42	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	25	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 9-3 : Serial interface characteristics (4-wire SPI)

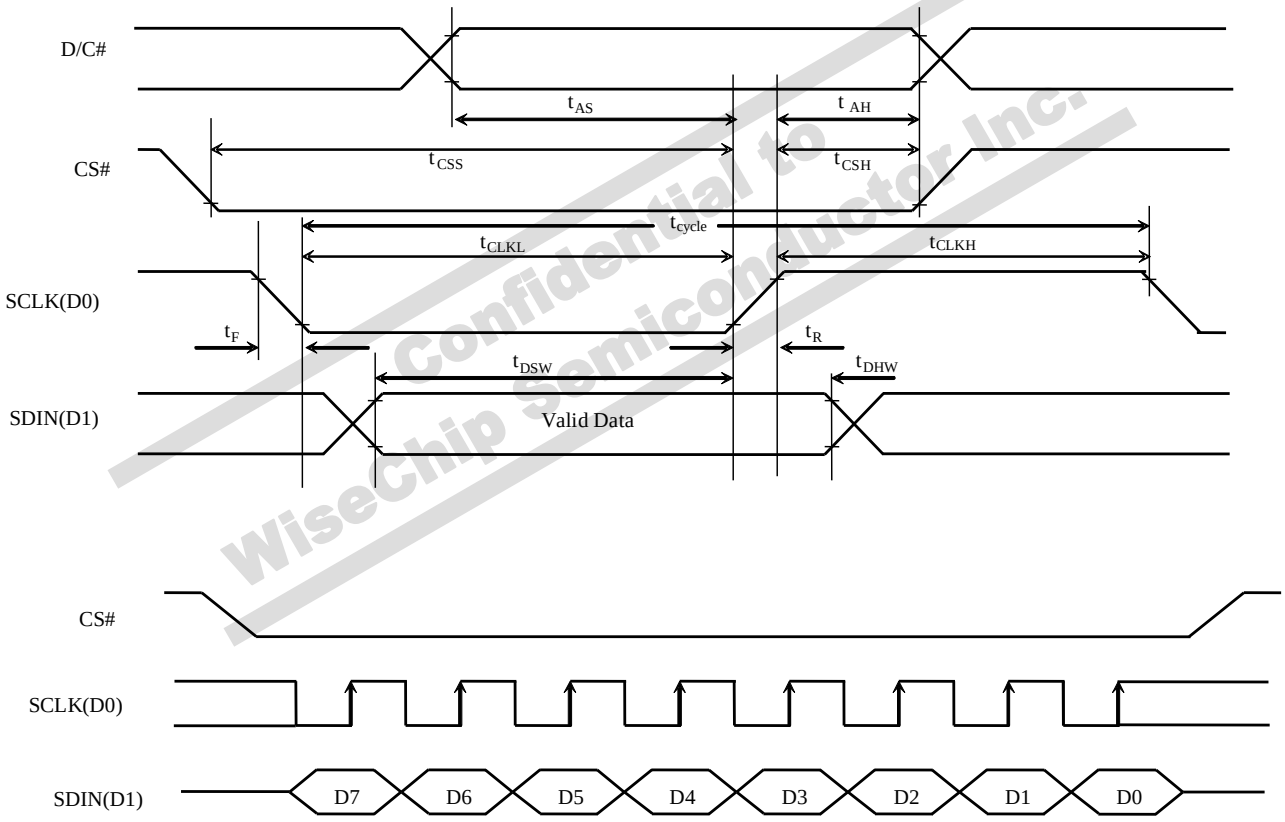


Table 9-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	25	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 9-4 : Serial interface characteristics (3-wire SPI)

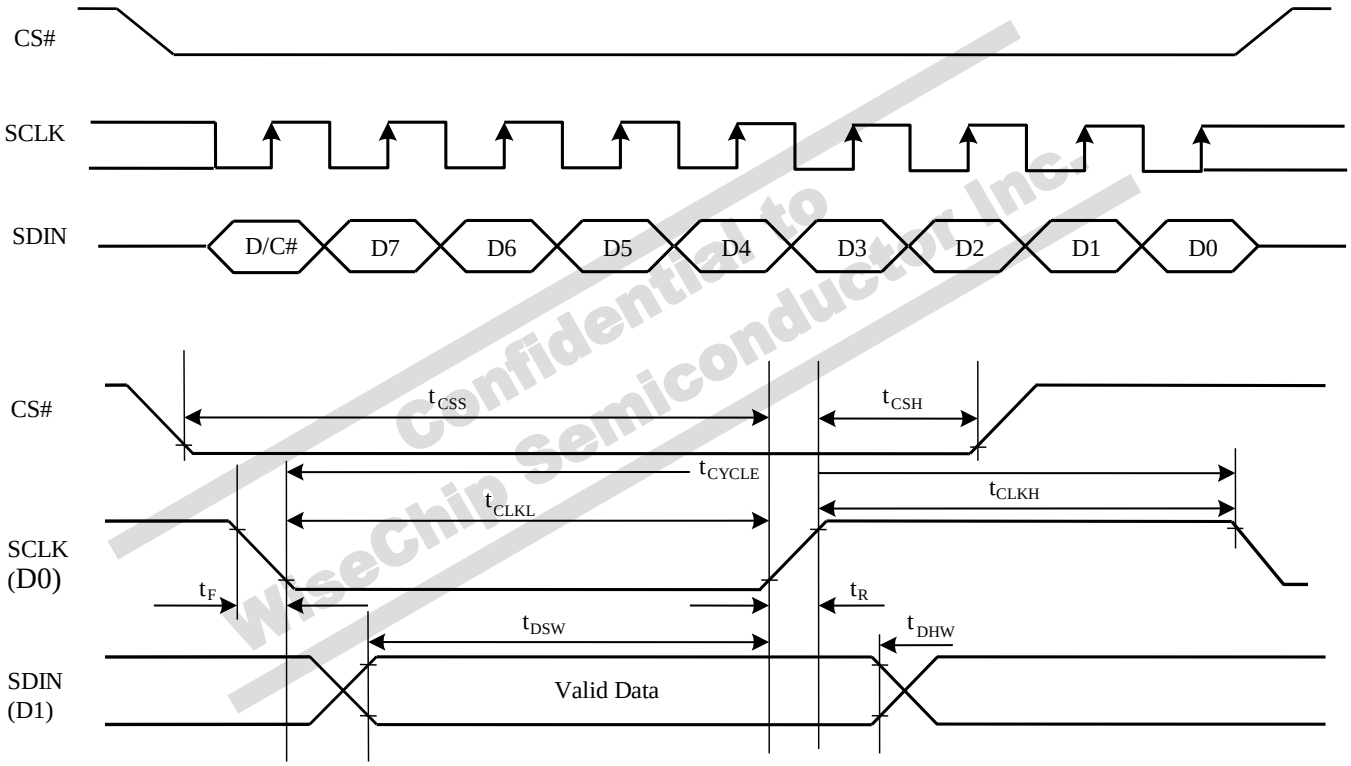
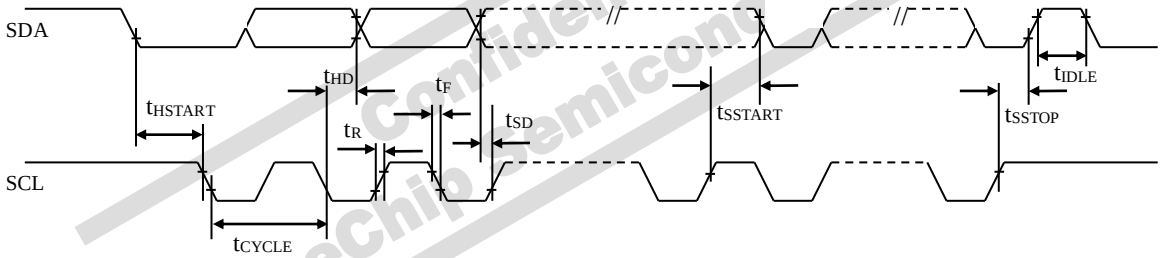


Table 9-6 : I²C Interface Timing Characteristics

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

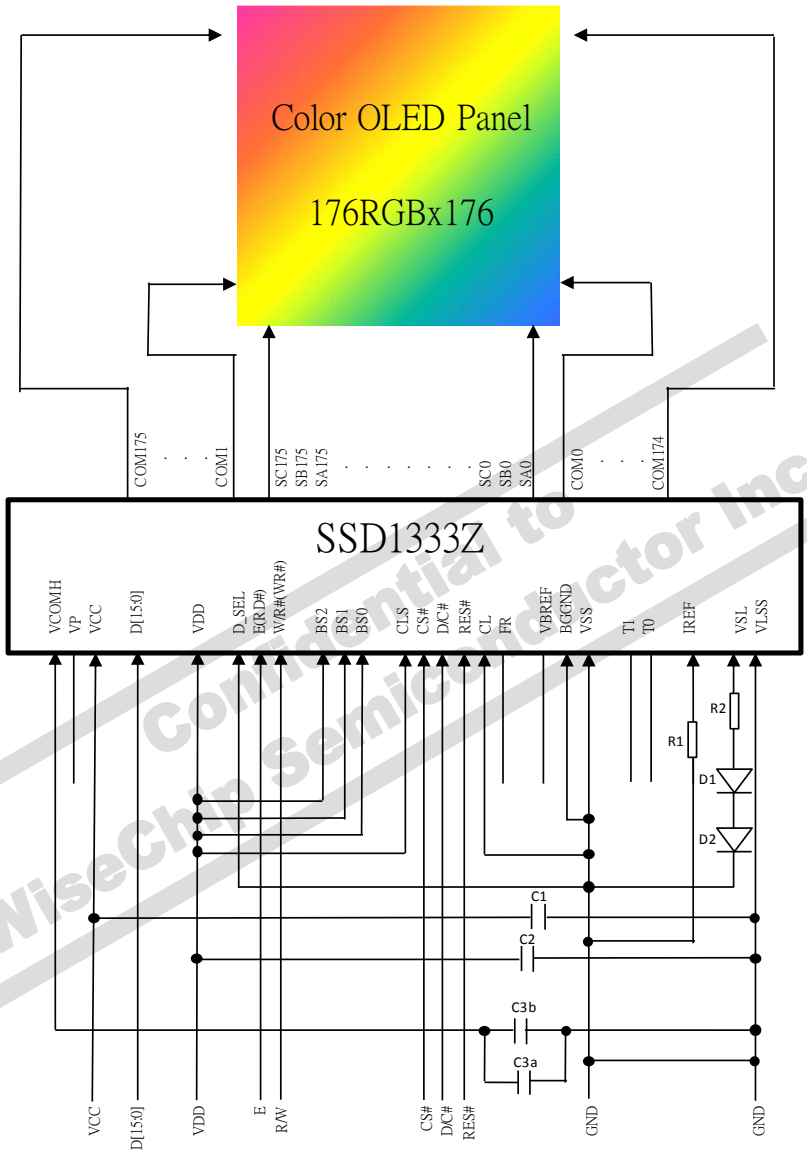
Figure 9-5 : I²C interface Timing characteristics



10 APPLICATION EXAMPLE

Figure 10-1 : SSD1333Z application example for 16-bit 8080-parallel interface mode

The configuration for 16-bit 8080-parallel interface mode is shown in the following diagram:
(V_{DD} = 2.8V, external V_{CC} = 12V, I_{REF} = 10uA



Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 12V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (12-2) / 10u
= 1MΩ
R2 = 50Ω, 1/8W (1)
D1 ~ D2: V_{th}=0.7V, 1N4148 (1)
C2: 1uF, C1, C3a: 4.7uF, C3b: 0.1uF (1)

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) Die gold bump face up.
(3) All V_{LSS} pads of the IC are recommended to be connected together to form a larger area of GND.
(4) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard GB/T 26572-2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

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