SH1108

160 X 160 Dot Matrix OLED/PLED Segment/Common Driver with Controller

Features

- Display Resolution Option：
  - 64 COM×160 SEG；
  - 96 COM×160 SEG；
  - 128 COM×160 SEG；
  - 160 COM×160 SEG；
- Embedded 160×160 bits SRAM
- Operating voltage:
  - Logic voltage supply: V_{DD} = 1.65V - 3.5V
  - DC-DC voltage supply: AV_{DD} = 2.4V -3.5V
  - OLED Operating voltage supply: Vpp=7.0V - 16.5V
- Maximum segment output current: 500μA
- Maximum common sink current: 80mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, and 3-wire & 4-wire serial peripheral interface.
- 400KHz fast I^2C bus interface
- Programmable frame frequency
- Row re-mapping and column re-mapping
- On-chip oscillator
- Available internal DC-DC converter
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
  - Sleep mode: <5μA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG form.

General Description

SH1108 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1108 consists of 160 segments, 160 commons that can support a maximum display resolution of 160 × 160. It is designed for Common Cathode type OLED panel.

SH1108 embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1108 is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.

Block Diagram

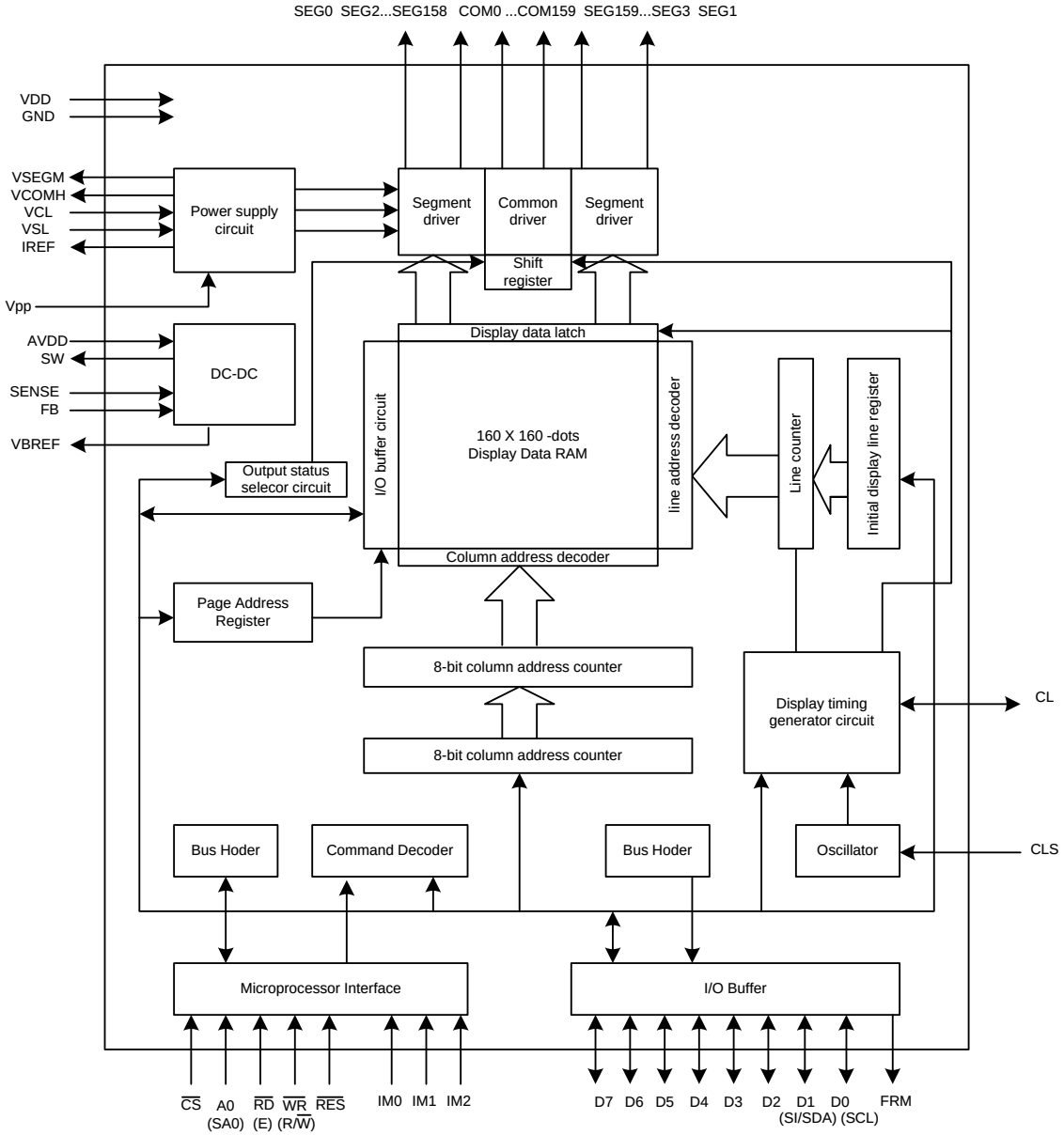


Figure 1 SH1108 Block Diagram

Pad Description

Power Supply

Pad NO.	Symbol	I/O	Description
41～42	V_{DD}	Supply	1.65 - 3.5V Power supply for logic and input/output
46	V_{DD}	O	1.65 - 3.5V Power output for pad option
23～24	AV_{DD}	Supply	2.4 – 3.5V power supply for the internal buffer of the DC-DC voltage converter
32	GND(ana)	Supply	Ground for analog.
33	GND(logic)	Supply	Ground for logic.
34	GND(buffer)	Supply	Ground for buffer.
3～8 78～83	GND	Supply	Ground.
44,48	GND	Supply	Ground output for pad option.
31	VSSA	Supply	Ground for VSL.
13~14	V_{SL}	Supply	This is a segment voltage reference pad. A capacitor should be connected between this pad and GND
35~39	V_{CL}	Supply	This is a common voltage reference pad. This pad should be connected to GND externally.
9~12 28~29 74~77	V_{PP}	Supply	This is the most positive voltage supply pad of the chip It should be supplied externally

OLED Driver Supplies

Pad NO.	Symbol	I/O	Description
49~50	I_{REF}	O	This is a segment current reference pad. A resistor should be connected between this pad and GND. Set the current at 15.625μA.
18~20	V_{COMH}	O	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and GND
15~17	V_{SEGM}	O	This is a pad for the voltage output high level for segment pre-charge. A capacitor should be connected between this pad and GND
25	V_{BREF}	O	This is an internal voltage reference pad for booster circuit
21~22	SW	O	This is an output pad driving the gate of the external NMOS of the booster circuit
26	FB	I	This is a feedback resistor input pad for the booster circuit. It is used to adjust the booster output voltage level, VPP
27	SENSE	I	This is a source current pad of the external NMOS of the booster circuit

System Bus Connection Pads

<table>
<tr><th>Pad NO.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>55</td><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>40</td><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.</td></tr>
<tr><td>43
45
47</td><td>IM0
IM1
IM2</td><td>I</td><td>These are the MPU interface mode select pads.
<table>
<tr><th></th><th>8080</th><th>I²C</th><th>6800</th><th>4-wire SPI</th><th>3-wire SPI</th></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>IM2</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>56</td><td>$\overline{CS}$</td><td>I</td><td>This pad is the chip select input. When $\overline{CS}$ = “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>57</td><td>$\overline{RES}$</td><td>I</td><td>This is a reset signal input pad. When $\overline{RES}$ is set to “L”, the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.</td></tr>
<tr><td>58</td><td>A0
（SA0）</td><td>I</td><td>This is the Data/Command control pad that determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I²C interface, this pad serves as SA0 to distinguish the different address of OLED driver.</td></tr>
<tr><td>59</td><td>$\overline{WR}$
($R/\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When $R/\overline{W}$ = “H”: Read.
When $R/\overline{W}$ = “L”: Write.</td></tr>
<tr><td>60</td><td>$\overline{RD}$
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.</td></tr>
<tr><td>61~68</td><td>D0 - D7
(SCL)
(SI/SDA)</td><td>I/O
I
I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance.
When the I²C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDA). At this time, D2 to D7 are set to high impedance.</td></tr>
<tr><td>54</td><td>FRM</td><td>O</td><td>This pad is No Connection pad, Its signal varies with the frame frequency. Its voltage is equal to VDD when the last common output of every frame is active, and is equal to GND during other time.</td></tr>
</table>

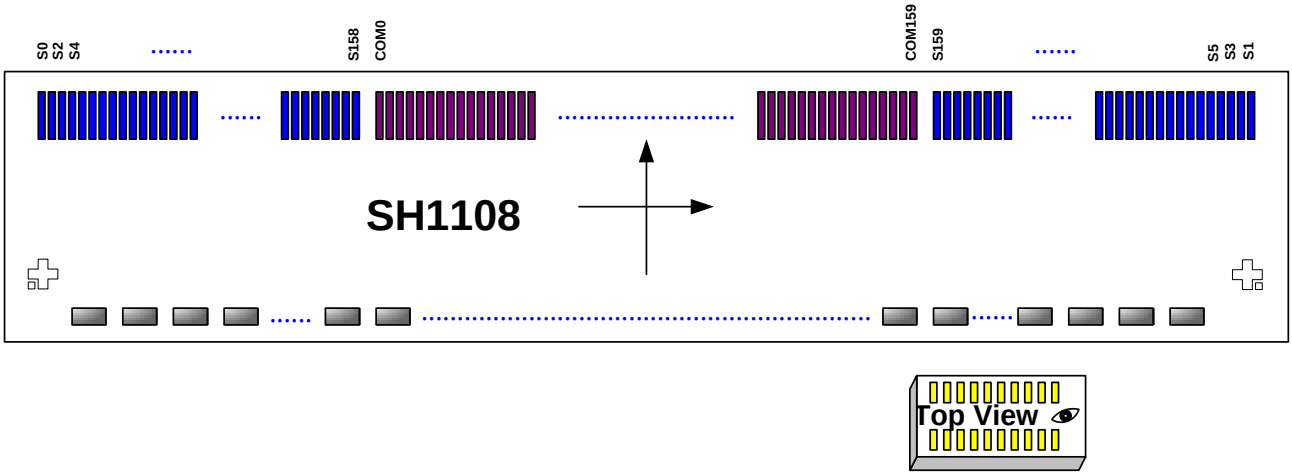
OLED Drive Pads

Pad NO.	Symbol	I/O	Description
331~410	SEG0,2, - 158	O	These pads are even Segment signal output for OLED display.
87~166	SEG1,3 -159	O	These pads are odd Segment signal output for OLED display.
168~260, 263~329	COM0 - 159	O	These pads are Common signal output for OLED display.

Test Pads

Pad NO.	Symbol	I/O	Description
51	TEST1	I	Test pad, internal pull low, no connection for user.
52	TEST2	O	Test pad, no connection for user.
53	TEST3	I	Test pad, no connection for user.
1~2,69~73, 84~86,167, 261~262,330, 411	Dummy	-	Dummy pads, no connection for user

Pad Configuration



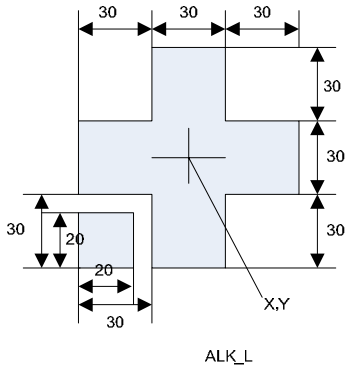
Chip Outline Dimensions

Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	10050	736
Chip height	All pads	300	
Bump size	I/O	95	40
	SEG	15	110
	COM	15	110
Pad pitch	COM	30	
	SEG	28	
	I/O	110	
Bump height	All pads	9±2	

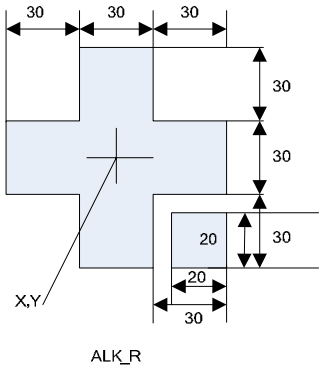
Alignment Mark Location

Unit: μm

NO	X	Y
ALK_L	-4888	-196
ALK_R	4888	-196



ALK_L



ALK_R

Pad Location (Total: pads) unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY	-4888	-316	82	GND	4455	-316	163	SEG[153]	2819	285	244	COM[83]	240	285
2	DUMMY	-4741	-316	83	GND	4598	-316	164	SEG[155]	2791	285	245	COM[82]	210	285
3	GND	-4598	-316	84	DUMMY	4741	-316	165	SEG[157]	2763	285	246	COM[81]	180	285
4	GND	-4455	-316	85	DUMMY	4888	-316	166	SEG[159]	2735	285	247	COM[80]	150	285
5	GND	-4312	-316	86	DUMMY	4975	285	167	DUMMY	2550	285	248	COM[79]	120	285
6	GND	-4169	-316	87	SEG[1]	4947	285	168	COM[159]	2520	285	249	COM[78]	90	285
7	GND	-4026	-316	88	SEG[3]	4919	285	169	COM[158]	2490	285	250	COM[77]	60	285
8	GND	-3883	-316	89	SEG[5]	4891	285	170	COM[157]	2460	285	251	COM[76]	30	285
9	VPP	-3740	-316	90	SEG[7]	4863	285	171	COM[156]	2430	285	252	COM[75]	0	285
10	VPP	-3630	-316	91	SEG[9]	4835	285	172	COM[155]	2400	285	253	COM[74]	-30	285
11	VPP	-3520	-316	92	SEG[11]	4807	285	173	COM[154]	2370	285	254	COM[73]	-60	285
12	VPP	-3410	-316	93	SEG[13]	4779	285	174	COM[153]	2340	285	255	COM[72]	-90	285
13	VSL	-3300	-316	94	SEG[15]	4751	285	175	COM[152]	2310	285	256	COM[71]	-120	285
14	VSL	-3190	-316	95	SEG[17]	4723	285	176	COM[151]	2280	285	257	COM[70]	-150	285
15	VSEGM	-3080	-316	96	SEG[19]	4695	285	177	COM[150]	2250	285	258	COM[69]	-180	285
16	VSEGM	-2970	-316	97	SEG[21]	4667	285	178	COM[149]	2220	285	259	COM[68]	-210	285
17	VSEGM	-2860	-316	98	SEG[23]	4639	285	179	COM[148]	2190	285	260	COM[67]	-240	285
18	VCOMH	-2750	-316	99	SEG[25]	4611	285	180	COM[147]	2160	285	261	DUMMY	-270	285
19	VCOMH	-2640	-316	100	SEG[27]	4583	285	181	COM[146]	2130	285	262	DUMMY	-480	285
20	VCOMH	-2530	-316	101	SEG[29]	4555	285	182	COM[145]	2100	285	263	COM[66]	-510	285
21	SW	-2420	-316	102	SEG[31]	4527	285	183	COM[144]	2070	285	264	COM[65]	-540	285
22	SW	-2310	-316	103	SEG[33]	4499	285	184	COM[143]	2040	285	265	COM[64]	-570	285
23	AVDD	-2200	-316	104	SEG[35]	4471	285	185	COM[142]	2010	285	266	COM[63]	-600	285
24	AVDD	-2090	-316	105	SEG[37]	4443	285	186	COM[141]	1980	285	267	COM[62]	-630	285
25	VBREF	-1980	-316	106	SEG[39]	4415	285	187	COM[140]	1950	285	268	COM[61]	-660	285
26	FB	-1870	-316	107	SEG[41]	4387	285	188	COM[139]	1920	285	269	COM[60]	-690	285
27	SENSE	-1760	-316	108	SEG[43]	4359	285	189	COM[138]	1890	285	270	COM[59]	-720	285
28	VPP	-1650	-316	109	SEG[45]	4331	285	190	COM[137]	1860	285	271	COM[58]	-750	285
29	VPP	-1540	-316	110	SEG[47]	4303	285	191	COM[136]	1830	285	272	COM[57]	-780	285
30	DUMMY	-1430	-316	111	SEG[49]	4275	285	192	COM[135]	1800	285	273	COM[56]	-810	285
31	VSSA	-1320	-316	112	SEG[51]	4247	285	193	COM[134]	1770	285	274	COM[55]	-840	285
32	GND(ana)	-1210	-316	113	SEG[53]	4219	285	194	COM[133]	1740	285	275	COM[54]	-870	285
33	GND(logic)	-1100	-316	114	SEG[55]	4191	285	195	COM[132]	1710	285	276	COM[53]	-900	285
34	GND(buf)	-990	-316	115	SEG[57]	4163	285	196	COM[131]	1680	285	277	COM[52]	-930	285
35	VCL	-880	-316	116	SEG[59]	4135	285	197	COM[130]	1650	285	278	COM[51]	-960	285
36	VCL	-770	-316	117	SEG[61]	4107	285	198	COM[129]	1620	285	279	COM[50]	-990	285
37	VCL	-660	-316	118	SEG[63]	4079	285	199	COM[128]	1590	285	280	COM[49]	-1020	285
38	VCL	-550	-316	119	SEG[65]	4051	285	200	COM[127]	1560	285	281	COM[48]	-1050	285
39	VCL	-440	-316	120	SEG[67]	4023	285	201	COM[126]	1530	285	282	COM[47]	-1080	285
40	CLS	-330	-316	121	SEG[69]	3995	285	202	COM[125]	1500	285	283	COM[46]	-1110	285
41	VDD	-220	-316	122	SEG[71]	3967	285	203	COM[124]	1470	285	284	COM[45]	-1140	285
42	VDD	-110	-316	123	SEG[73]	3939	285	204	COM[123]	1440	285	285	COM[44]	-1170	285
43	IM0	0	-316	124	SEG[75]	3911	285	205	COM[122]	1410	285	286	COM[43]	-1200	285
44	GND	110	-316	125	SEG[77]	3883	285	206	COM[121]	1380	285	287	COM[42]	-1230	285
45	IM1	220	-316	126	SEG[79]	3855	285	207	COM[120]	1350	285	288	COM[41]	-1260	285
46	VDD	330	-316	127	SEG[81]	3827	285	208	COM[119]	1320	285	289	COM[40]	-1290	285
47	IM2	440	-316	128	SEG[83]	3799	285	209	COM[118]	1290	285	290	COM[39]	-1320	285
48	GND	550	-316	129	SEG[85]	3771	285	210	COM[117]	1260	285	291	COM[38]	-1350	285
49	IREF	660	-316	130	SEG[87]	3743	285	211	COM[116]	1230	285	292	COM[37]	-1380	285
50	IREF	770	-316	131	SEG[89]	3715	285	212	COM[115]	1200	285	293	COM[36]	-1410	285
51	TEST1	880	-316	132	SEG[91]	3687	285	213	COM[114]	1170	285	294	COM[35]	-1440	285
52	TEST2	990	-316	133	SEG[93]	3659	285	214	COM[113]	1140	285	295	COM[34]	-1470	285
53	TEST3	1100	-316	134	SEG[95]	3631	285	215	COM[112]	1110	285	296	COM[33]	-1500	285
54	FRM	1210	-316	135	SEG[97]	3603	285	216	COM[111]	1080	285	297	COM[32]	-1530	285
55	CL	1320	-316	136	SEG[99]	3575	285	217	COM[110]	1050	285	298	COM[31]	-1560	285
56	CSB	1430	-316	137	SEG[101]	3547	285	218	COM[109]	1020	285	299	COM[30]	-1590	285
57	RESB	1540	-316	138	SEG[103]	3519	285	219	COM[108]	990	285	300	COM[29]	-1620	285
58	A0	1650	-316	139	SEG[105]	3491	285	220	COM[107]	960	285	301	COM[28]	-1650	285
59	WRB	1760	-316	140	SEG[107]	3463	285	221	COM[106]	930	285	302	COM[27]	-1680	285
60	RDB	1870	-316	141	SEG[109]	3435	285	222	COM[105]	900	285	303	COM[26]	-1710	285
61	D[0]	1980	-316	142	SEG[111]	3407	285	223	COM[104]	870	285	304	COM[25]	-1740	285
62	D[1]	2090	-316	143	SEG[113]	3379	285	224	COM[103]	840	285	305	COM[24]	-1770	285
63	D[2]	2200	-316	144	SEG[115]	3351	285	225	COM[102]	810	285	306	COM[23]	-1800	285
64	D[3]	2310	-316	145	SEG[117]	3323	285	226	COM[101]	780	285	307	COM[22]	-1830	285
65	D[4]	2420	-316	146	SEG[119]	3295	285	227	COM[100]	750	285	308	COM[21]	-1860	285
66	D[5]	2530	-316	147	SEG[121]	3267	285	228	COM[99]	720	285	309	COM[20]	-1890	285
67	D[6]	2640	-316	148	SEG[123]	3239	285	229	COM[98]	690	285	310	COM[19]	-1920	285
68	D[7]	2750	-316	149	SEG[125]	3211	285	230	COM[97]	660	285	311	COM[18]	-1950	285
69	DUMMY	2860	-316	150	SEG[127]	3183	285	231	COM[96]	630	285	312	COM[17]	-1980	285
70	DUMMY	2970	-316	151	SEG[129]	3155	285	232	COM[95]	600	285	313	COM[16]	-2010	285
71	DUMMY	3080	-316	152	SEG[131]	3127	285	233	COM[94]	570	285	314	COM[15]	-2040	285
72	DUMMY	3190	-316	153	SEG[133]	3099	285	234	COM[93]	540	285	315	COM[14]	-2070	285
73	DUMMY	3300	-316	154	SEG[135]	3071	285	235	COM[92]	510	285	316	COM[13]	-2100	285
74	VPP	3410	-316	155	SEG[137]	3043	285	236	COM[91]	480	285	317	COM[12]	-2130	285
75	VPP	3520	-316	156	SEG[139]	3015	285	237	COM[90]	450	285	318	COM[11]	-2160	285
76	VPP	3630	-316	157	SEG[141]	2987	285	238	COM[89]	420	285	319	COM[10]	-2190	285
77	VPP	3740	-316	158	SEG[143]	2959	285	239	COM[88]	390	285	320	COM[9]	-2220	285
78	GND	3883	-316	159	SEG[145]	2931	285	240	COM[87]	360	285	321	COM[8]	-2250	285
79	GND	4026	-316	160	SEG[147]	2903	285	241	COM[86]	330	285	322	COM[7]	-2280	285
80	GND	4169	-316	161	SEG[149]	2875	285	242	COM[85]	300	285	323	COM[6]	-2310	285
81	GND	4312	-316	162	SEG[151]	2847	285	243	COM[84]	270	285	324	COM[5]	-2340	285

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
325	COM[4]	-2370	285	406	SEG[8]	-4835	285
326	COM[3]	-2400	285	407	SEG[6]	-4863	285
327	COM[2]	-2430	285	408	SEG[4]	-4891	285
328	COM[1]	-2460	285	409	SEG[2]	-4919	285
329	COM[0]	-2490	285	410	SEG[0]	-4947	285
330	DUMMY	-2520	285	411	DUMMY	-4975	285
331	SEG[158]	-2735	285				
332	SEG[156]	-2763	285				
333	SEG[154]	-2791	285				
334	SEG[152]	-2819	285				
335	SEG[150]	-2847	285				
336	SEG[148]	-2875	285				
337	SEG[146]	-2903	285				
338	SEG[144]	-2931	285				
339	SEG[142]	-2959	285				
340	SEG[140]	-2987	285				
341	SEG[138]	-3015	285				
342	SEG[136]	-3043	285				
343	SEG[134]	-3071	285				
344	SEG[132]	-3099	285				
345	SEG[130]	-3127	285				
346	SEG[128]	-3155	285				
347	SEG[126]	-3183	285				
348	SEG[124]	-3211	285				
349	SEG[122]	-3239	285				
350	SEG[120]	-3267	285				
351	SEG[118]	-3295	285				
352	SEG[116]	-3323	285				
353	SEG[114]	-3351	285				
354	SEG[112]	-3379	285				
355	SEG[110]	-3407	285				
356	SEG[108]	-3435	285				
357	SEG[106]	-3463	285				
358	SEG[104]	-3491	285				
359	SEG[102]	-3519	285				
360	SEG[100]	-3547	285				
361	SEG[98]	-3575	285				
362	SEG[96]	-3603	285				
363	SEG[94]	-3631	285				
364	SEG[92]	-3659	285				
365	SEG[90]	-3687	285				
366	SEG[88]	-3715	285				
367	SEG[86]	-3743	285				
368	SEG[84]	-3771	285				
369	SEG[82]	-3799	285				
370	SEG[80]	-3827	285				
371	SEG[78]	-3855	285				
372	SEG[76]	-3883	285				
373	SEG[74]	-3911	285				
374	SEG[72]	-3939	285				
375	SEG[70]	-3967	285				
376	SEG[68]	-3995	285				
377	SEG[66]	-4023	285				
378	SEG[64]	-4051	285				
379	SEG[62]	-4079	285				
380	SEG[60]	-4107	285				
381	SEG[58]	-4135	285				
382	SEG[56]	-4163	285				
383	SEG[54]	-4191	285				
384	SEG[52]	-4219	285				
385	SEG[50]	-4247	285				
386	SEG[48]	-4275	285				
387	SEG[46]	-4303	285				
388	SEG[44]	-4331	285				
389	SEG[42]	-4359	285				
390	SEG[40]	-4387	285				
391	SEG[38]	-4415	285				
392	SEG[36]	-4443	285				
393	SEG[34]	-4471	285				
394	SEG[32]	-4499	285				
395	SEG[30]	-4527	285				
396	SEG[28]	-4555	285				
397	SEG[26]	-4583	285				
398	SEG[24]	-4611	285				
399	SEG[22]	-4639	285				
400	SEG[20]	-4667	285				
401	SEG[18]	-4695	285				
402	SEG[16]	-4723	285				
403	SEG[14]	-4751	285				
404	SEG[12]	-4779	285				
405	SEG[10]	-4807	285				

Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) or I^2C Interface can be selected by different selections of IM0~2 as shown in Table 1.

Table 1

Interface	Config			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
6800	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	A0	$\overline{RES}$
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
4-Wire SPI	0	0	0	Hz (Note1)						SI	SCL	Pull High or Low		$\overline{CS}$	A0	$\overline{RES}$
3-Wire SPI	1	0	0	Hz (Note1)						SI	SCL	Pull High or Low		$\overline{CS}$	Pull Low	$\overline{RES}$
I^2C	0	1	0	Hz (Note1)						SDA	SCL	Pull High or Low		Pull Low	SA0	$\overline{RES}$

Note1: When Serial Interface (SPI) or I^2C Interface is selected, D7~D2 is Hz. D7~D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~D2 unconnected.

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R / $\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. When $\overline{WR}$ (R / $\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R / $\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table 2.

Table 2

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	0	1	6800 microprocessor bus	$\overline{CS}$	A0	E	R / $\overline{W}$	D0 to D7

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in figure 2 below.

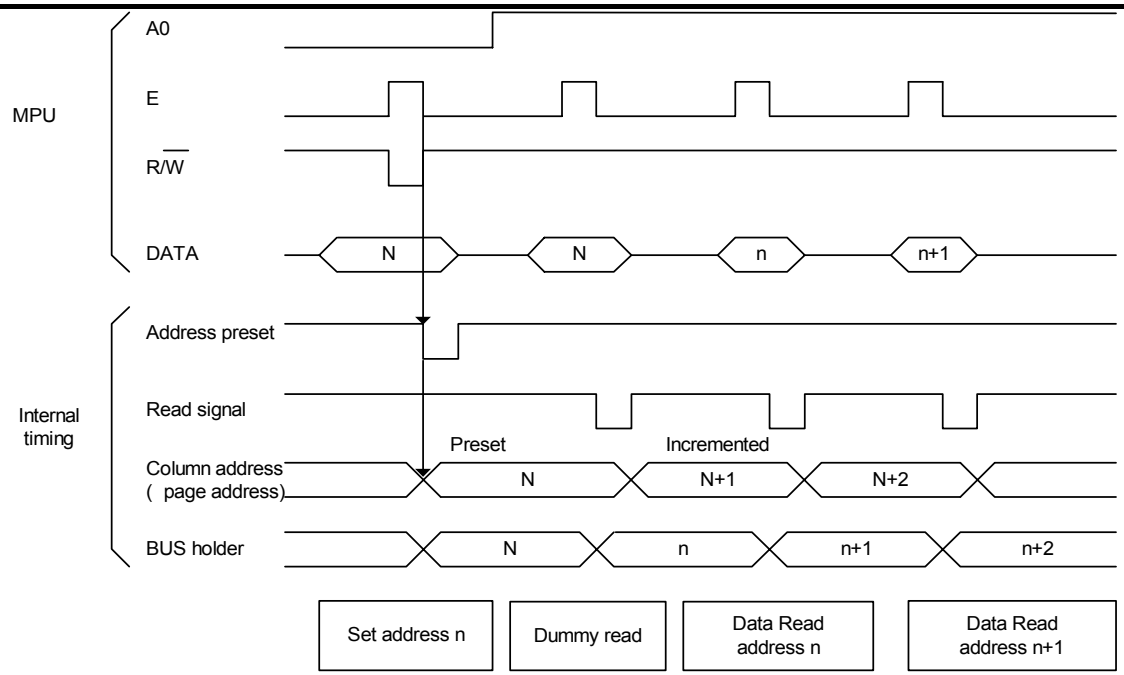


Figure 2

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R / $\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by A0 signal. The $\overline{WR}$ (R / $\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table 3.

Table 3

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
0	1	1	8080 microprocessor bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1108 identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ (R / $\overline{W}$) signals.

Table 4

Common	6800 processor	8080 processor		Function
A0	(R / $\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6 … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM (A0=1) or command register (A0=0) in the same clock. See figure 3

Table 5

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	0	0	4-wire SPI	$\overline{CS}$	A0	-	-	SCL	SI	(Hz)

Note: "-" pin must always be HIGH or LOW. D7~D2 is recommended to connect the VDD or GND. It's also allowed to leave D7~D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

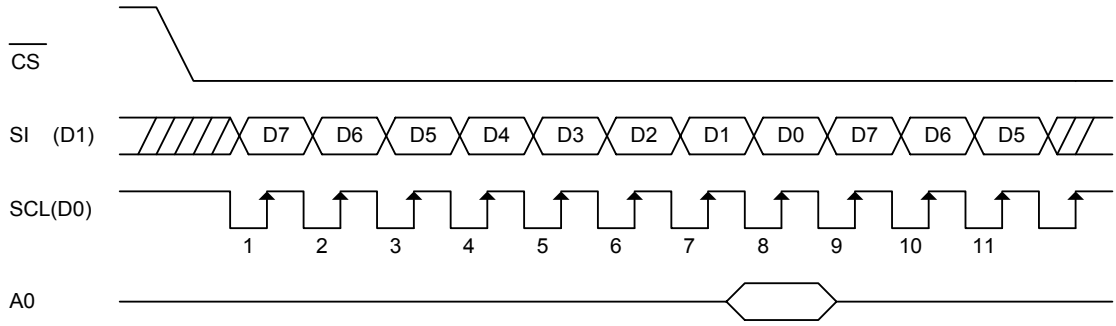


Figure 3 4-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into a 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6 … D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$ =1) or command register ($D/\overline{C}$ =0). See figure 4.

Table 6

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
1	0	0	3-wire SPI	$\overline{CS}$	Pull Low	-	-	SCL	SI	(Hz)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended.

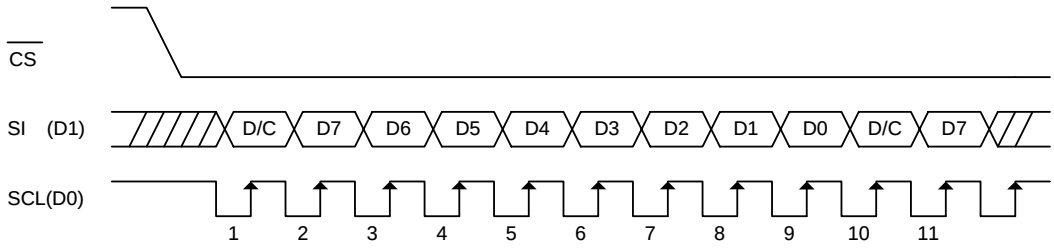


Figure4 3-wire SPI data transfer

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

I²C-bus Interface

The SH1108 can transfer data via a standard I²C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status and RAM data can be read out of the chip.

Table 7

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	1	0	I²C Interface	Pull Low	SA0	-	-	SCL	SDA	(Hz)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the V_{DD} or GND. It is also allowed to leave D7~ D2 unconnected.

$\overline{CS}$ Signal could always pull low in I²C-bus application.

Characteristics of the I²C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of V_{DD}.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

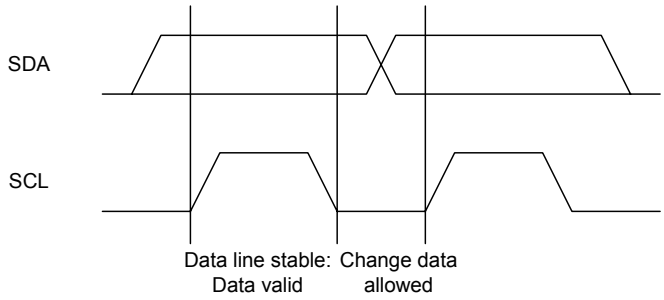


Figure 5 Bit Transfer

Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

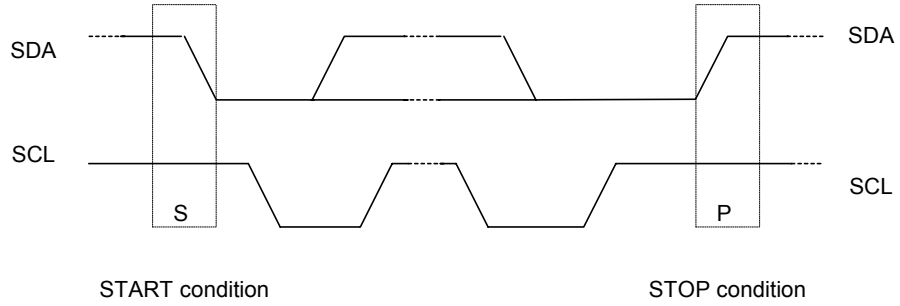


Figure 6 Start and Stop conditions

System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

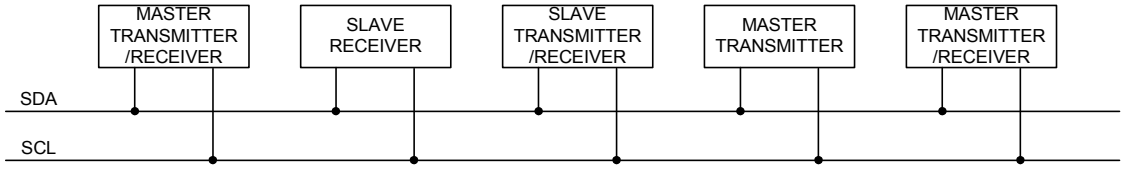


Figure 7 System configuration

Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

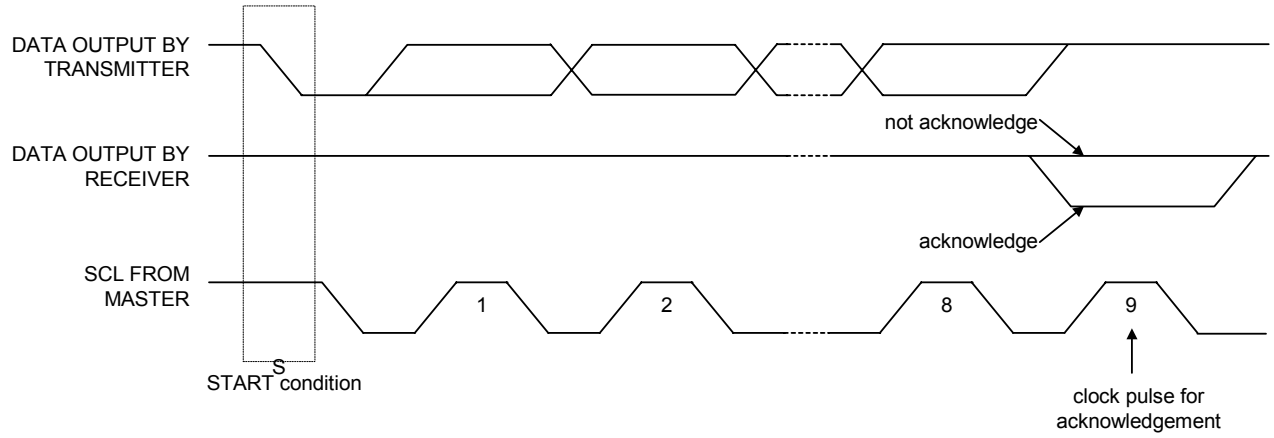


Figure 8 Acknowledge

Protocol

The SH1108 supports both read and write access. The $R/\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I^2C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the SH1108. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1 (VDD). The I^2C-bus protocol is illustrated in Fig.7. The sequence is initiated with a START condition (S) from the I^2C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I^2C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and $D/\overline{C}$ (note1), plus a data byte (see Fig.9). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the $D/\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended SH1108 device. If the $D/\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I^2C-bus master issues a stop condition (P). If the $R/\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the $D/\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

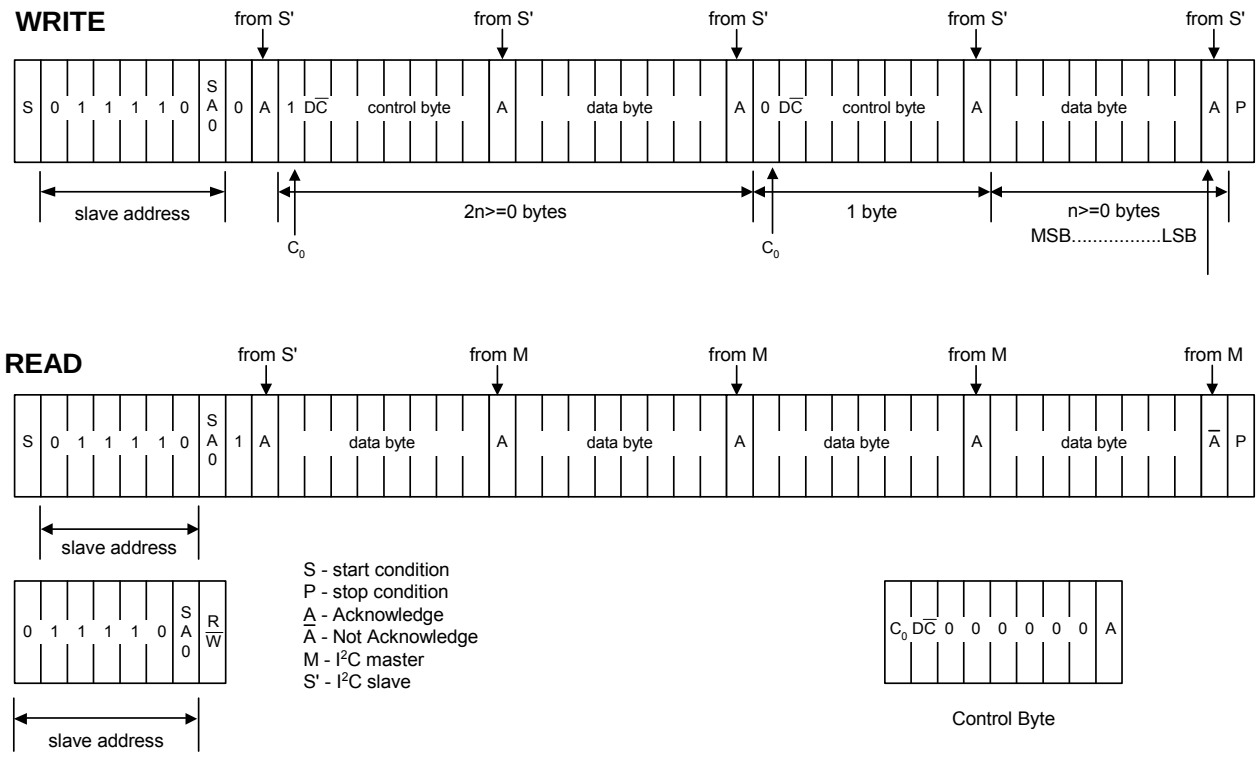


Figure 9 I²C Protocol

Note1:

1. Co＝“ 0 ”: The last control byte , only data bytes to follow,
   Co＝“ 1 ”: Next two bytes are a data byte and another control byte;
2. D/C̄ ＝“ 0 ”: The data byte is for command operation,
   D/C̄ ＝“ 1 ”: The data byte is for RAM operation.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160 X 160 bits.

For mechanical flexibility, re-mapping on segment and the direction of common outputs can be selected by software.

The Page Address Circuit

As shown in figure 10, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access in page addressing mode and it is incremented (+1) with each display data read/write command in vertical addressing mode.

The Column Address Circuit

As shown in figure 10, the display data RAM column address is specified by the Column Address Set command. The specified column address or page address (it depends on the mode of RAM addressing) is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 9FH to page 1 column 00H in page addressing mode, it is necessary to re-specify both the page address and the column address.

The Display Address Circuit

The display address circuit, as shown in figure 10, specifies the display address relating to the common output when the contents of the display data RAM are displayed. (This is the COM0 output when the common output mode is normal and the COM159 output for SH1108 when the common output mode is reversed. The display area is a 160-line area for the SH1108 from the first display address. As shown in Table 8, the common driver direction select command can be used to reverse the relationship between the display data RAM display address and the common output.

Table 8

Common Output Scan Direction	COM0	…	COM159
D= “0”	00 (H) →	Display Address	→ 9F (H)
D= “1”	9F (H) ←	Display Address	← 00 (H)

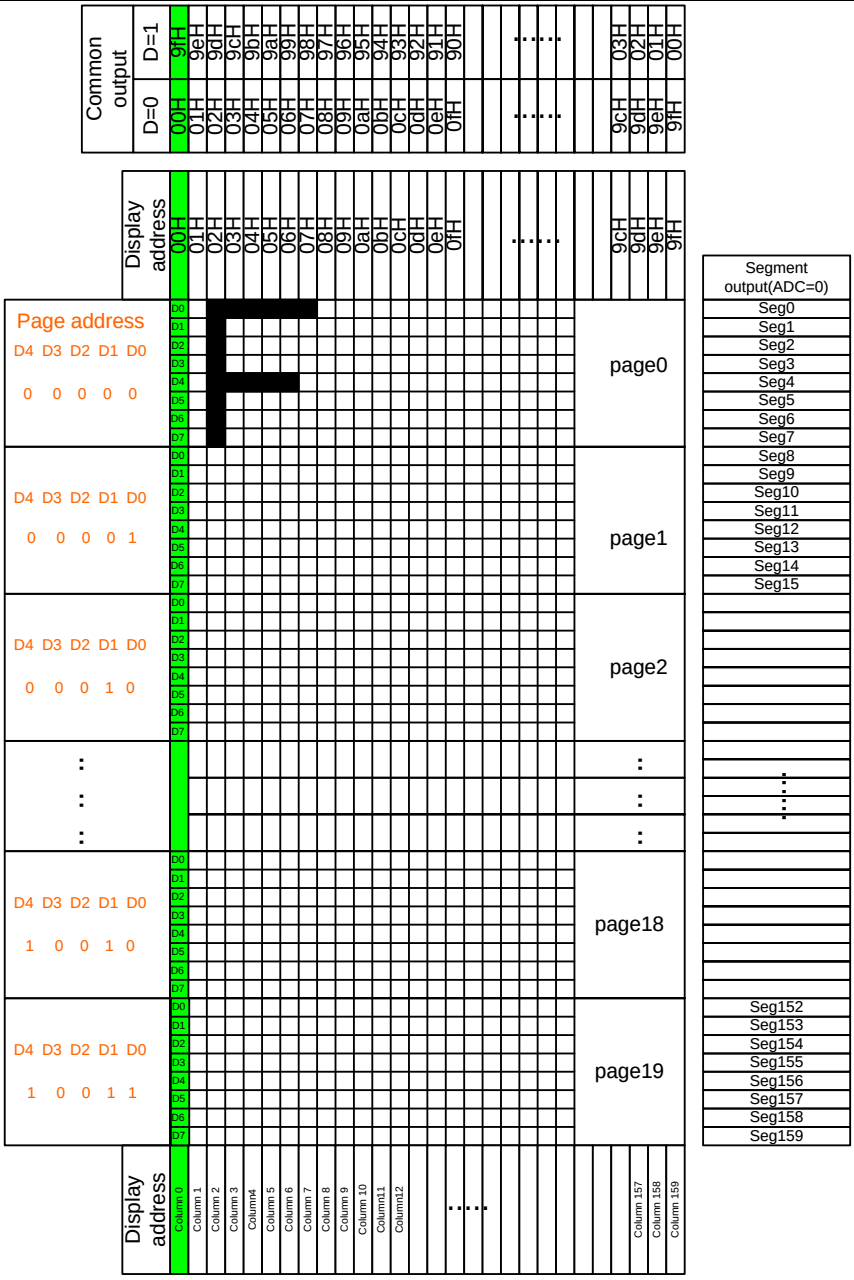


Figure 10 (a) RAM map example: ADC=0(POR)

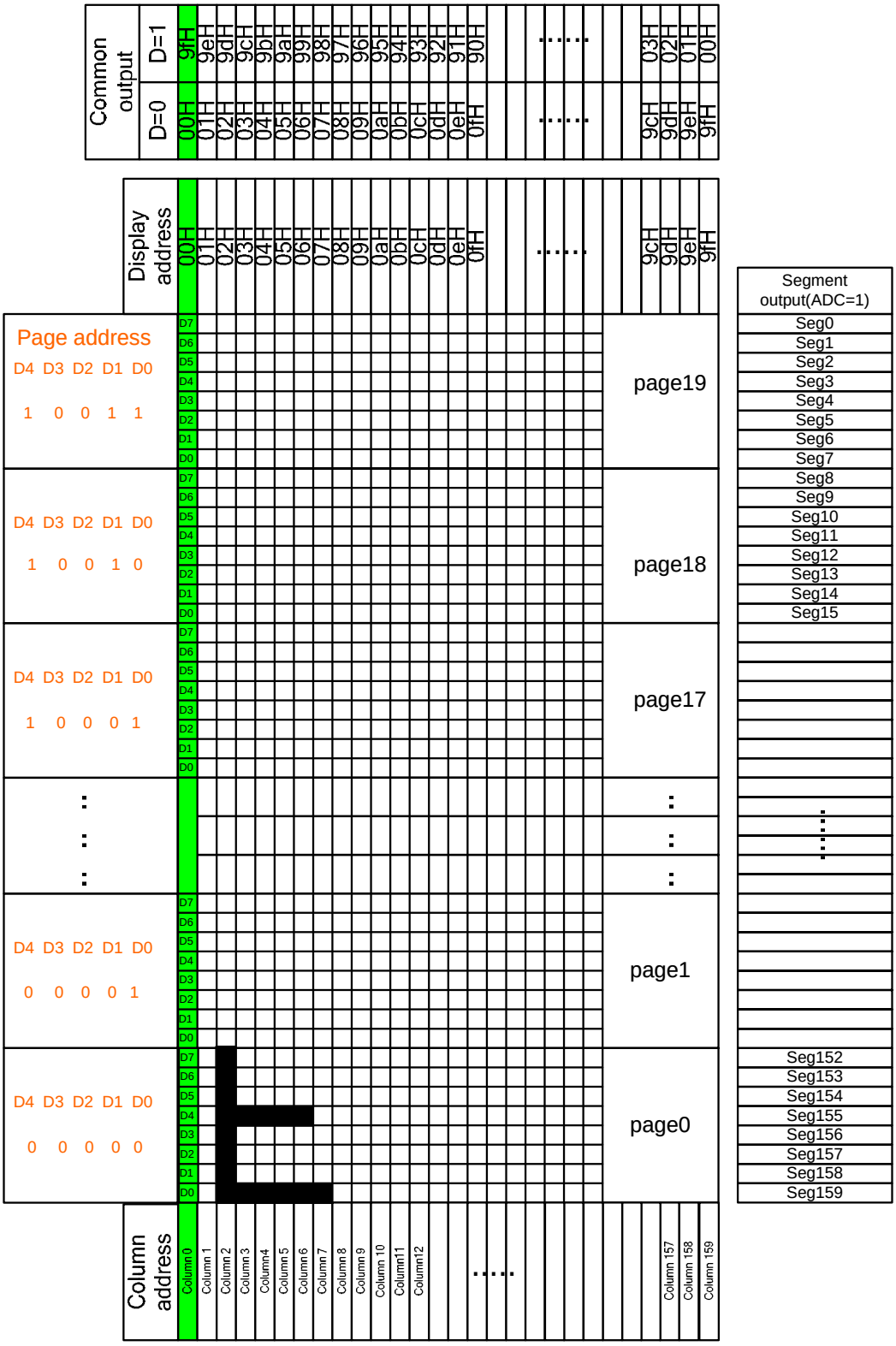


Figure 10（b）RAM map example: ADC=1(Seg remap)

The Oscillator Circuit

This is a RC type oscillator (Figure 11) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation stops and the display clock is inputted through the CL terminal.

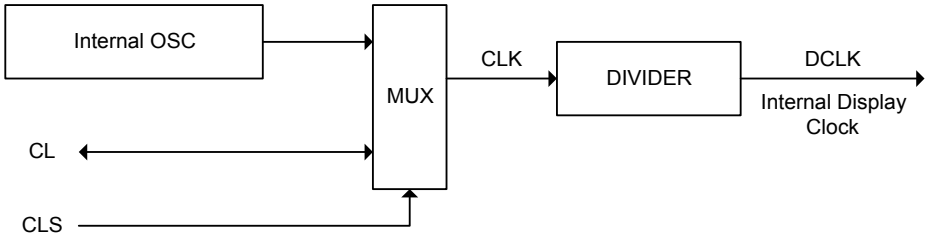


Figure 11

DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for hand held applications. In SH1108, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure 12) can generate a high voltage supply VPP from a low voltage supply input AVDD. VPP is the voltage supply to the OLED driver block

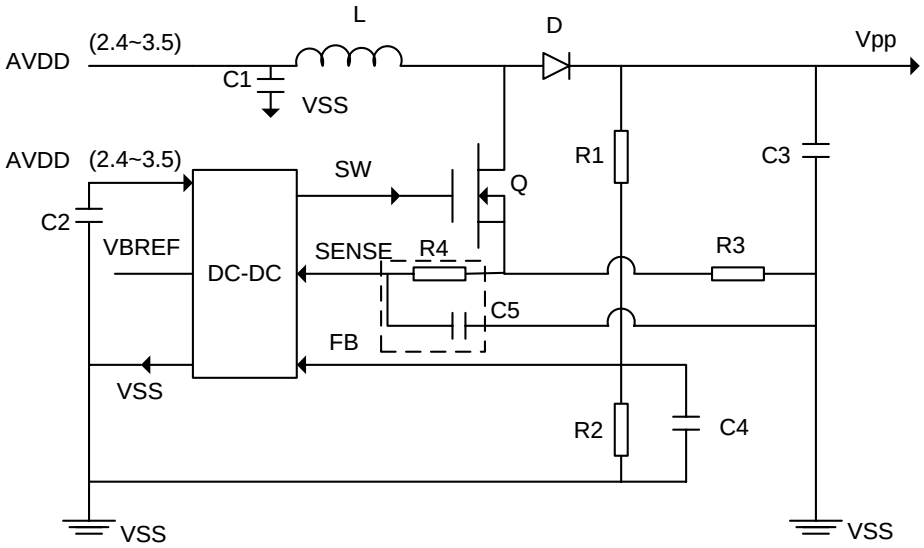


Figure 12

V_{PP}= $(1+\frac{R1}{R2})$ X V_{BREF}, (R_2: 80 - 120k Ω)

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. VPP and VDD are external power supplies. IREF is a reference current source for segment current drivers, it can change the brightness of the screen and the value depends on the resistance of R_{ref} and Vpp:

When Vpp=15V, contrast = 0xff, the value of resistor R_{ref} can be found as Table 9:

Table 9

IREF	15.625μA	11.25μA	6.25μA
I_{seg}(Max)	500μA	360μA	200μA
R_{ref}	750KΩ	1MΩ	1.8MΩ

Common Drivers/Segment Drivers

Segment drivers deliver 160 current sources to drive OLED panel. The driving current can be adjusted up to 500μA with 256 steps. Common drivers generate voltage scanning pulses.

Reset Circuit

When the $\overline{RES}$ input falls to “L”, these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 160 X 160 Display mode.
3. Normal segment and display data mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface.
5. Column address counter is set at 0.
6. Contrast control register is set at 80H.
7. Normal common scan direction
8. Internal DC-DC is selected.

Commands

The SH1108 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R / $\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R / $\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below. When the serial interface is selected, the input data is starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)

2. Set Higher Column Address: (10H - 19H)

Specify column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 159 is accessed (In page addressing mode).The page address is not changed during this time.

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
High bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Low bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:								:
1	0	0	1	1	1	1	1	159

Note: Don't use any commands not mentioned above.

3. Set Memory addressing mode (20H - 21H)

There are two different memory addressing modes in SH1108: page addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes, “COL” means column.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	D

■ Page addressing mode (20H) (POR)

In page addressing mode, after the display RAM is read/ written, the column address is increased automatically by 1. If the column address reaches column end address, the column address is reset to column start address and page address is not changed. Users have to set the new page and column addresses in order to access the next page RAM content. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the page and column address for page addressing mode is shown in figure 13-1 and figure 13-2.

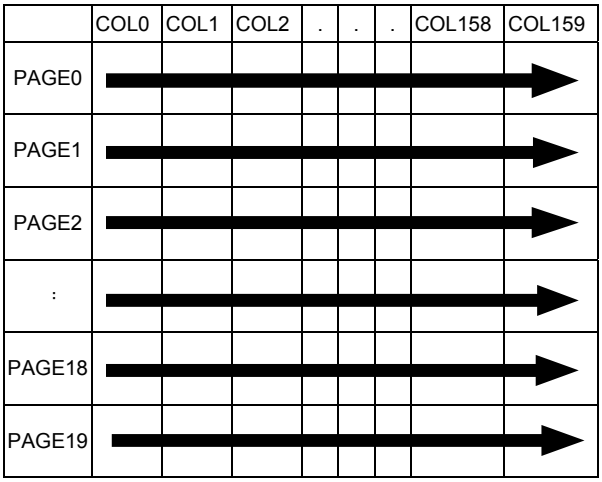


Figure13-1(a)

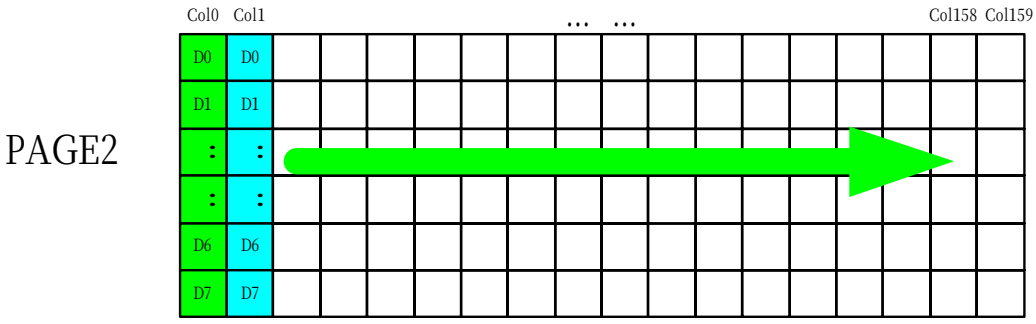


Figure13-1(b)

Figure13-1 page addressing mode (Seg-remap=0)

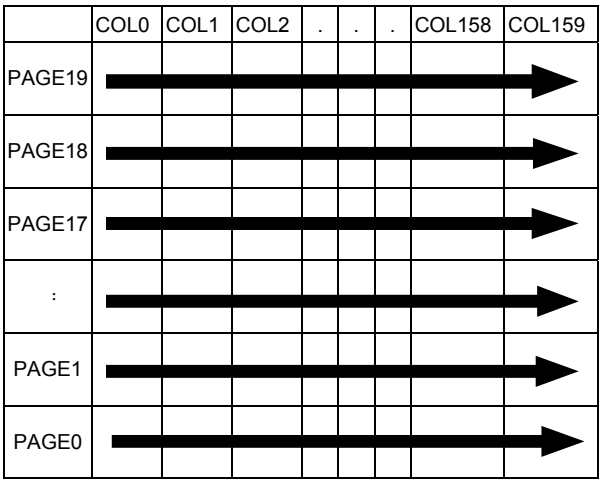


Figure13-2(a)

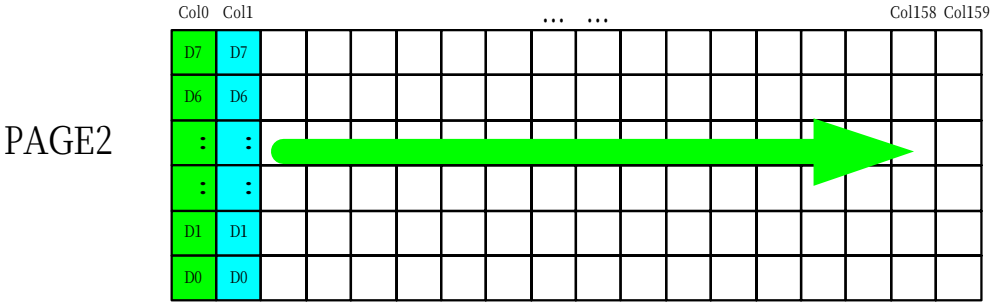


Figure13-2(b)

Figure13-2 page addressing mode (Seg-remap=1)

■ Vertical addressing mode: (21H)

In vertical addressing mode, after the display RAM is read/ written, the page address is increased automatically by 1. If the page address reaches the page end address, the page address is reset to page start address and column address is not changed. Users have to set the new page and column addresses in order to access the next column. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the page and column address for vertical addressing mode is shown in Figure 13-3 and Figure 13-4.

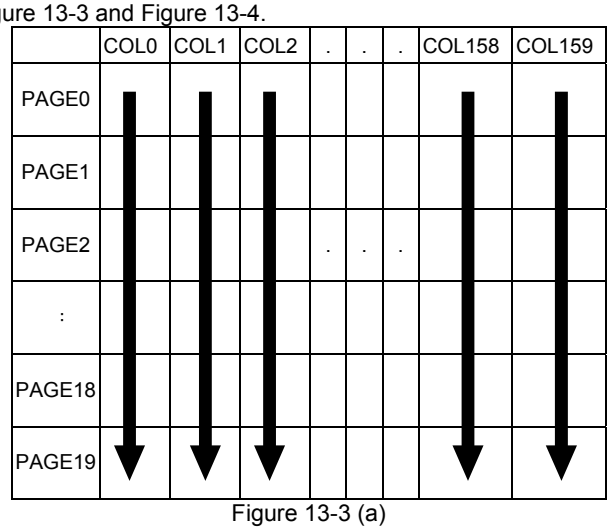


Figure 13-3 (a)

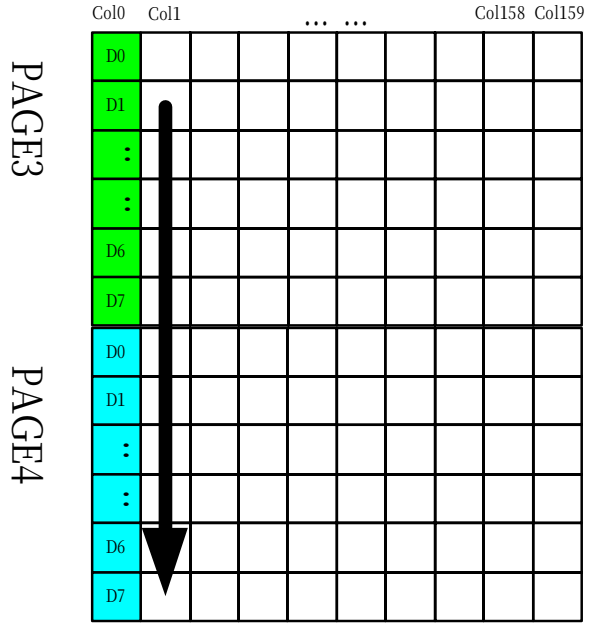


Figure13-3 (b)

Figure 13-3 Vertical addressing mode (Seg remap=0)

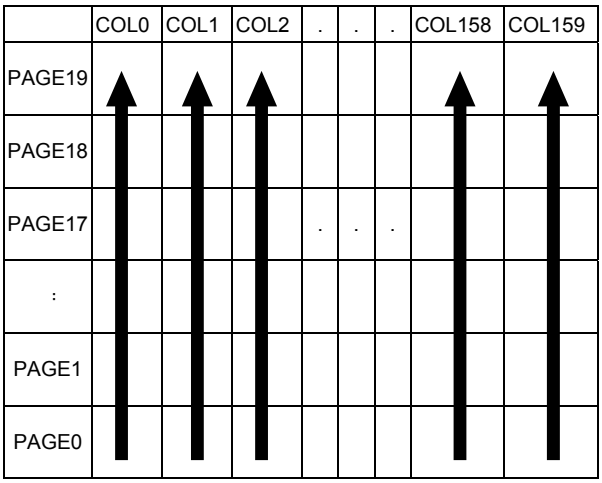


Figure13-4 (a)

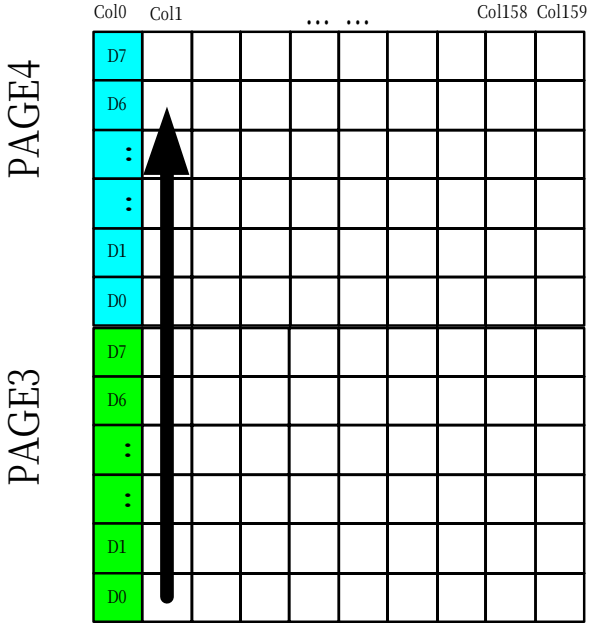


Figure13-4 (b)
13-4 Vertical addressing mode (Seg remap=1)

4. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: $I_{SEG} = \alpha/256 \times I_{REF} \times$ scale factor

Where: α is contrast step; IREF is reference current equals 15.625μA; Scale factor = 32

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	$\frac{E}{\overline{RD}}$	$\frac{R/\overline{W}}{\overline{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

5. Set Segment Re-map: (A0H - A1H)

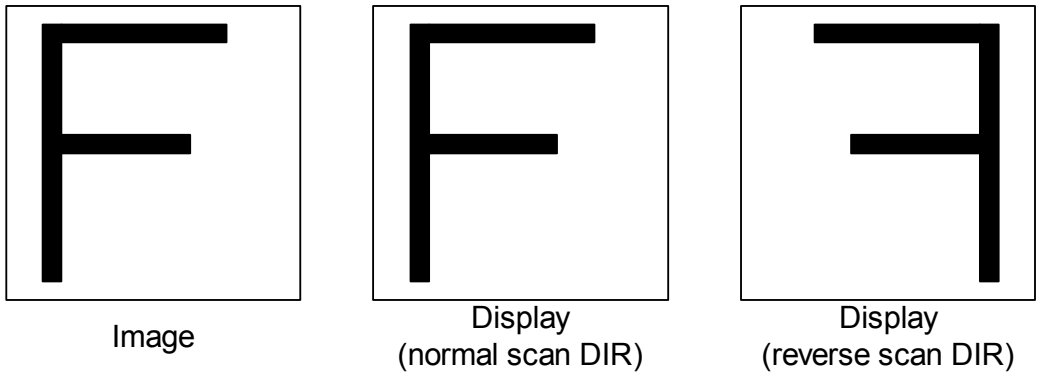
Change the relationship between RAM page address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the page address section of figure 10. When display data is written or read, the column address or page address (depends on the memory addressing mode) is incremented by 1 as shown in figure 2.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

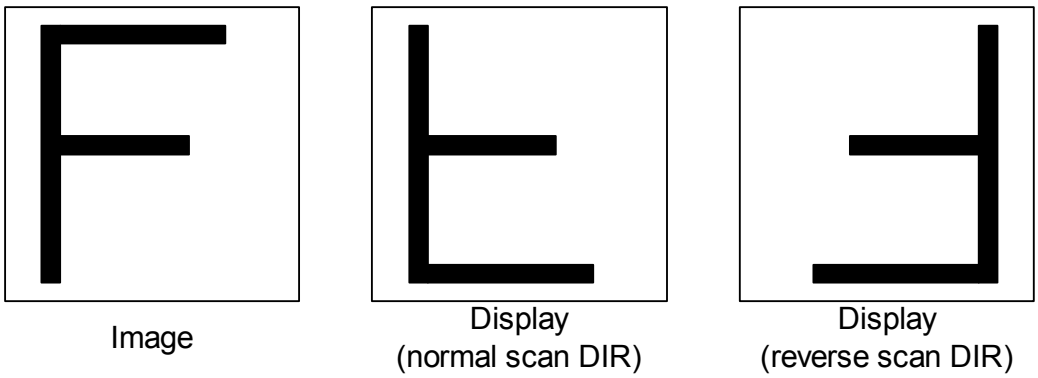
When ADC = “L”, the down rotates (normal direction). (POR)

When ADC = “H”, the up rotates (reverse direction).

The display examples of Segment Re-map command are showed in figure 14



(a) ADC=0



(b) ADC=1(segment remap)

Figure 14 the display example of Set Segment Re-map and common scan direction command

6. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (POR)

When D = “H”, the entire display ON status is provided.

7. Set Normal/Reverse Display: (A6H -A7H)

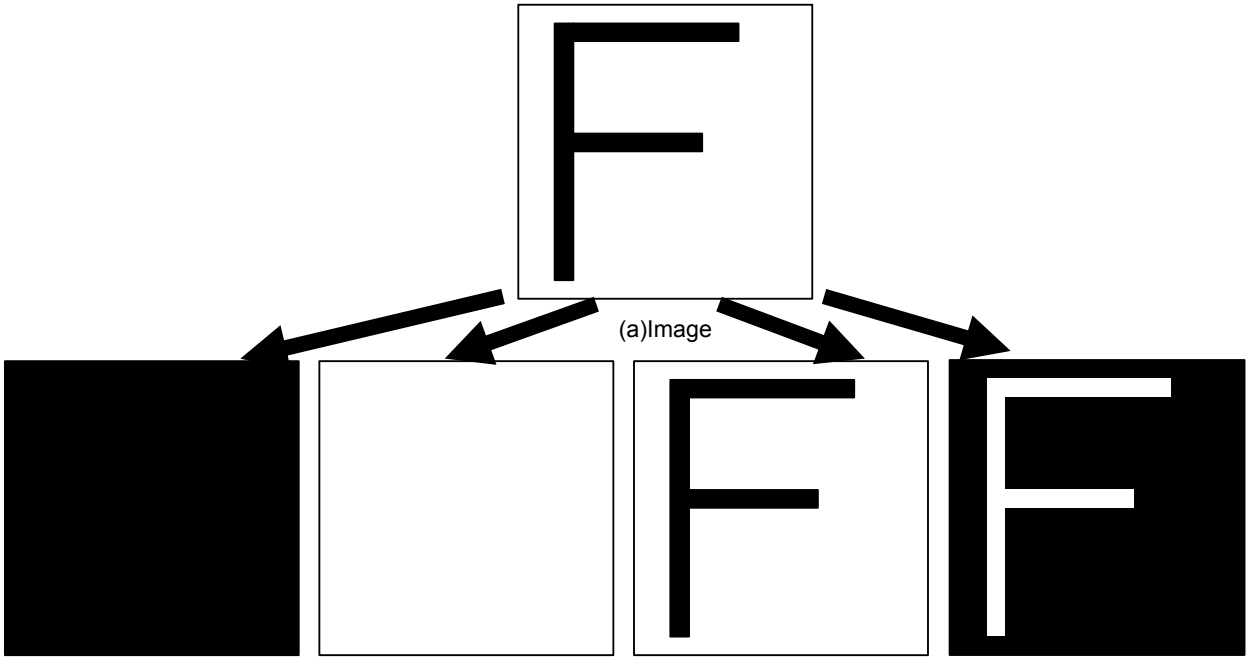
Reverse the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (POR)

When D = “H”, the RAM data is low, being OLED ON potential (reverse display)

The display example of Entire display off/on and normal/reverse command are showed in figure 15



(b) Display off (0xAE) (c) Entire display on (0xA5) (d) Normal display (0xA6) (e) Reverse display (0xA7)

Figure 15: display example of entire display on and normal/reverse

8. Display Resolution Control: (Double Bytes Command)

This command is used to control the display resolution. There are four resolution options: 64 COM×160 SEG；

96 COM×160 SEG；128 COM×160 SEG；160 COM×160 SEG；

■ Display Resolution Command Set (A9H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	1

■ Data of Display Resolution Set (00H – 03H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	0	0	0	D1	D0

D1-D0 defines common scan setting:

D1	D0	Display scan line	Column address	Display resolution
0	0	COM48 to COM111	Column48 to Column111	64 COM×160 SEG
0	1	COM32 to COM127	Column32 to Column127	96 COM×160 SEG
1	0	COM16 to COM143	Column16 to Column143	128 COM×160 SEG
1	1	COM0 to COM159	Column0 to Column159	160 COM (POR) ×160 SEG

Note: Don't use any commands not mentioned above for user.

9. Set DC-DC Setting: (Double Bytes Command)

This command is to control the DC-DC voltage converter status and the switch frequency. Issuing this command then Display ON command will turn on the converter. The panel display must be off while issuing this command.

- DC-DC Control Mode Set: (ADH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

- DC-DC ON/OFF Mode Set: (8AH - 8BH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	F2	F1	F0	D

When D = “L”, DC-DC is disable.

When D = “H”, DC-DC will be turned on when display on. (POR)

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used.
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

F2	F1	F0	Switch Frequency
0	0	0	0.6SF (POR)
0	0	1	0.7SF
0	1	0	0.8SF
0	1	1	0.9SF
1	0	0	1.0SF
1	0	1	1.1SF
1	1	0	1.2SF
1	1	1	1.3SF

500KHz-25%<SF<500KHz+35%

10. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (POR)

When D = “H”, Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and DC-DC circuit.

(2) Stops the OLED drive and outputs Hz as the segment/common driver output.

(3) Holds the display data and operation mode provided before the start of the sleep mode.

(4) The MPU can access to the built-in display RAM.

11. Set Page Address: (Double Bytes Command)

Specify page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

■ Page Address Command Set (B0H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	0	0	0

■ Data Of Page Address Set(00H – 13H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	A4	A3	A2	A1	A0

A4~A0 defines the page address

A4	A3	A2	A1	A0	Page Address
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19

Note: Don’t use any commands not mentioned above for user.

12. Set Common Output Scan Direction: (C0H – C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = “L”, Scan from COM0 to COM [N -1]. (POR)

When D = “H”, Scan from COM [N -1] to COM0.

13. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row and oscillator frequency.

- Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

- Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

A0	$\frac{E}{\overline{RD}}$	$\frac{R / \overline{W}}{\overline{WR}}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A3 - A0 defines the divide ration of the display clocks (DCLK). Divide Ration = A[3:0] +1.

A_3	A_2	A_1	A_0	Divide Ration
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A7 - A4 sets the oscillator frequency. Oscillator frequency increases with the value of A[7:4] and vice versa.

A_7	A_6	A_5	A_4	Oscillator Frequency of f_{OSC}
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	f_{OSC} (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

14. Set Dis-charge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK.

POR is 2 DCLKs.

- Pre-charge Period Mode Set: (D9H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

- Dis-charge/Pre-charge Period Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Pre-charge Period Adjust: (A3 - A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	Note
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Dis-charge Period Adjust: (A7 - A4)

A_7	A_6	A_5	A_4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Note:

When set A[3:0] =0, the period for display will increase 2 DCLKs. And there is no pre-charge period so that it will save power consumption.

15. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{COMH} = \beta_1 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_1	A[7:0]	β_1
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.442	22H	0.648
03H	0.449	23H	0.654
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.731
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.525	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770 (POR)
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.596	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H - FFH	1		

16. Set VSEGM Deselect Level: (Double Bytes Command)

This command is to set the VSEMG pad output voltage level at deselect stage.

■ VSEGM Deselect Level Mode Set: (DCH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VSEGM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{SEGM} = \beta_1 \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β_1	A[7:0]	β_1
00H	0.430	20H	0.635
01H	0.436	21H	0.642
02H	0.442	22H	0.648
03H	0.449	23H	0.654
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.731
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.525	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770 (POR)
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.596	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834
40H - FFH	1		

17. Set Discharge VSL Level (30H - 3FH)

This command is to set the Segment output discharge voltage level.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	1	D_3	D_2	D_1	D_0

This command is to set the segment discharge voltage level

D[3:0]	V_{SL}
00H	0V (Default)
01H	0.1 V_{REF}
02H	0.125 V_{REF}
03H	0.150 V_{REF}
04H	0.175 V_{REF}
05H	0.2 V_{REF}
06H	0.225 V_{REF}
07H	0.250 V_{REF}
08H	0.275 V_{REF}
09H	0.3 V_{REF}
0AH	0.325 V_{REF}
0BH	0.350 V_{REF}
0CH	0.375 V_{REF}
0DH	0.4 V_{REF}
0EH	0.425 V_{REF}
0FH	0.450 V_{REF}

18. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. In page addressing mode, once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. In vertical addressing mode, once read-modify-write is issued, page address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address or page address (it depends on the addressing mode) returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

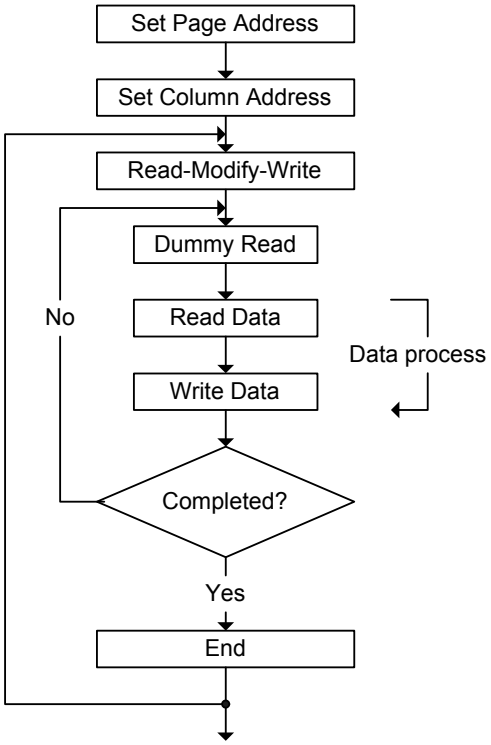


Figure 16

19. End: (EEH)

Cancels Read-Modify-Write mode and returns column address or page address (it depends on the RAM addressing mode) to the original address (when Read-Modify-Write is issued.)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

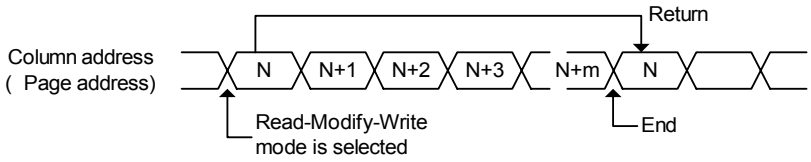


Figure 17

20. NOP: (E3H)

No Operation Command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

21. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

22. Read ID

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	ID					

BUSY: When high, the SH1108 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When it goes low, the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command.

ID： These bits contain the information of the chip. The output bits 001000(it means SH1108).

23. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address or page address (depends on the mode of memory addressing) is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2.Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3.Set memory addressing mode	0	1	0	0	0	1	0	0	0	0	D	D = 1, Vertical Addressing Mode D = 0, Page Addressing Mode (POR=20H)
4. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
5. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The down (0) or up (1) rotation. (POR = A0H)
6. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
7. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
8. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 81H)
DC-DC Setting Mode Set	0	1	0	1	0	0	0	F2	F1	F0	D	

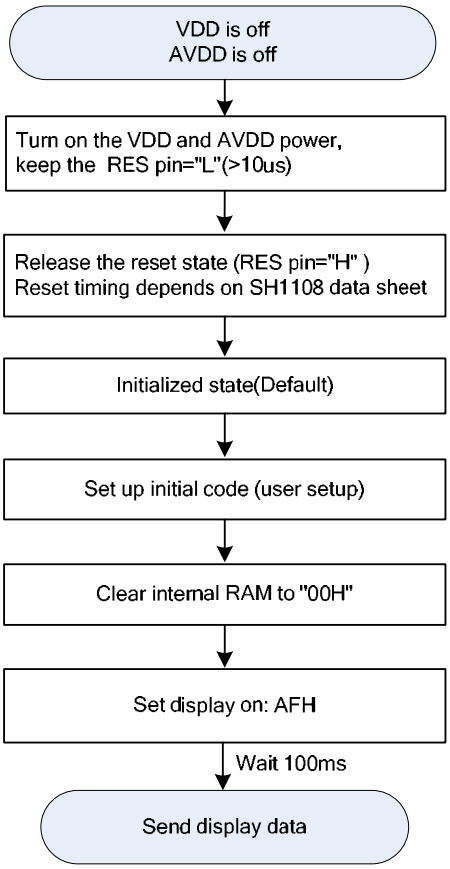
Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
9. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
10. Set Page Address	0	1	0	1	0	1	1	0	0	0	0	Specifies page address to load display RAM data to page address register. (POR = 00H)
				*	*	*	Page address					
11. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N – 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
12. Set Display Resolution	0	1	0	1	0	1	0	1	0	0	1	This command is use to set the display resolution.(POR=03H)
	0	1	0	0	0	0	0	0	0	Display resolution		
13. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
14. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
15. VCOM Deselect Level Mode	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
Set VCOM Deselect Level Data Set	0	1	0	VCOM = (β_1 X V_{REF})								
16. VSEGM Deselect Level Mode	0	1	0	1	1	0	1	1	1	0	0	This command is to set the VSEMG pad output voltage level at deselect stage. (POR = 35H)
Set VSEGM Deselect Level Data Set	0	1	0	VSEGM = (β_1 X V_{REF})								
17. VSL Deselect Level Data Set	0	1	0	0	0	1	1	D3	D2	D1	D0	This command is to set the VSL voltage (POR=30H)
18. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
19. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
20. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
21. Write Display Data	1	1	0	Write RAM data								
22. Read Status	0	0	1	BUSY	ON/ OFF	ID						
23. Read Display Data	1	0	1	Read RAM data								

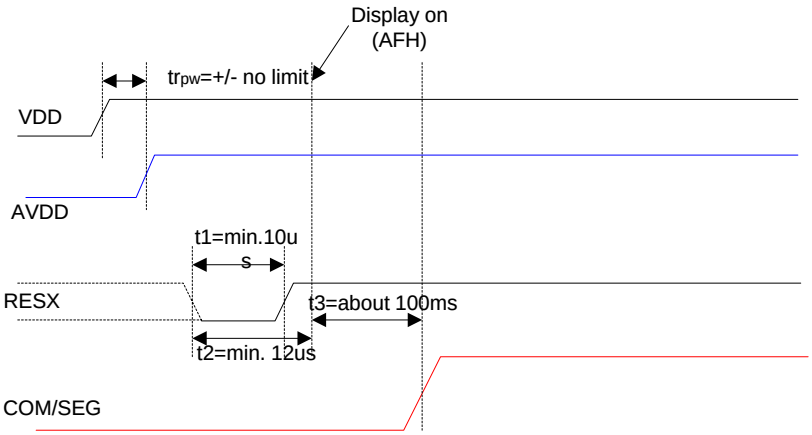
Note: Do not use any other command, or the system malfunction may result.

1. Power On/Off and Initialization

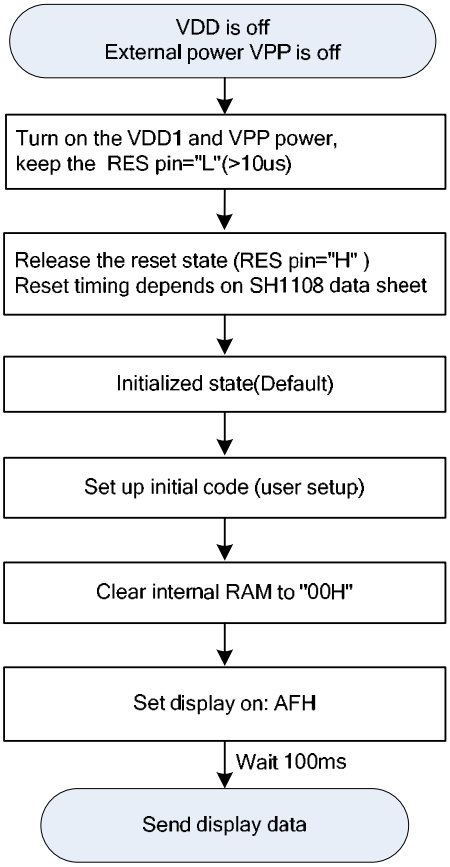
1.1. Built-in DC-DC pump power is being used immediately after turning on the power:



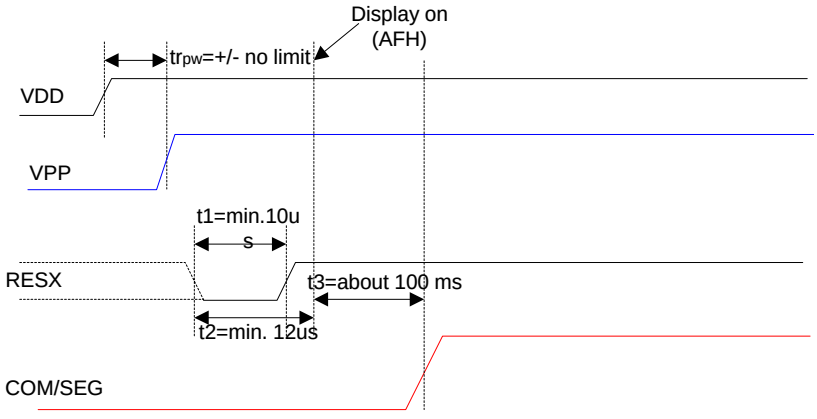
Power on sequence：



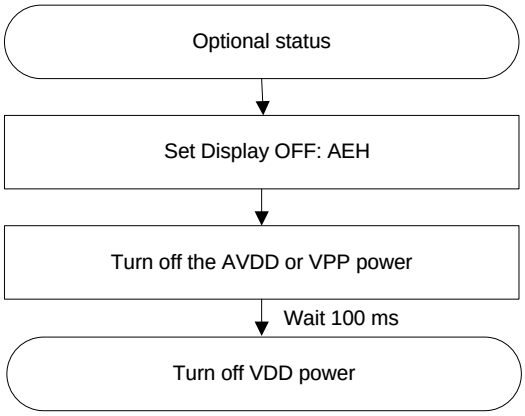
1.2. External power is being used immediately after turning on the power:



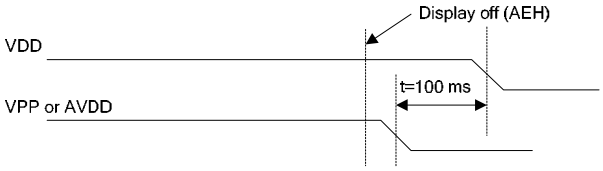
Power on sequence：



1.3 Power Off



Power off sequence：



Note：There will be no damages to the display module if the power sequences are not met.

Absolute Maximum Rating*

DC Supply Voltage (V_{DD}) . . . . . .-0.3V to +3.6V

DC Supply Voltage (V_{PP}) . . . . . -0.3V to +17V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (GND **= 0V, VDD = 1.65 - 3.5V AVDD=2.4-3.5V, TA =+25°C, unless otherwise specified)**

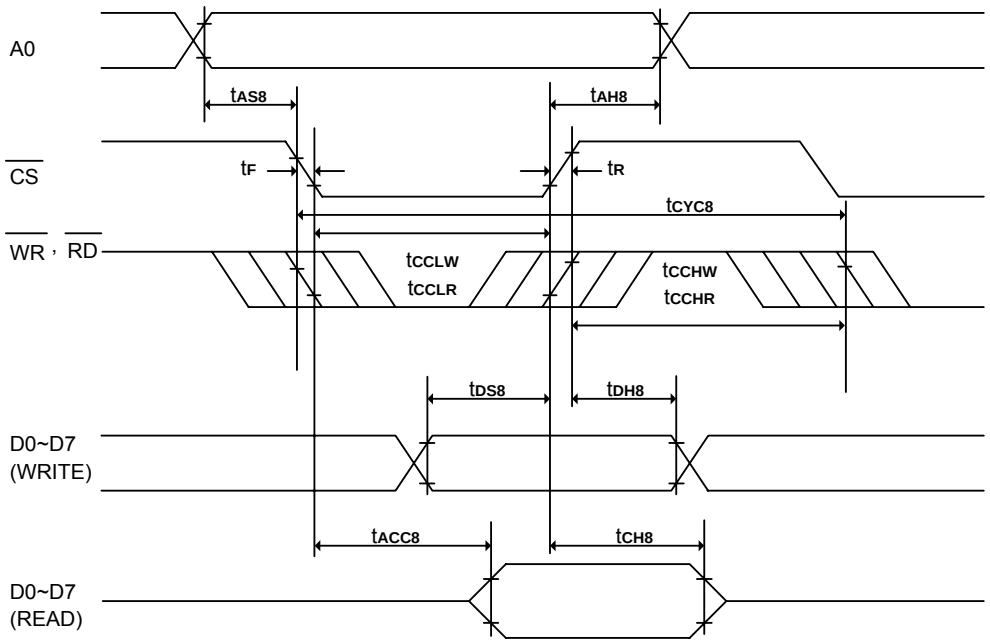
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage	1.65	-	3.5	V	
AV_{DD}	DC-DC voltage	2.4	-	3.5	V	
V_{PP}	OLED Operating voltage	7	15	16.5	V	
V_{BREF}	Internal voltage reference	1.15	1.20	1.25	V	
I_{DD1}	Dynamic current consumption 1(in V_{DD})	-	170	250	μA	V_{DD} = 3V, AV_{DD}=3V, I_{REF} = -15.625μA, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached.
I_{DD2}	Dynamic current consumption 2 (in AVDD)	-	190	285	μA	V_{DD}=3V, AV_{DD}=3V, I_{REF} = -15.625μA, Contrast α = 256, Bulid-in DC-DC ON, VPP=15V, Display ON, display data = All ON, No panel attached.
I_{PP}	OLED dynamic current consumption	-	1.57	2.0	mA	V_{DD} = 3V, AV_{DD} =3V ,V_{PP} = 15V, IREF = -15.625μA, Contrast α = 256, Display ON, Display data = All ON, No panel attached
I_{SP}	Sleep mode current consumption in V_{DD} & AVDD	-	0.01	5	μA	During sleep, T_A = +25°C, V_{DD} = 3V,AV_{DD}=3V
	Sleep mode current consumption in V_{PP}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{PP} = 15V (External)
I_{SEG}	Segment output current	-	-500	-	μA	V_{DD} = 3V, V_{PP} = 15V, I_{REF} = -15.625μA, R_{LOAD} = 20k , Display ON. Contrast α = 256.
		-	-343.75	-	μA	V_{DD} = 3V, V_{PP} = 15V, I_{REF} = -15.625μA, R_{LOAD} = 20k , Display ON. Contrast α = 176.
		-	-187.5	-	μA	V_{DD} = 3V, V_{PP} = 15V, I_{REF} = -15.625μA, R_{LOAD} = 20k , Display ON. Contrast α = 96.
		-	-31.25	-	μA	V_{DD} = 3V, V_{PP} = 15V, I_{REF} = -15.625μA, R_{LOAD} = 20k , Display ON. Contrast α = 16
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} - I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:131] at contrast α = 256.
ΔI_{SEG2}	Adjacent segment output current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG}[N] - I_{SEG}[N+1])/(I_{SEG}[N] + I_{SEG}[N+1]) X 100% I_{SEG} [0:131] at contrast α = 256.

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD}	-	V_{DD}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0~2 and $\overline{RES}$.
V_{ILC}	Low-level input voltage	GND	-	0.2 X V_{DD}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD}	-	V_{DD}	V	I_{OH} = -0.5mA (D0 - D7, and CL).
V_{OLC}	Low -level output voltage	GND	-	0.2 X V_{DD}	V	I_{OL} = 0.5mA (D0, D2 - D7, and CL)
V_{OLCS}	SDA low -level output voltage	GND	-	0.2 X V_{DD}	V	VDD<2V I_{OL}=2mA (SDA)
				0.4		VDD>2V I_{OL}=3mA (SDA)
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD} or GND (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0~2 and $\overline{RES}$).
I_{Hz}	Hz leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
f_{OSC}	Oscillation frequency		900		kHz	T_A = +25°C.VDD=3V
f_{FRM}	Frame frequency for 160 Commons	-	104	-	Hz	When f_{OSC} = 900kHz, Divide ratio = 1, common width = 54 DCLKs.
R_{ON1}	Common switch resistance	-	15	-	Ω	V_{pp}=15V,V_{com}= GND +0.4V
R_{ON2}	Common switch resistance	-	500	-	Ω	V_{pp}=15V,V_{COM}=0.770XV_{pp}-0.4V

AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



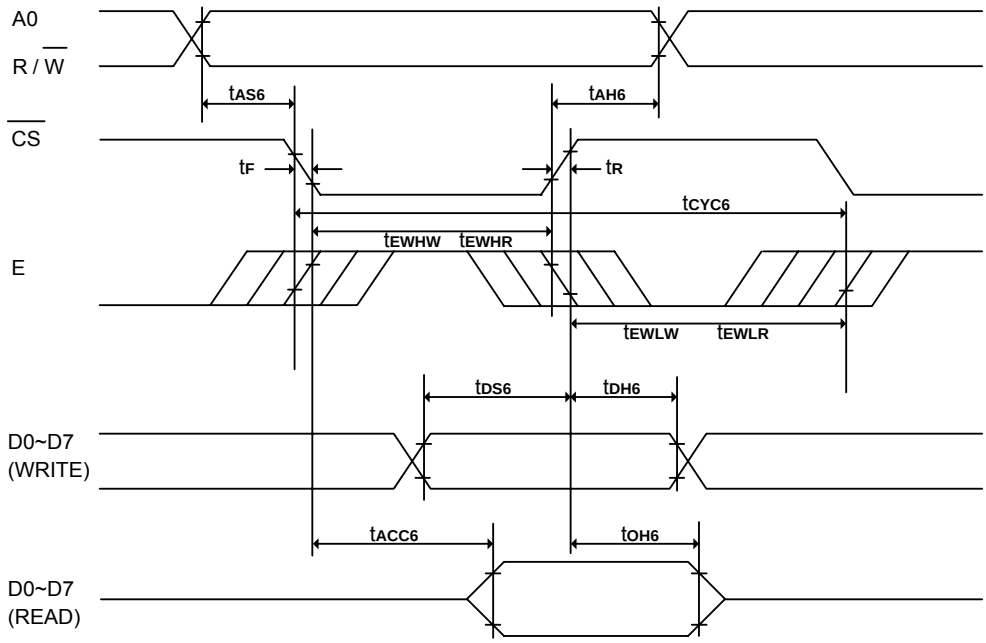
(V_{DD} = 1.65V – 2.4V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	30	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(V_{DD} = 2.4V – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



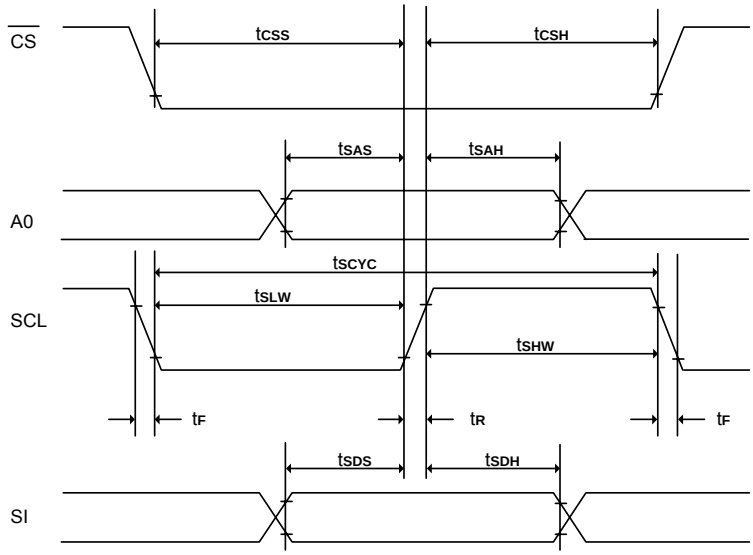
(V_{DD} = 1.65 – 2.4V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(V_{DD} = 2.4 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(3) System buses Write characteristics 3 (For 4 wire SPI)



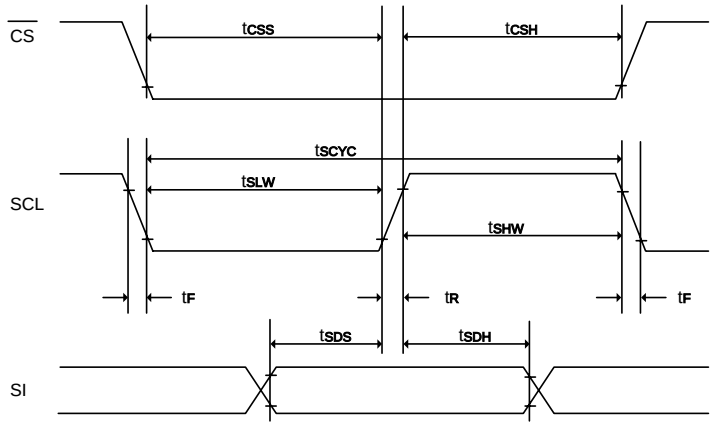
(V_{DD} = 1.65 – 1.8V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SAS}	Address setup time	150	-	-	ns	
t_{SAH}	Address hold time	150	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(V_{DD} = 1.8 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	200	-	-	ns	
t_{SAS}	Address setup time	120	-	-	ns	
t_{SAH}	Address hold time	120	-	-	ns	
t_{SDS}	Data setup time	80	-	-	ns	
t_{SDH}	Data hold time	80	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	96	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	48	-	-	ns	
t_{SHW}	Serial clock H pulse width	80	-	-	ns	
t_{SLW}	Serial clock L pulse width	80	-	-	ns	
t_R	Rise time	-	-	12	ns	
t_F	Fall time	-	-	12	ns	

(4) System buses Write characteristics 4(For 3 wire SPI)



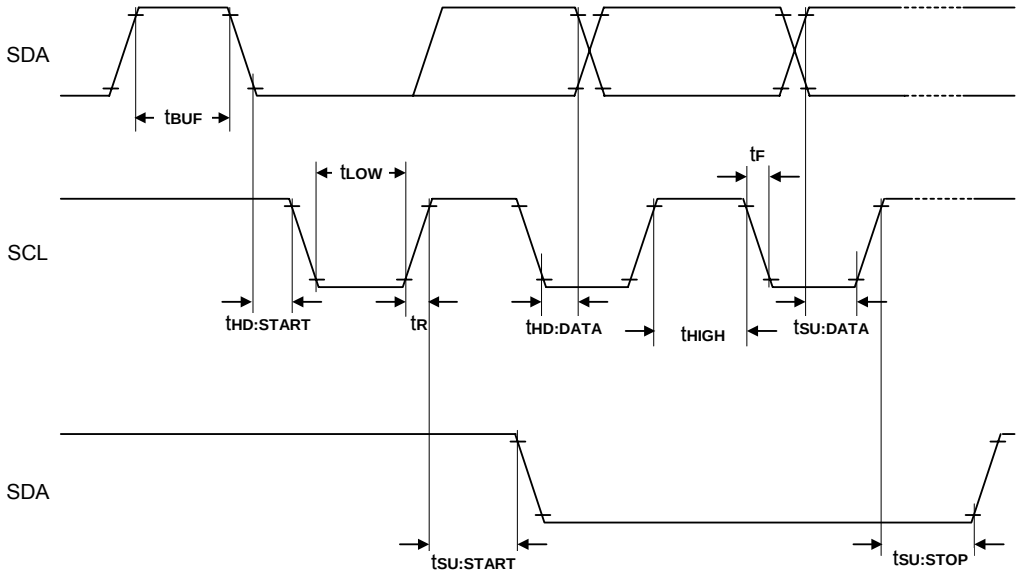
(V_{DD} = 1.65 – 1.8V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(V_{DD} = 1.8 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	200	-	-	ns	
t_{SDS}	Data setup time	80	-	-	ns	
t_{SDH}	Data hold time	80	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	96	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	48	-	-	ns	
t_{SHW}	Serial clock H pulse width	80	-	-	ns	
t_{SLW}	Serial clock L pulse width	80	-	-	ns	
t_R	Rise time	-	-	12	ns	
t_F	Fall time	-	-	12	ns	

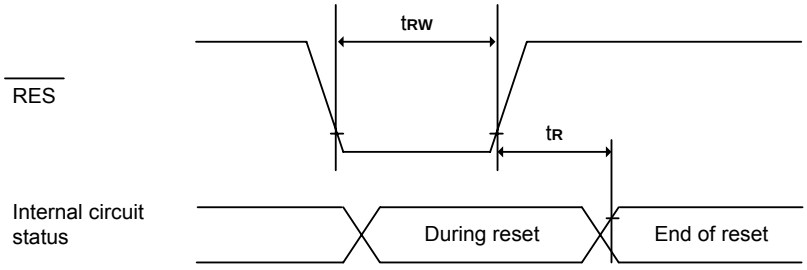
(5) I²C interface characteristics



(V_{DD} = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{SCL}	SCL clock frequency	DC	-	400	kHz	
T_{LOW}	SCL clock Low pulse width	1.3	-	-	s	
T_{HIGH}	SCL clock H pulse width	0.6	-	-	s	
$T_{SU:DATA}$	data setup time	100	-	-	ns	
$T_{HD:DATA}$	data hold time	0	-	0.9	s	
T_R	SCL, SDA rise time	20+0.1Cb	-	300	ns	
T_F	SCL, SDA fall time	20+0.1Cb	-	300	ns	
Cb	Capacity load on each bus line	-	-	400	pF	
$T_{SU:START}$	Setup timefor re-START	0.6	-	-	s	
$T_{HD:START}$	START Hold time	0.6	-	-	s	
$T_{SU:STOP}$	Setup time for STOP	0.6	-	-	s	
T_{BUF}	Bus free times between STOP and START condition	1.3	-	-	s	

1- **Reset Timing**



(V_{DD} = 1.65 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	s	
t_{RW}	Reset low pulse width	10.0	-	-	s	

Application Circuit (for reference only)

Reference Connection to MPU:

1- **8080 series interface: (Internal oscillator, External Vpp)**

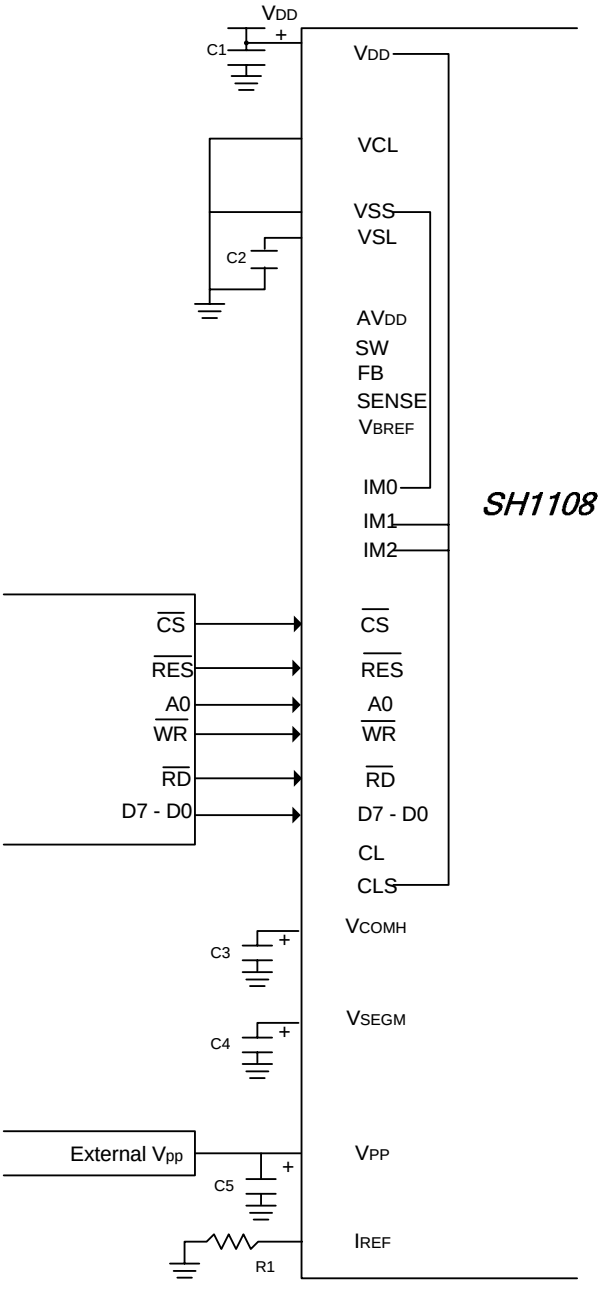


Figure 18-1

Note:

C1 – C5: 4.7μF

R1: about 1M (Refer to the table 8), R1 = (Voltage at IREF – GND)/IREF

1- **6800 Series Interface: (Internal oscillator, Built-in DC-DC)**

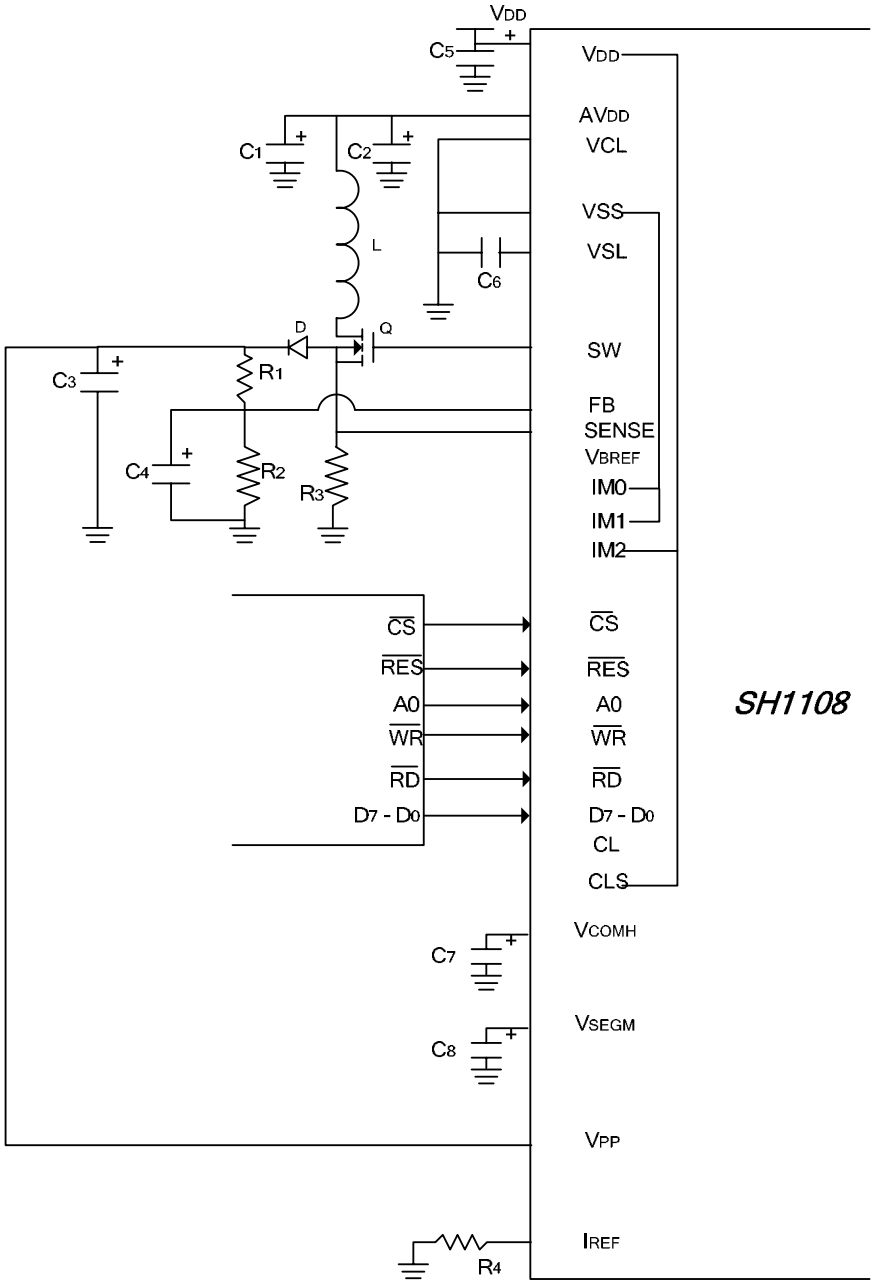


Figure 18-2

Note:
L, D, Q, R1, R2, R3, and C1---C4: Please refer to following description of DC-DC module.
C5-C8: 4.7μF.
R4: about 1M. (Refer to the table 8), R_4 = (Voltage at I_{REF} – GND)/I_{REF}

1- **Serial Interface (3-wire or 4-wire SPI): (External oscillator, External V_{PP}, Max 16.5V)**

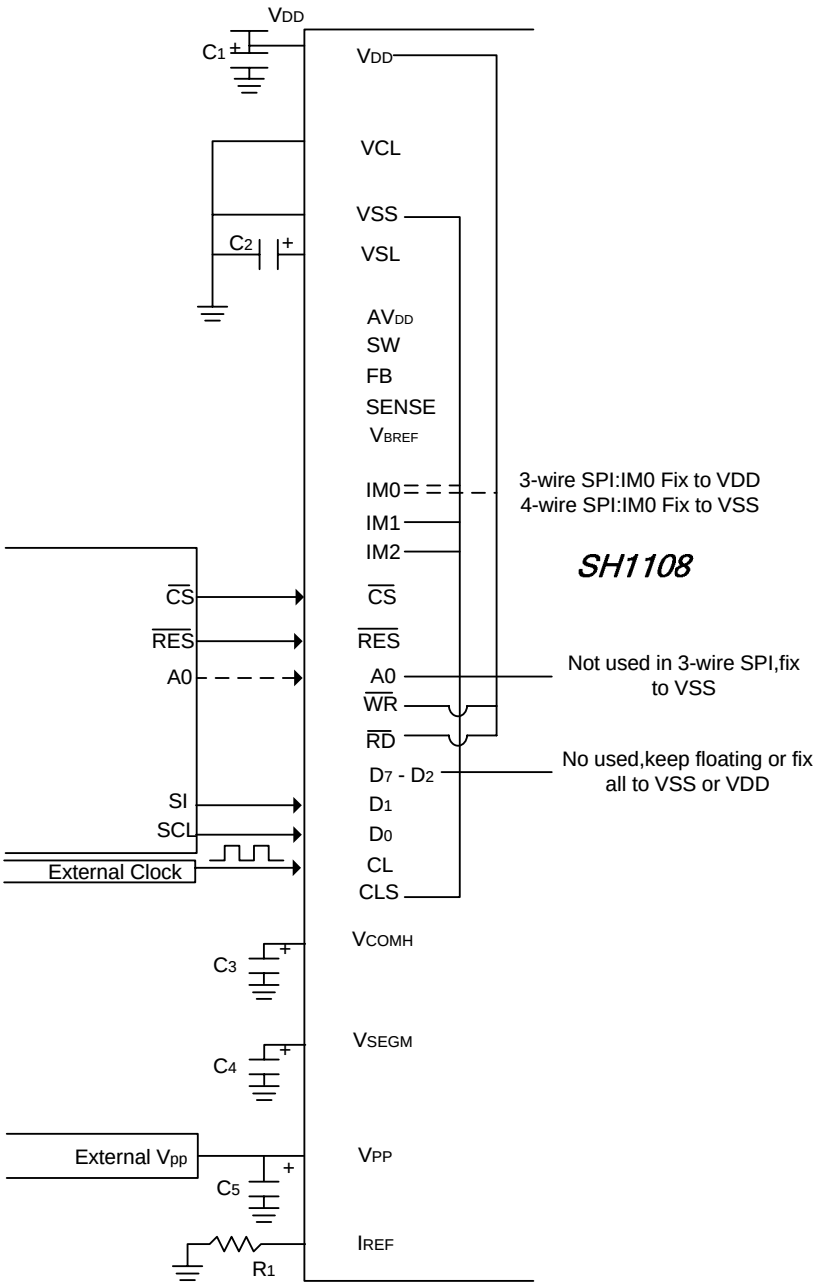


Figure 18-3

Note:
C1---C5: 4.7μF
R1: Recommend 1Ṃ (Refer to the table 8)

1- **I²C Interface (Internal oscillator, External VPP, Max 16.5V)**

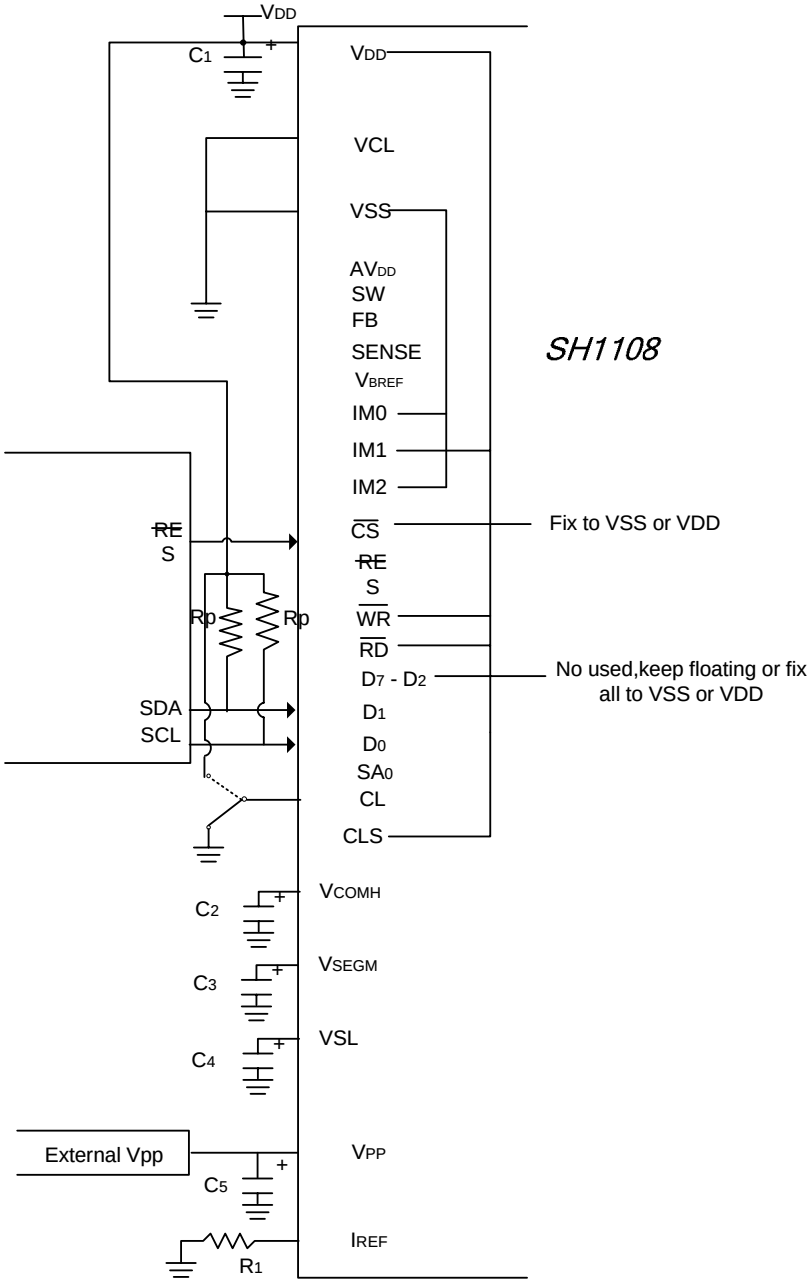


Figure 18-4

Note:
C1---C5:4.7μF
R1: Recommend1Ṃ (Refer to the table 8)
The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1(VDD)
The positive supply of pull-up resistor must equal to the value of VDD
Recommend the value of resistor Rp equal to 1.5KΩ .

DC-DC

Below application circuit is an example for the input voltage of 3V AVDD to generate Vpp of about 15V@10mA-25mA application

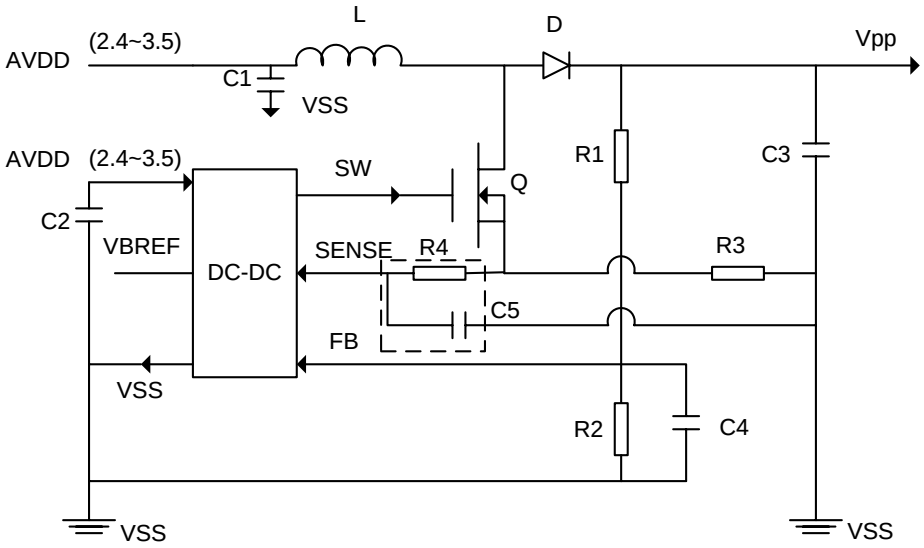


Figure 19

Symbol	Value	Recommendation
L	10μH	
D	SCHOTTKY DIODE	20V@0.5A, MBR0520
Q	MOSFET	N-FET with low RDS(ON),MGSF1N02LT1
R1	1.1M	1%,1/8W
R2	100K	1%,1/8W
R3	0.12	1%,1/2W
R4	10K	1%,1/8W
C1	22μF	Ceramic/16V
C2	0.1μF	Ceramic/16V
C3	10μF	Low ESR/16V
C4	56pF	Ceramic/16V
C5	220pF	Ceramic/16V

Note: R4&C5 are optional; they can increase the efficiency of inductance

Ordering Information

Part No.	Package
SH1108G	Gold bump on chip tray

SPEC Revision History

Version	Content	Date
2.0	P54～P55：Modify the Serial clock cycle of SPI interface	May.2014
1.0	Original	Dec.2013