NV3007 Datasheet

A-Si TFT LCD Single Chip Driver

168RGBx428 Resolution and 262K color

Version 1.0

Jun, 2024

1. Introduction

NV3007 is a single-chip driver for 262,144-color, a-Si TFT liquid crystal display with maximum resolution of 168RGBx428 dots. It contains 252-channel source driver, a 24-channel GIP driver which used for dual-gate control, 161,784-byte GRAM for graphic display data, internal precise power supply circuit which supports full color, 8-color display mode and sleep mode.

NV3007 provides 3-/4-line serial peripheral interface (SPI)， quad serial peripheral interface (QSPI). The display area can be specified in internal GRAM by window address function.

NV3007 is suitable for medium or small size portable products which low power characteristics is major concern. And it can make a display system with fewest components.

An ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution option:
  - 168(RGB)(H) x428(V)
- LCD Driver Output:
  - Source outputs: 252 channels
  - GIP outputs: 24 channels for dual-gate control
- Interface:
  - 8-bit/9-bit Serial Peripheral Interface (SPI) and 2 data lane SPI
  - Quad serial peripheral interface
- On chip Build-In Circuits:
  - Timing generator
  - Oscillator
  - Graphic RAM: 161,784-byte
  - DC/DC converter
- Build-In NV Memory for LCD Initia1 Register Setting
  - OTP to store ID1~ID3
  - OTP(One-Time-Programming) memory store initialization register settings
- Low-power consumption architecture used
- Power supplies Range:
  - I/O and digital voltage (IOVCC): 1.8V ~ 3.6V
  - Analog voltage range (VCI): 2.8V ~ 3.6V
- Output Voltage Range:
  - Source/Gamma power supply voltage
    - GVDD ~ GVCL = 6.4V ~ -4.2V
  - Gate driver output voltage
    - VGH - GND = 12.0V ~ 15.5V
    - VGL - GND = -9.0V ~ -12.5V
    - VGH - VGL≦28V
    - VCOM connect to ground

- Display color:
  - Normal mode: Full color, 262K-color (color depth selectable)
  - Idle mode: 8-color
- Driving Algorithm:
  - Dot Inversion
  - Column Inversion
- Power saving mode: Sleep mode
- Operate temperature range: -30℃ to 85℃
- No need for external electronic component
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1. Block Diagram

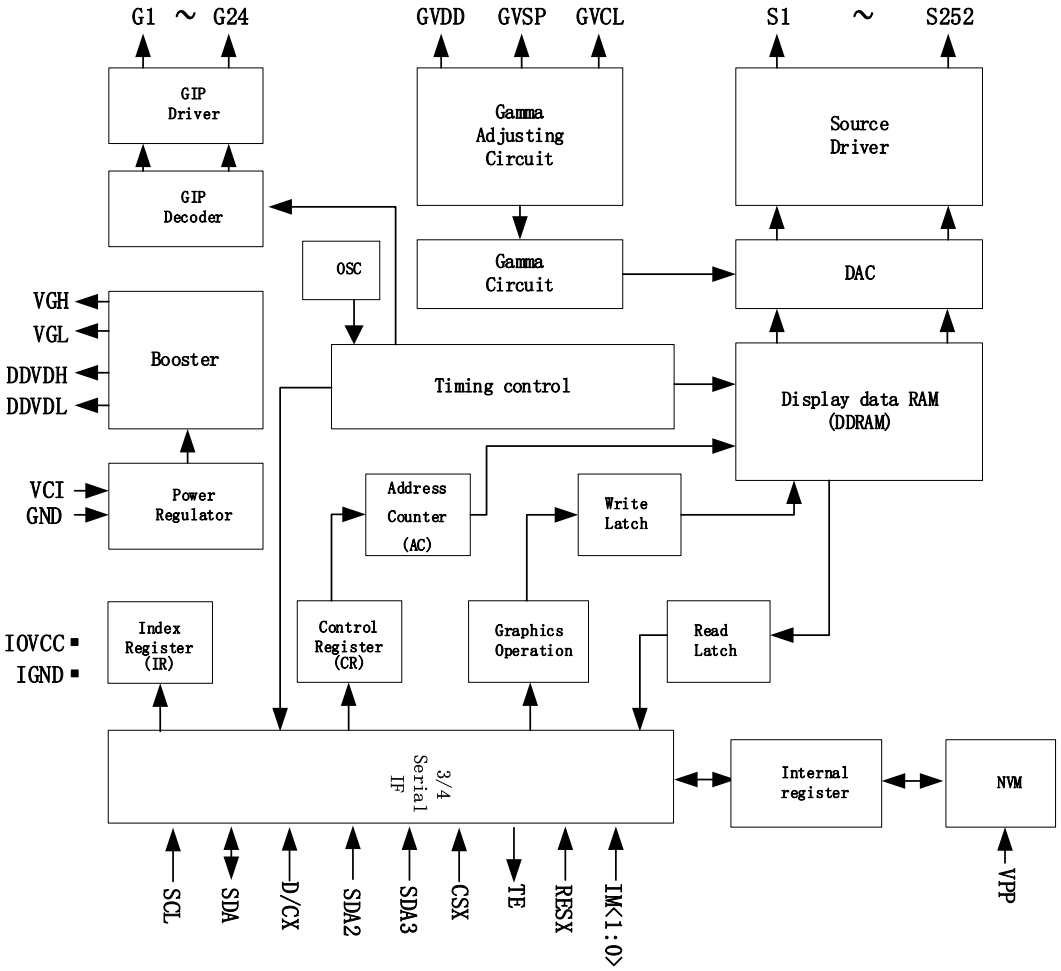


Figure 3-1 Block Diagram

3.2. Pin Description

Power Supply Pins			
Pin Name	**I/O**	**Pin Type (Voltage Level)**	**Descriptions**
IOVCC	I	I/O Power	Power supply for IO circuits(1.8~3.6V)
VCI	I	Analog Power	Power supply for analog circuits(2.8~3.6V)
IGND	I	I/O Ground	Ground for IO system.
GND	I	Analog Ground	Ground for analog system.
VPP	I	NVM Power	Power supply for internal NVM. When writing NVM, it needs external power supply voltage (8.25V). If not used, let this pin open.

Table 3-2-1 Power Supply Pins

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Pin Type (Voltage Level)</th><th>Descriptions</th></tr>
<tr><td>IM<1:0></td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>Select the interface mode
<table>
<tr><th>IM<1.></th><th>IM<0.></th><th>Interface Mode</th><th>Data Pins in use</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td>3-wire 9-bit data serial interface</td><td>SDA: In/Out</td></tr>
<tr><td>2 data line serial interface</td><td>SDA: In/Out,
D/CX:In</td></tr>
<tr><td>1</td><td>1</td><td>4-wire 8-bit data serial interface</td><td>SDA: In/Out</td></tr>
<tr><td rowspan="2">1(or 0)</td><td rowspan="2">0(or 0)</td><td>1-wire quad Serial Peripheral Interface</td><td>SDA: In/Out</td></tr>
<tr><td>4-wire quad Serial Peripheral Interface</td><td>SDA: In
D/CX: In
SDA2: In
SDA3: In</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>Chip select input pin("Low" enable).</td></tr>
<tr><td>D/CX</td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>This pin is used to select "Data or Command" in 4-wire serial interface
When DCX='1', data is selected.
When DCX='0', command is selected.
This pin is used serial interface data in 2 data line / 4-wire quad serial peripheral interface.
If not used, this pin should be connected to IOVCC or IGND.</td></tr>
<tr><td>SCL</td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>This pin is used serial interface clock in serial data interface.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Digital I/O (IOVCC/ IGND)</td><td>Serial in/out signal in 3-wire 9-bit/4-wire 8-bit/2 data line/1-wire quad serial data interface.
Serial input signal in 4-wire quad serial data interface.
The data is applied on the rising edge of the SCL signal.</td></tr>
<tr><td>SDA2</td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>This pin is used serial interface data in 4-wire quad serial peripheral interface.
If not used, this pin should be connected to IOVCC or IGND.</td></tr>
<tr><td>SDA3</td><td>I</td><td>Digital Input (IOVCC/ IGND)</td><td>This pin is used serial interface data in 4-wire quad serial peripheral interface.
If not used, this pin should be connected to IOVCC or IGND.</td></tr>
<tr><td>TE</td><td>O</td><td>Digital Output (IOVCC/ IGND)</td><td>Tearing effect signal is used to synchronize MPU to frame memory writing.
If not used, please let this pin open.</td></tr>
</table>

Table 3-2-2 Interface Logic Signals

LCD Driver Output Pins			
Pin Name	**I/O**	**Pin Type**	**Descriptions**
S252~S1	O	Source	Source output signals. Leave the pin to open when not in use.
G24~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
VCOM	O	Ground	Connect to ground.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).

Table 3-2-3 LCD Driver Output Pins

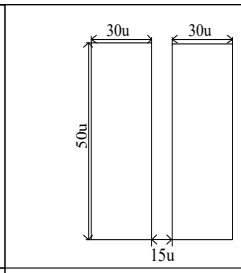
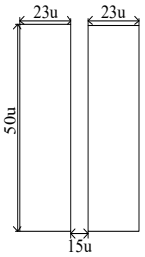
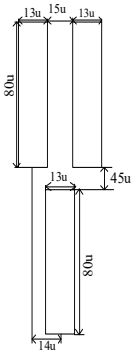
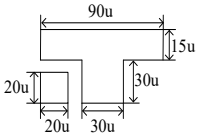
Test and Other Pins			
Pin Name	**I/O**	**Pin Type**	**Descriptions**
DVDD	O	Open	Internal test pins. Leave the pin open.
DDVDH	O	Open	Power pad for analog circuit. Leave the pin open.
DDVDL	O	Open	Power pad for analog circuit. Leave the pin open.
VDDS	O	Open	Power pad for analog circuit. Leave the pin open.
GVDD	O	Open	Internal test pins. Leave the pin open.
GVSP	O	Open	Internal test pins. Leave the pin open.
GVCL	O	Open	Internal test pins. Leave the pin open.
OSC_IN	I	Open	Internal test pins. Leave the pin open.
OSC_SEL	I	Open	Internal test pins. Leave the pin open.
TEST0/TEST1 TEST2/TEST3	O	Open	Internal test pins. Leave the pin open.
IB_T	O	Open	Internal test pins. Leave the pin open.
VREF_T	O	Open	Internal test pins. Leave the pin open.
VBG_T	O	Open	Internal test pins. Leave the pin open.
DUM	-	Open	These pins are dummy. Leave the pin open.

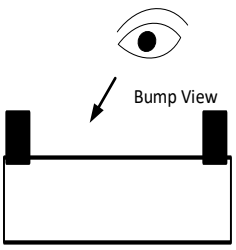
Table 3-2-4 Test and Other Pins

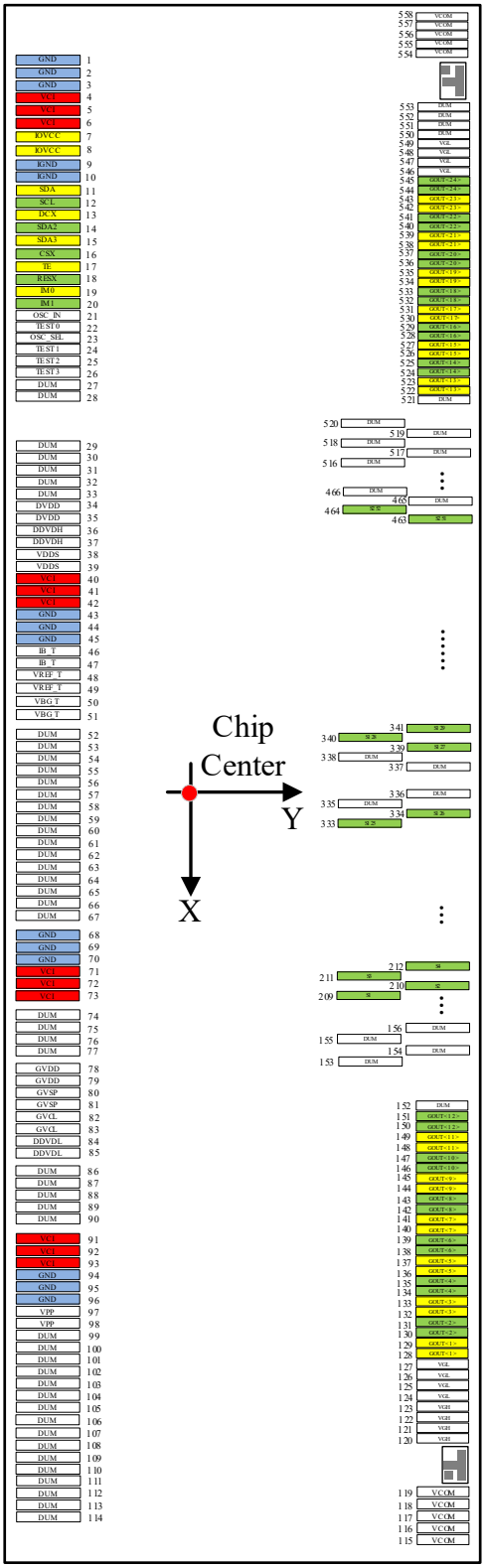
No.	Item		Description
1	Source Driver		252 channels
2	GIP Diver for gate control		24 channels
3	TFT Display's Capacitor Structure		Cst structure only (Cst on Common)
4	Drive Output	S1~S252	V0~V63 grayscales
		G1~G24	VGH-VGL
5	Input Voltage	IOVCC	1.8 ~ 3.6V
		VCI	2.8 ~ 3.6V
6	Liquid Crystal Drive Voltages	DDVDH	6.2 ~ 6.8V
		DDVDL	-4.0V ~ -5.0V
		VGH	12.0 ~ 15.5V
		VGL	-9.0 ~ -12.5V
		|VGH − VGL|	Max.28.0V
7	Internal Boost circuits	DDVDH	VCI*3
		DDVDL	VCI*-2
		VGH	VCI*7
		VGL	VCI*-6

Table 3-2-5 Liquid crystal power supply specifications

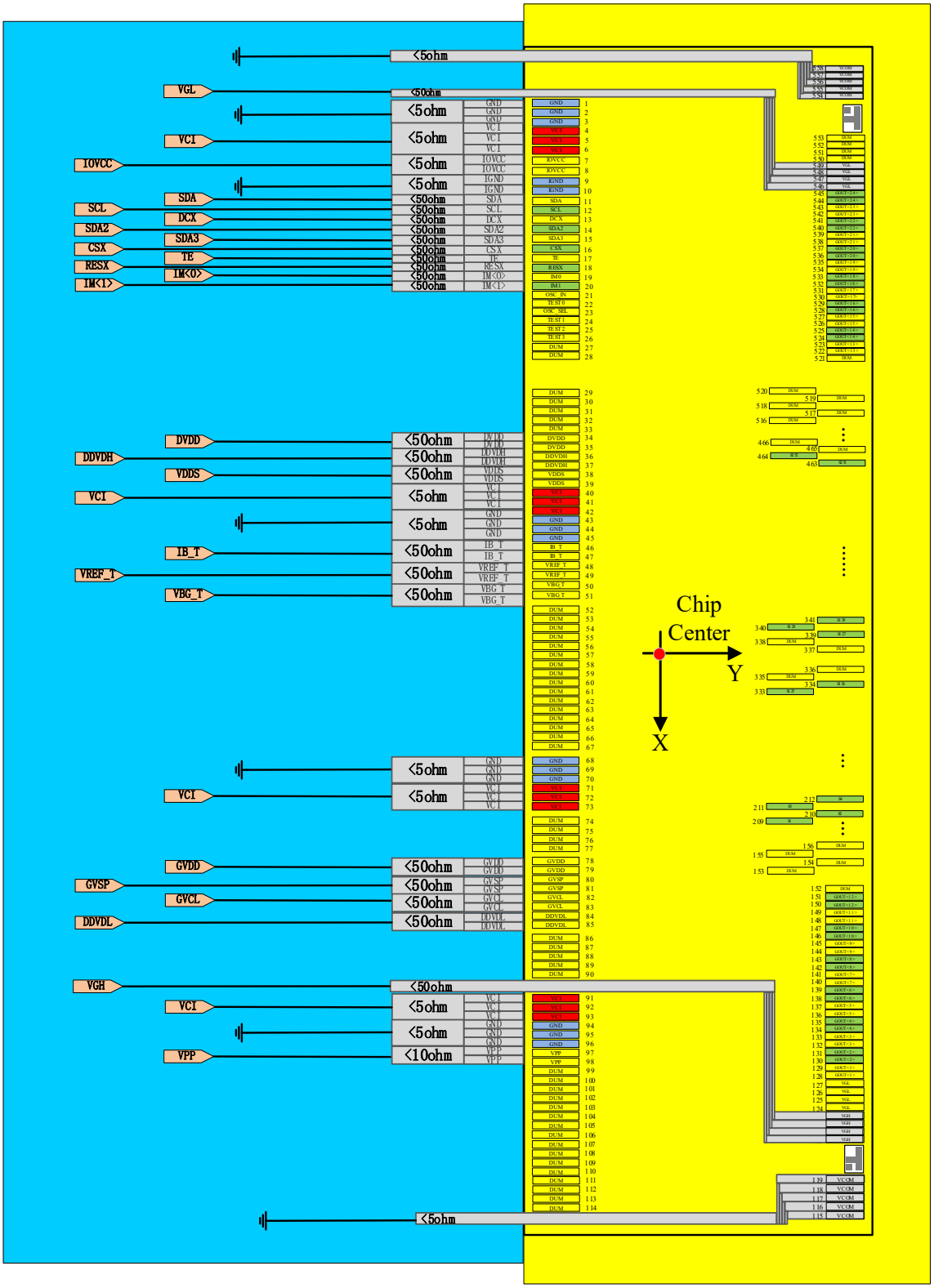
3.3. Bump Arrangement

Chip Size:10720um x 643um(not include scribe line) 10780um x 703um (include scribe line)	
Chip thickness: 250um(±10um)	
Bump height: 9um(±3um)	
Input Pads 1~114	
Gout Related Pads 128~151,522~545	
Source Related Pads 209~334,339~464	
Mark The left size is the Same with the right size	



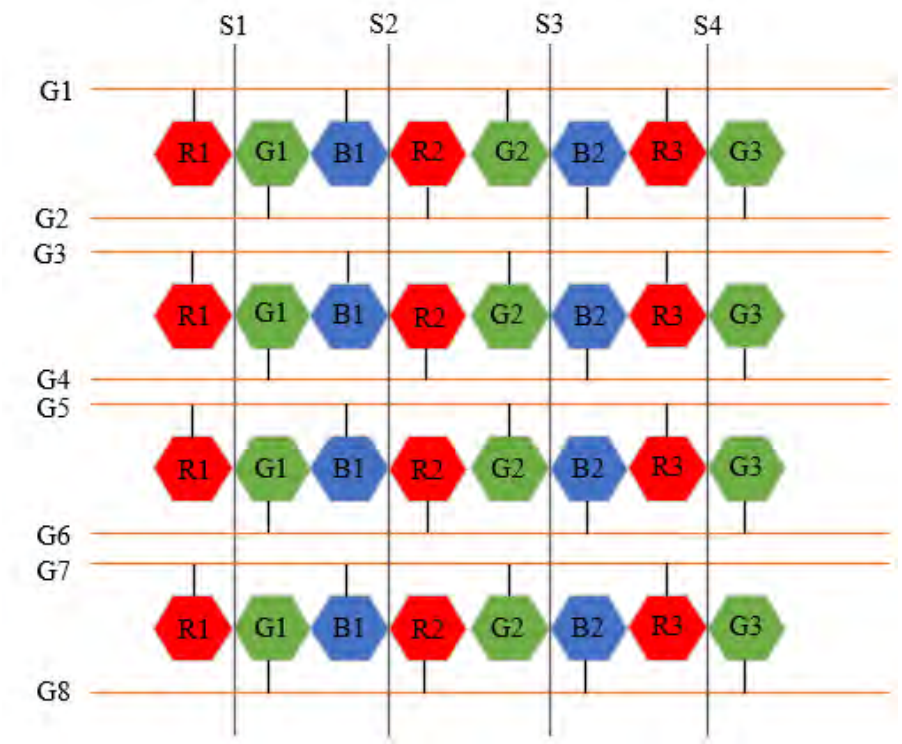


3.4. Pin Connection

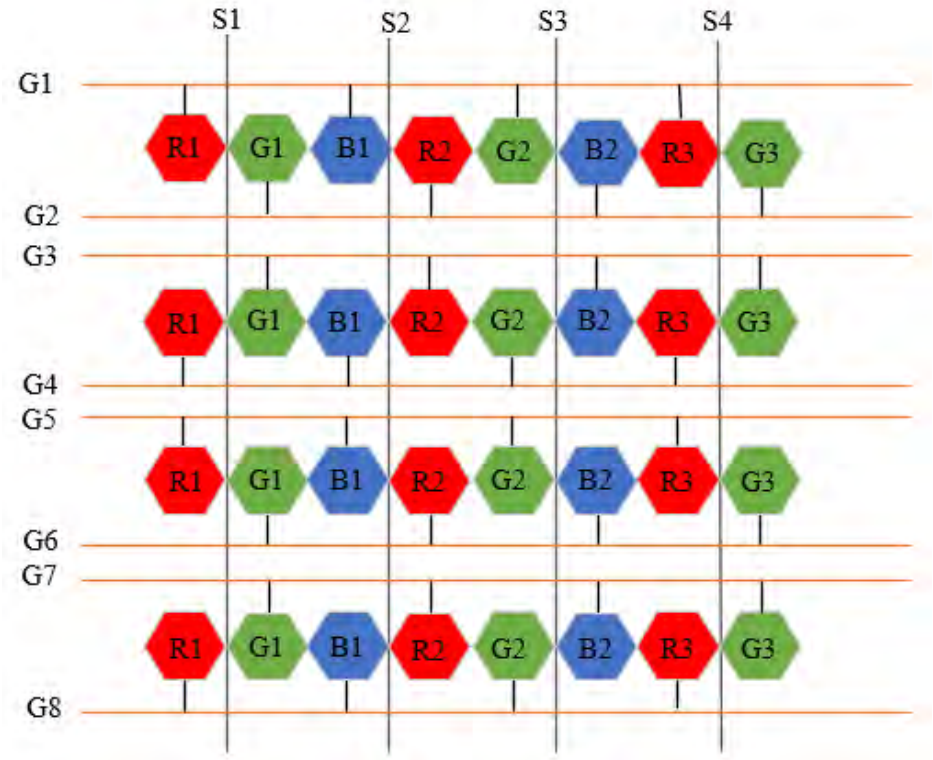


3.5. Supported pixel structure

3.5.1. Z type pixel structure



3.5.2. Bow-shaped type pixel structure



3.6. PAD coordinates

NO	PAD Name	X-axis	Y-axis
1	GND	-5321	-272
2	GND	-5276	-272
3	GND	-5231	-272
4	VCI	-5186	-272
5	VCI	-5141	-272
6	VCI	-5096	-272
7	IOVCC	-5051	-272
8	IOVCC	-5006	-272
9	IGND	-4961	-272
10	IGND	-4916	-272
11	SDA	-4871	-272
12	SCL	-4826	-272
13	DCX	-4781	-272
14	SDA2	-4736	-272
15	SDA3	-4691	-272
16	CSX	-4646	-272
17	TE	-4601	-272
18	RESX	-4556	-272
19	IM<0>	-4511	-272
20	IM<1>	-4466	-272
21	OSC_IN	-4421	-272
22	TEST0	-4376	-272
23	OSC_SEL	-4331	-272
24	TEST1	-4286	-272
25	TEST2	-4241	-272
26	TEST3	-4196	-272
27	DUM	-4151	-272
28	DUM	-4106	-272
29	DUM	-3251	-272
30	DUM	-3071	-272
31	DUM	-2891	-272
32	DUM	-2711	-272
33	DUM	-2531	-272
34	DVDD	-2289	-272
35	DVDD	-2244	-272
36	DDVDH	-2199	-272
37	DDVDH	-2154	-272
38	VDDS	-2109	-272
39	VDDS	-2064	-272
40	VCI	-2019	-272
41	VCI	-1974	-272
42	VCI	-1929	-272
43	GND	-1884	-272
44	GND	-1839	-272
45	GND	-1794	-272
46	IB_T	-1749	-272
47	IB_T	-1704	-272
48	VREF_T	-1659	-272
49	VREF_T	-1614	-272
50	VBG_T	-1569	-272
51	VBG_T	-1524	-272
52	DUM	-1299	-272
53	DUM	-1119	-272
54	DUM	-939	-272
55	DUM	-759	-272
56	DUM	-579	-272
57	DUM	-399	-272
58	DUM	-219	-272
59	DUM	-39	-272
60	DUM	141	-272
61	DUM	321	-272
62	DUM	501	-272
63	DUM	681	-272
64	DUM	861	-272
65	DUM	1041	-272
66	DUM	1221	-272
67	DUM	1401	-272
68	GND	1564	-272
69	GND	1609	-272
70	GND	1654	-272
71	VCI	1699	-272
72	VCI	1744	-272
73	VCI	1789	-272
74	DUM	1969	-272
75	DUM	2149	-272
76	DUM	2329	-272
77	DUM	2509	-272
78	GVDD	2627	-272
79	GVDD	2672	-272
80	GVSP	2717	-272
81	GVSP	2762	-272
82	GVCL	2807	-272
83	GVCL	2852	-272
84	DDVDL	2897	-272
85	DDVDL	2942	-272
86	DUM	3122	-272
87	DUM	3302	-272
88	DUM	3482	-272
89	DUM	3662	-272
90	DUM	3842	-272
91	VCI	4051	-272
92	VCI	4096	-272
93	VCI	4141	-272
94	GND	4186	-272
95	GND	4231	-272
96	GND	4276	-272
97	VPP	4321	-272
98	VPP	4366	-272
99	DUM	4411	-272
100	DUM	4456	-272
101	DUM	4501	-272
102	DUM	4546	-272
103	DUM	4591	-272
104	DUM	4636	-272
105	DUM	4681	-272
106	DUM	4726	-272
107	DUM	4771	-272
108	DUM	4816	-272
109	DUM	4861	-272
110	DUM	4906	-272
111	DUM	4951	-272
112	DUM	4996	-272
113	DUM	5041	-272
114	DUM	5086	-272
115	VCOM	5282	272
116	VCOM	5244	272
117	VCOM	5206	272
118	VCOM	5168	272
119	VCOM	5130	272
120	VGH	4870	272

NO	PAD Name	X-axis	Y-axis
121	VGH	4832	272
122	VGH	4794	272
123	VGH	4756	272
124	VGL	4718	272
125	VGL	4680	272
126	VGL	4642	272
127	VGL	4604	272
128	GOUT<1>	4566	272
129	GOUT<1>	4528	272
130	GOUT<2>	4490	272
131	GOUT<2>	4452	272
132	GOUT<3>	4414	272
133	GOUT<3>	4376	272
134	GOUT<4>	4338	272
135	GOUT<4>	4300	272
136	GOUT<5>	4262	272
137	GOUT<5>	4224	272
138	GOUT<6>	4186	272
139	GOUT<6>	4148	272
140	GOUT<7>	4110	272
141	GOUT<7>	4072	272
142	GOUT<8>	4034	272
143	GOUT<8>	3996	272
144	GOUT<9>	3958	272
145	GOUT<9>	3920	272
146	GOUT<10>	3882	272
147	GOUT<10>	3844	272
148	GOUT<11>	3806	272
149	GOUT<11>	3768	272
150	GOUT<12>	3730	272
151	GOUT<12>	3692	272
152	DUM	3654	272
153	DUM	3438	132
154	DUM	3424	257
155	DUM	3410	132
156	DUM	3396	257
157	DUM	3382	132
158	DUM	3368	257
159	DUM	3354	132
160	DUM	3340	257
161	DUM	3326	132
162	DUM	3312	257

NO	PAD Name	X-axis	Y-axis
163	DUM	3298	132
164	DUM	3284	257
165	DUM	3270	132
166	DUM	3256	257
167	DUM	3242	132
168	DUM	3228	257
169	DUM	3214	132
170	DUM	3200	257
171	DUM	3186	132
172	DUM	3172	257
173	DUM	3158	132
174	DUM	3144	257
175	DUM	3130	132
176	DUM	3116	257
177	DUM	3102	132
178	DUM	3088	257
179	DUM	3074	132
180	DUM	3060	257
181	DUM	3046	132
182	DUM	3032	257
183	DUM	3018	132
184	DUM	3004	257
185	DUM	2990	132
186	DUM	2976	257
187	DUM	2962	132
188	DUM	2948	257
189	DUM	2934	132
190	DUM	2920	257
191	DUM	2906	132
192	DUM	2892	257
193	DUM	2878	132
194	DUM	2864	257
195	DUM	2850	132
196	DUM	2836	257
197	DUM	2822	132
198	DUM	2808	257
199	DUM	2794	132
200	DUM	2780	257
201	DUM	2766	132
202	DUM	2752	257
203	DUM	2738	132
204	DUM	2724	257

NO	PAD Name	X-axis	Y-axis
205	DUM	2710	132
206	DUM	2696	257
207	DUM	2682	132
208	DUM	2668	257
209	S<1>	2654	132
210	S<2>	2640	257
211	S<3>	2626	132
212	S<4>	2612	257
213	S<5>	2598	132
214	S<6>	2584	257
215	S<7>	2570	132
216	S<8>	2556	257
217	S<9>	2542	132
218	S<10>	2528	257
219	S<11>	2514	132
220	S<12>	2500	257
221	S<13>	2486	132
222	S<14>	2472	257
223	S<15>	2458	132
224	S<16>	2444	257
225	S<17>	2430	132
226	S<18>	2416	257
227	S<19>	2402	132
228	S<20>	2388	257
229	S<21>	2374	132
230	S<22>	2360	257
231	S<23>	2346	132
232	S<24>	2332	257
233	S<25>	2318	132
234	S<26>	2304	257
235	S<27>	2290	132
236	S<28>	2276	257
237	S<29>	2262	132
238	S<30>	2248	257
239	S<31>	2234	132
240	S<32>	2220	257
241	S<33>	2206	132
242	S<34>	2192	257
243	S<35>	2178	132
244	S<36>	2164	257
245	S<37>	2150	132
246	S<38>	2136	257

NO	PAD Name	X-axis	Y-axis
247	S<39>	2122	132
248	S<40>	2108	257
249	S<41>	2094	132
250	S<42>	2080	257
251	S<43>	2066	132
252	S<44>	2052	257
253	S<45>	2038	132
254	S<46>	2024	257
255	S<47>	2010	132
256	S<48>	1996	257
257	S<49>	1982	132
258	S<50>	1968	257
259	S<51>	1954	132
260	S<52>	1940	257
261	S<53>	1926	132
262	S<54>	1912	257
263	S<55>	1898	132
264	S<56>	1884	257
265	S<57>	1870	132
266	S<58>	1856	257
267	S<59>	1842	132
268	S<60>	1828	257
269	S<61>	1814	132
270	S<62>	1800	257
271	S<63>	1786	132
272	S<64>	1772	257
273	S<65>	1758	132
274	S<66>	1744	257
275	S<67>	1730	132
276	S<68>	1716	257
277	S<69>	1702	132
278	S<70>	1688	257
279	S<71>	1674	132
280	S<72>	1660	257
281	S<73>	1646	132
282	S<74>	1632	257
283	S<75>	1618	132
284	S<76>	1604	257
285	S<77>	1590	132
286	S<78>	1576	257
287	S<79>	1562	132
288	S<80>	1548	257

NO	PAD Name	X-axis	Y-axis
289	S<81>	1534	132
290	S<82>	1520	257
291	S<83>	1506	132
292	S<84>	1492	257
293	S<85>	1478	132
294	S<86>	1464	257
295	S<87>	1450	132
296	S<88>	1436	257
297	S<89>	1422	132
298	S<90>	1408	257
299	S<91>	1394	132
300	S<92>	1380	257
301	S<93>	1366	132
302	S<94>	1352	257
303	S<95>	1338	132
304	S<96>	1324	257
305	S<97>	1310	132
306	S<98>	1296	257
307	S<99>	1282	132
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315	S<107>	1170	132
316	S<108>	1156	257
317	S<109>	1142	132
318	S<110>	1128	257
319	S<111>	1114	132
320	S<112>	1100	257
321	S<113>	1086	132
322	S<114>	1072	257
323	S<115>	1058	132
324	S<116>	1044	257
325	S<117>	1030	132
326	S<118>	1016	257
327	S<119>	1002	132
328	S<120>	988	257
329	S<121>	974	132
330	S<122>	960	257

NO	PAD Name	X-axis	Y-axis
331	S<123>	946	132
332	S<124>	932	257
333	S<125>	918	132
334	S<126>	904	257
335	DUM	890	132
336	DUM	876	257
337	DUM	-876	257
338	DUM	-890	132
339	S<127>	-904	257
340	S<128>	-918	132
341	S<129>	-932	257
342	S<130>	-946	132
343	S<131>	-960	257
344	S<132>	-974	132
345	S<133>	-988	257
346	S<134>	-1002	132
347	S<135>	-1016	257
348	S<136>	-1030	132
349	S<137>	-1044	257
350	S<138>	-1058	132
351	S<139>	-1072	257
352	S<140>	-1086	132
353	S<141>	-1100	257
354	S<142>	-1114	132
355	S<143>	-1128	257
356	S<144>	-1142	132
357	S<145>	-1156	257
358	S<146>	-1170	132
359	S<147>	-1184	257
360	S<148>	-1198	132
361	S<149>	-1212	257
362	S<150>	-1226	132
363	S<151>	-1240	257
364	S<152>	-1254	132
365	S<153>	-1268	257
366	S<154>	-1282	132
367	S<155>	-1296	257
368	S<156>	-1310	132
369	S<157>	-1324	257
370	S<158>	-1338	132
371	S<159>	-1352	257
372	S<160>	-1366	132

NO	PAD Name	X-axis	Y-axis
373	S<161>	-1380	257
374	S<162>	-1394	132
375	S<163>	-1408	257
376	S<164>	-1422	132
377	S<165>	-1436	257
378	S<166>	-1450	132
379	S<167>	-1464	257
380	S<168>	-1478	132
381	S<169>	-1492	257
382	S<170>	-1506	132
383	S<171>	-1520	257
384	S<172>	-1534	132
385	S<173>	-1548	257
386	S<174>	-1562	132
387	S<175>	-1576	257
388	S<176>	-1590	132
389	S<177>	-1604	257
390	S<178>	-1618	132
391	S<179>	-1632	257
392	S<180>	-1646	132
393	S<181>	-1660	257
394	S<182>	-1674	132
395	S<183>	-1688	257
396	S<184>	-1702	132
397	S<185>	-1716	257
398	S<186>	-1730	132
399	S<187>	-1744	257
400	S<188>	-1758	132
401	S<189>	-1772	257
402	S<190>	-1786	132
403	S<191>	-1800	257
404	S<192>	-1814	132
405	S<193>	-1828	257
406	S<194>	-1842	132
407	S<195>	-1856	257
408	S<196>	-1870	132
409	S<197>	-1884	257
410	S<198>	-1898	132
411	S<199>	-1912	257
412	S<200>	-1926	132
413	S<201>	-1940	257
414	S<202>	-1954	132

NO	PAD Name	X-axis	Y-axis
415	S<203>	-1968	257
416	S<204>	-1982	132
417	S<205>	-1996	257
418	S<206>	-2010	132
419	S<207>	-2024	257
420	S<208>	-2038	132
421	S<209>	-2052	257
422	S<210>	-2066	132
423	S<211>	-2080	257
424	S<212>	-2094	132
425	S<213>	-2108	257
426	S<214>	-2122	132
427	S<215>	-2136	257
428	S<216>	-2150	132
429	S<217>	-2164	257
430	S<218>	-2178	132
431	S<219>	-2192	257
432	S<220>	-2206	132
433	S<221>	-2220	257
434	S<222>	-2234	132
435	S<223>	-2248	257
436	S<224>	-2262	132
437	S<225>	-2276	257
438	S<226>	-2290	132
439	S<227>	-2304	257
440	S<228>	-2318	132
441	S<229>	-2332	257
442	S<230>	-2346	132
443	S<231>	-2360	257
444	S<232>	-2374	132
445	S<233>	-2388	257
446	S<234>	-2402	132
447	S<235>	-2416	257
448	S<236>	-2430	132
449	S<237>	-2444	257
450	S<238>	-2458	132
451	S<239>	-2472	257
452	S<240>	-2486	132
453	S<241>	-2500	257
454	S<242>	-2514	132
455	S<243>	-2528	257
456	S<244>	-2542	132

NO	PAD Name	X-axis	Y-axis
457	S<245>	-2556	257
458	S<246>	-2570	132
459	S<247>	-2584	257
460	S<248>	-2598	132
461	S<249>	-2612	257
462	S<250>	-2626	132
463	S<251>	-2640	257
464	S<252>	-2654	132
465	DUM	-2668	257
466	DUM	-2682	132
467	DUM	-2696	257
468	DUM	-2710	132
469	DUM	-2724	257
470	DUM	-2738	132
471	DUM	-2752	257
472	DUM	-2766	132
473	DUM	-2780	257
474	DUM	-2794	132
475	DUM	-2808	257
476	DUM	-2822	132
477	DUM	-2836	257
478	DUM	-2850	132
479	DUM	-2864	257
480	DUM	-2878	132
481	DUM	-2892	257
482	DUM	-2906	132
483	DUM	-2920	257
484	DUM	-2934	132
485	DUM	-2948	257
486	DUM	-2962	132
487	DUM	-2976	257
488	DUM	-2990	132
489	DUM	-3004	257
490	DUM	-3018	132
491	DUM	-3032	257
492	DUM	-3046	132
493	DUM	-3060	257
494	DUM	-3074	132
495	DUM	-3088	257
496	DUM	-3102	132
497	DUM	-3116	257
498	DUM	-3130	132

NO	PAD Name	X-axis	Y-axis
499	DUM	-3144	257
500	DUM	-3158	132
501	DUM	-3172	257
502	DUM	-3186	132
503	DUM	-3200	257
504	DUM	-3214	132
505	DUM	-3228	257
506	DUM	-3242	132
507	DUM	-3256	257
508	DUM	-3270	132
509	DUM	-3284	257
510	DUM	-3298	132
511	DUM	-3312	257
512	DUM	-3326	132
513	DUM	-3340	257
514	DUM	-3354	132
515	DUM	-3368	257
516	DUM	-3382	132
517	DUM	-3396	257
518	DUM	-3410	132
519	DUM	-3424	257
520	DUM	-3438	132
521	DUM	-3654	272
522	GOUT<13>	-3692	272
523	GOUT<13>	-3730	272
524	GOUT<14>	-3768	272
525	GOUT<14>	-3806	272
526	GOUT<15>	-3844	272
527	GOUT<15>	-3882	272
528	GOUT<16>	-3920	272
529	GOUT<16>	-3958	272
530	GOUT<17>	-3996	272
531	GOUT<17>	-4034	272
532	GOUT<18>	-4072	272
533	GOUT<18>	-4110	272
534	GOUT<19>	-4148	272
535	GOUT<19>	-4186	272
536	GOUT<20>	-4224	272
537	GOUT<20>	-4262	272
538	GOUT<21>	-4300	272
539	GOUT<21>	-4338	272
540	GOUT<22>	-4376	272

NO	PAD Name	X-axis	Y-axis
541	GOUT<22>	-4414	272
542	GOUT<23>	-4452	272
543	GOUT<23>	-4490	272
544	GOUT<24>	-4528	272
545	GOUT<24>	-4566	272
546	VGL	-4604	272
547	VGL	-4642	272
548	VGL	-4680	272
549	VGL	-4718	272
550	DUM	-4756	272
551	DUM	-4794	272
552	DUM	-4832	272
553	DUM	-4870	272
554	VCOM	-5130	272
555	VCOM	-5168	272
556	VCOM	-5206	272
557	VCOM	-5244	272
558	VCOM	-5282	272

Name	X-axis	Y-axis
left mark	-5000	296.5
right mark	5000	296.5

4. Interface setting

4.1. SPI Interface

The selection of interface is done by IM [1:0] bits. Please refer to the Table in the following.

IM1	IM0	Interface Mode	CSX	D/CX	SCL	Function
0	1	3-wire serial interface 2 data line serial	"L"	-	↓	Write/Read command, parameter or display data.
1	1	4-wire serial interface	"L"	"H/L"	↓	Write/Read command, parameter or display data.
1 (or 0)	0 (or 0)	1-wire quad Serial Peripheral Interface 4-wire quad Serial Peripheral Interface	"L"	-	↓	Write/Read command, parameter or display data.

Table 4-1 Interface Type Selection

4.1.1. Standard SPI Interface

NV3007 supplies 3-line/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and NV3007. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (SDA2 and SDA3), which are not used, must be connected to IGND. Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

These shown figures are the example of 3-line/4-line SPI interface.

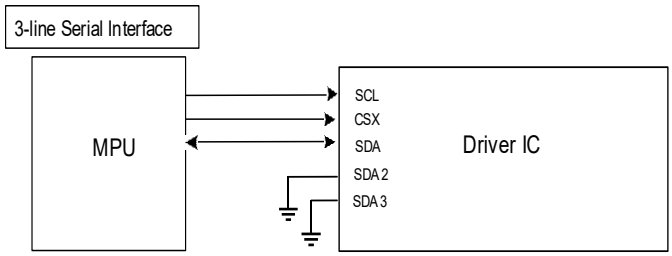


Figure 4-1-1-1 3-line SPI interface

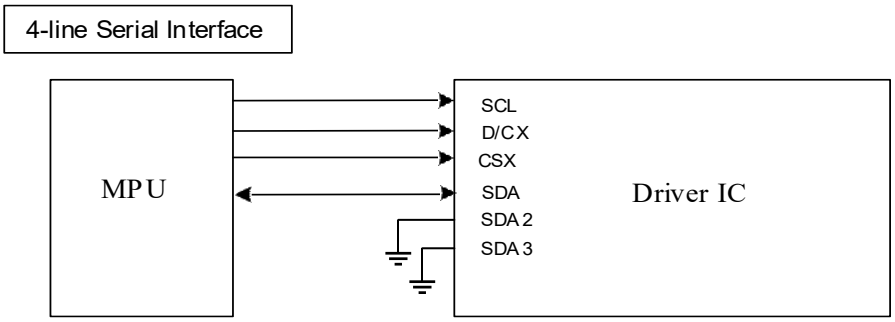


Figure 4-1-1-2 4-line SPI interface

4.1.1.1. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to NV3007. The 3-line serial data packet contains a data/command select bit (D/CX) and a transmission byte. In 4-line serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If the D/CX bit “low”, the transmission byte is interpreted as a command byte. If the D/CX is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to NV3007 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

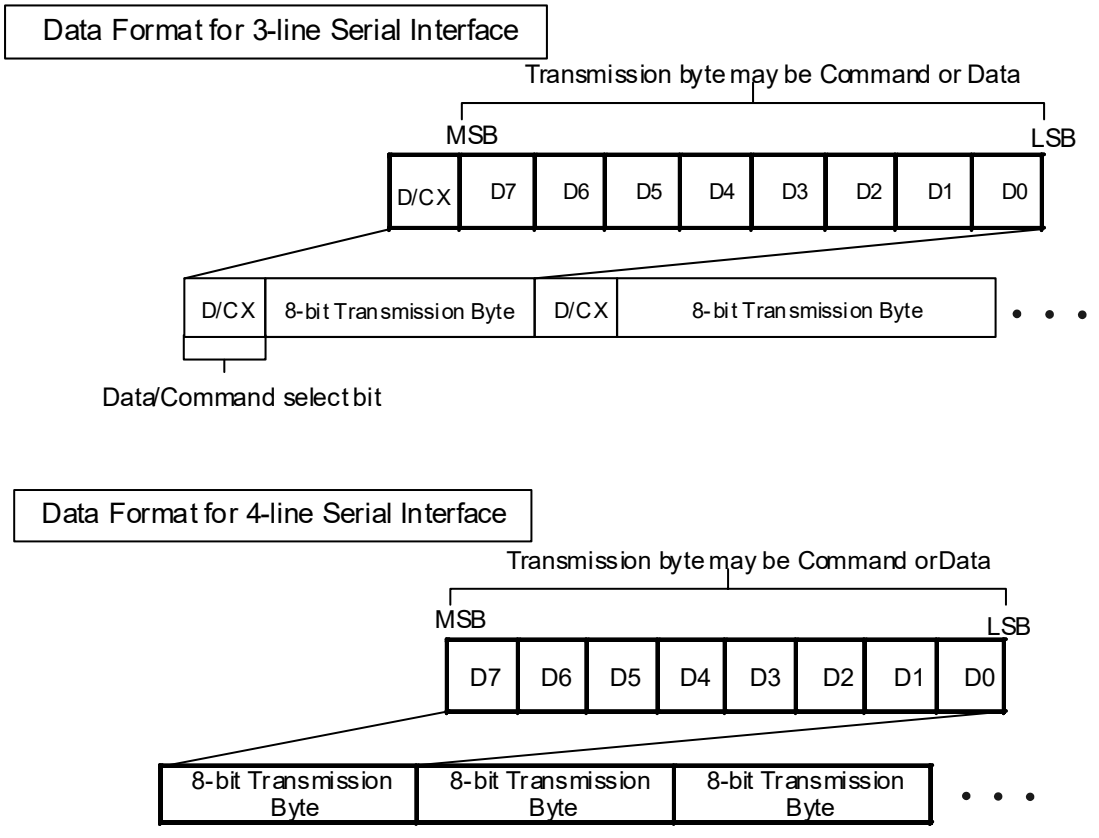


Figure 4-1-1-1-1 Serial interface data stream format

Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by NV3007 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

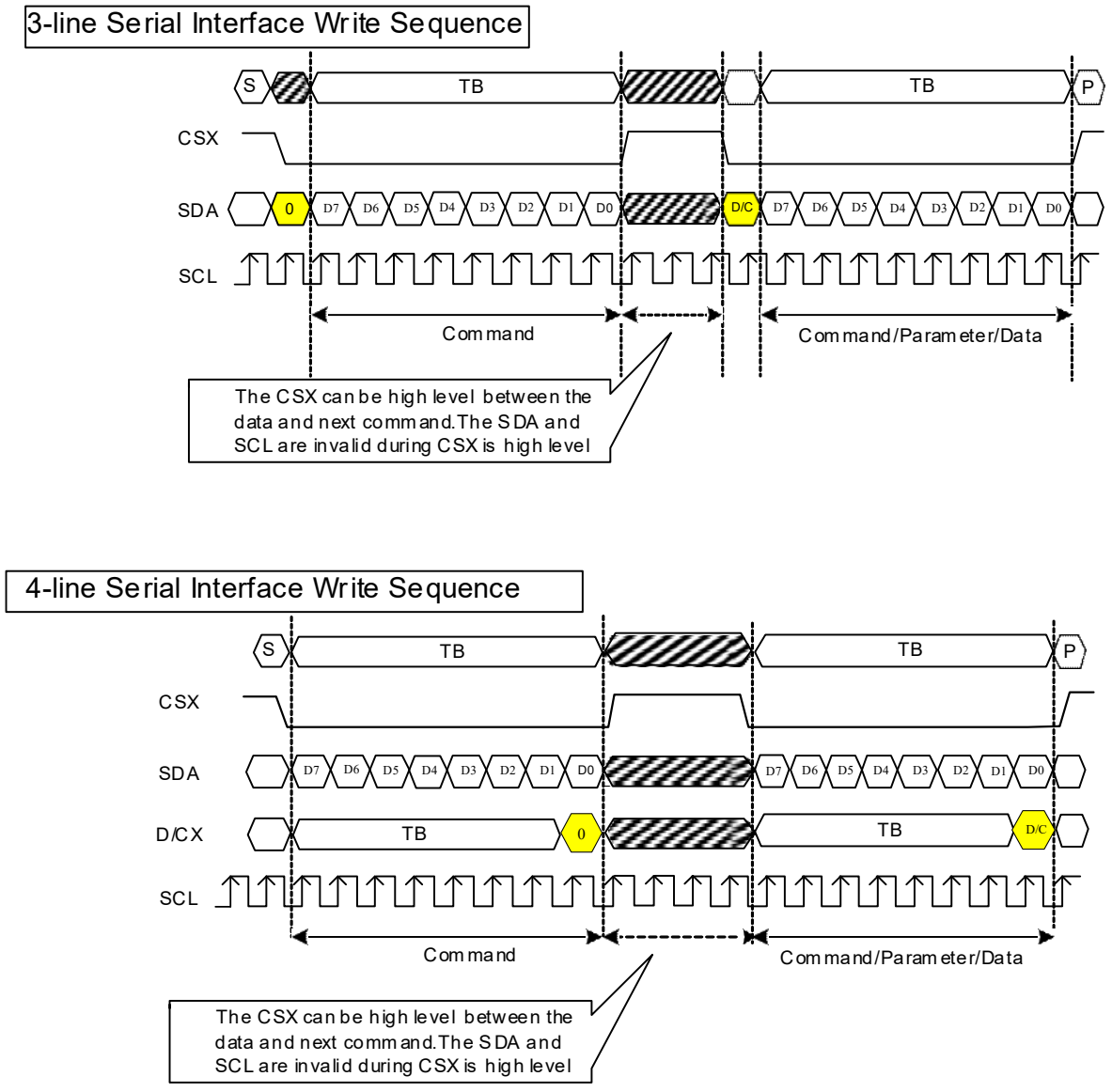
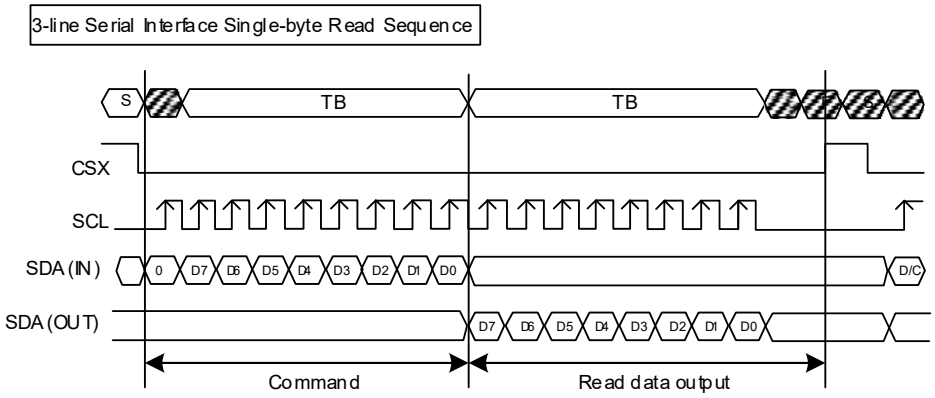
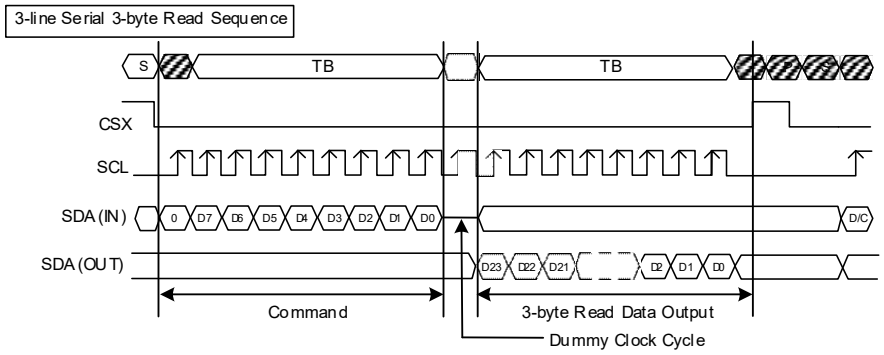


Figure 4-1-1-1-2 Serial interface write sequence

4.1.1.2. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from NV3007. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. NV3007 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has two types of transmitted command data (single/multi-byte) according command code.





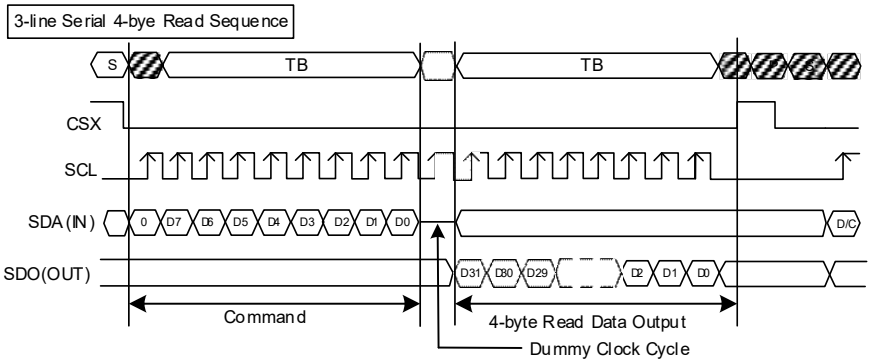
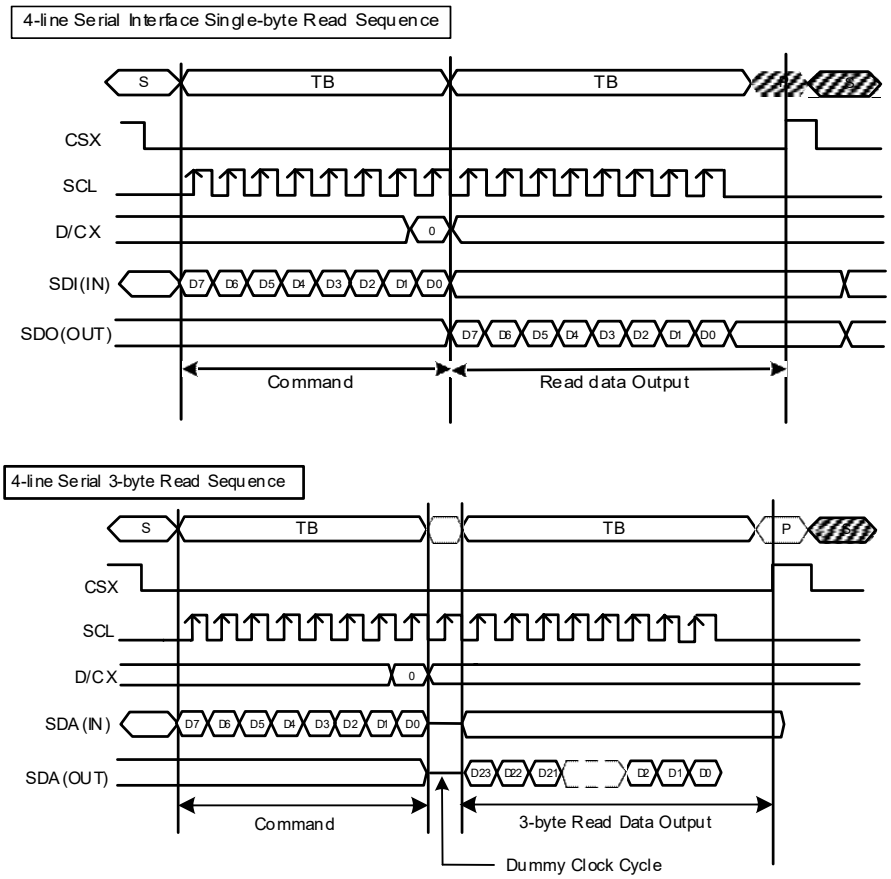


Figure 4-1-1-2-1 3-line serial interface read sequence



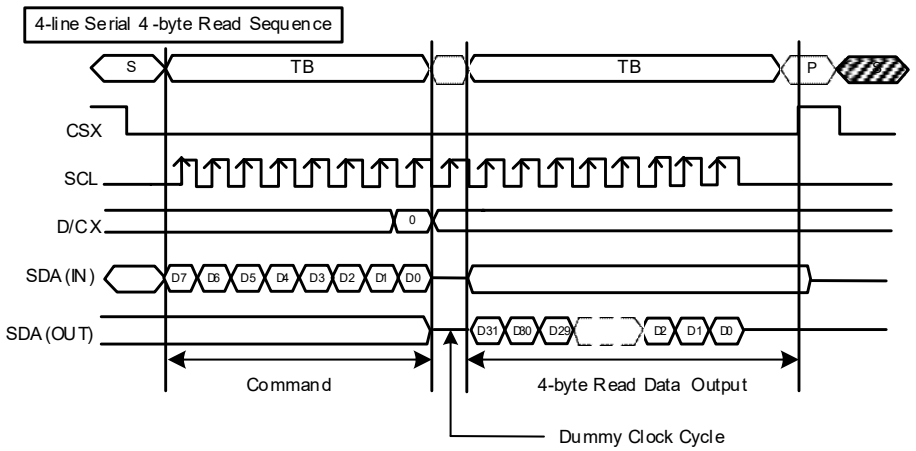


Figure 4-1-1-2-2 4-line serial interface read sequence

4.1.2. Dual SPI Interface

NV3007 supplies Dual-SPI interfaces for communication between host and NV3007. 2 data lane serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input 1/output), and D/CX (serial data input 2).

The shown figure is the example of 2-data line serial interface.

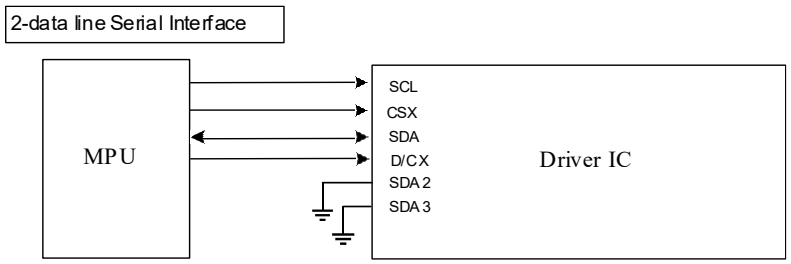


Figure 4-1-2 2-data line serial interface

4.1.2.1. Write Cycle Sequence

Command write mode:

The command write protocol of 2 data lane serial interface is the same with the 3-line serial interface,so users can ignore the input data of D/CX.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

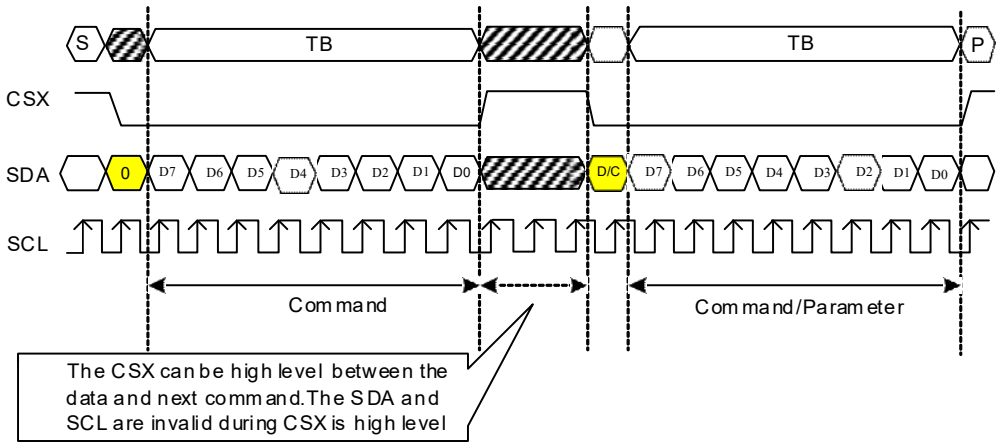


Figure 4-1-2-1 3-line serial interface command write mode protocol

SRAM write mode:

The SRAM write mode of 2 data line serial interface need use SDA pin and D/CX pin to be data input pins.

4.1.2.2. Read Cycle Sequence

The read mode of 2 data lane serial interface is the same with the 3-line serial interface and D/CX pin can be ignored.

4.1.3. Quad SPI Interface

NV3007 supplies 1-line and 4-line bi-directional serial interfaces for communication between host and NV3007. Here 1-line and 4-line represent the number of data lines. The 1-line serial mode consists of chip enabled input (CSX), serial clock input (SCL), and serial data Input/output (SDA), The 4-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL), the serial data Input/output (SDA(SIO0) and serial data Input (D/CX(SI1) & SDA2(SI2) & SDA3(SI3)) for data transmission. Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary.

Each transmission has three part: op-code (first byte after CSX falling edge), Address and Data. op-code used to distinguish different operations between MPU and NV3007 as below table shown.

OP code	Operation	Description
02H	Write Command	In general, this operation used to write registers. When the address is “2C” or “3C”, the following data is identified as RAM data.
03H	Read Command	Read register content from NV3007
32H	Write RAM data	The address must be “2C” or “3C” and the timing takes 24 cycles, see the section 4.2.5 for details
12H	Write RAM data	The address must be “2C” or “3C” and the timing takes 6 cycles, see the section 4.2.5 for details

Note: Each transmission must end with CSX rising edge.

These shown figures are the example of 1-line/4-line Quad SPI interface.

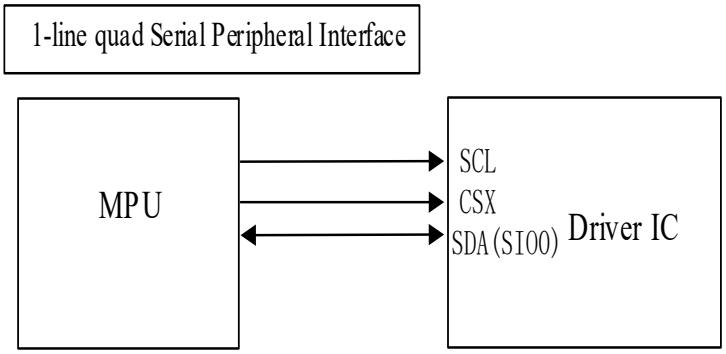


Figure 4-1-3-1 1-line Quad SPI interface

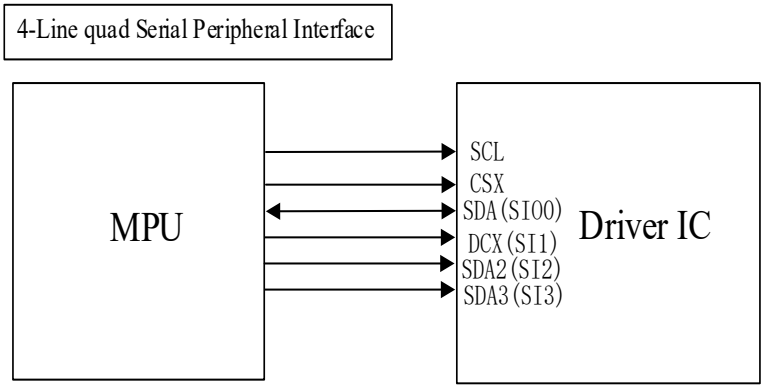


Figure 4-1-3-2 4-line Quad SPI interface

4.1.3.1. Write Cycle Sequence

The write mode of the interface means that the host writes commands or data to NV3007. 1-line serial interface commands and data are written in the same way. The first is that the host processor drives CSX pin to low and Then set the first byte to 02H. Each bit of data is read by NV3007 on the rising edge of the SCL signal, and the data bit of data on the falling edge is set by the host on SDA.

The 1-wire serial interface writes sequence described in the figure as below.

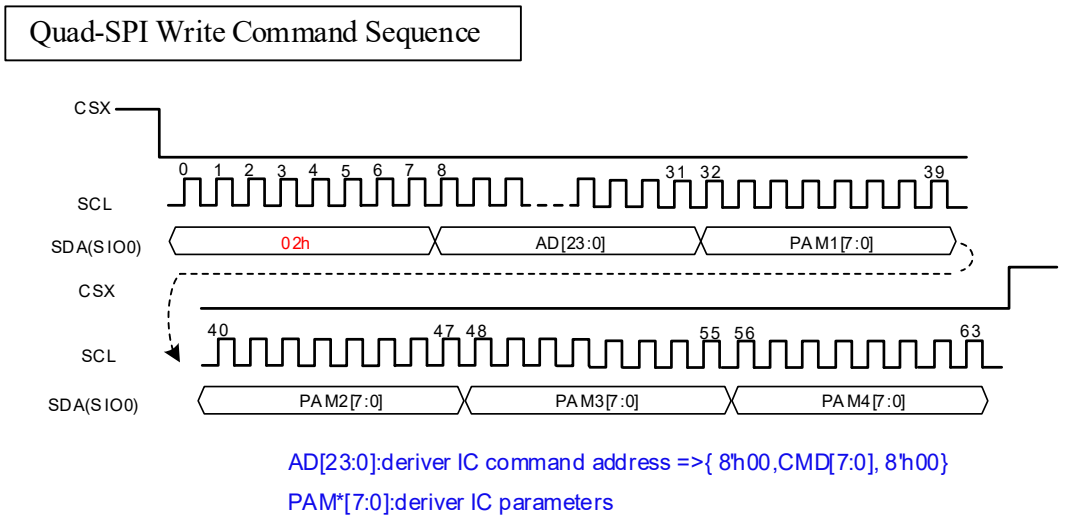


Figure 4-1-3-1-1 Quad SPI write command sequence

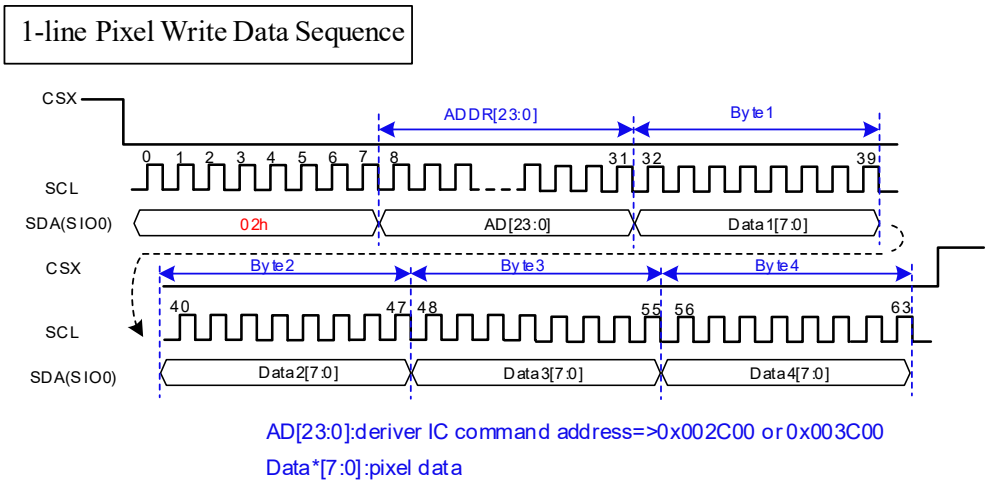


Figure 4-1-3-1-2 1-line Quad SPI write data sequence

4-line serial interface commands and data are written in the same way. The first is that the host processor drives CSX pin to low and then set the first byte to 12H or 32H. Each bit of data is read by NV3007 on the rising edge of the SCL signal, and the data bit of data on the falling edge is set by the host on SDA. The 4-line serial interface writes sequence described in the figure as below.

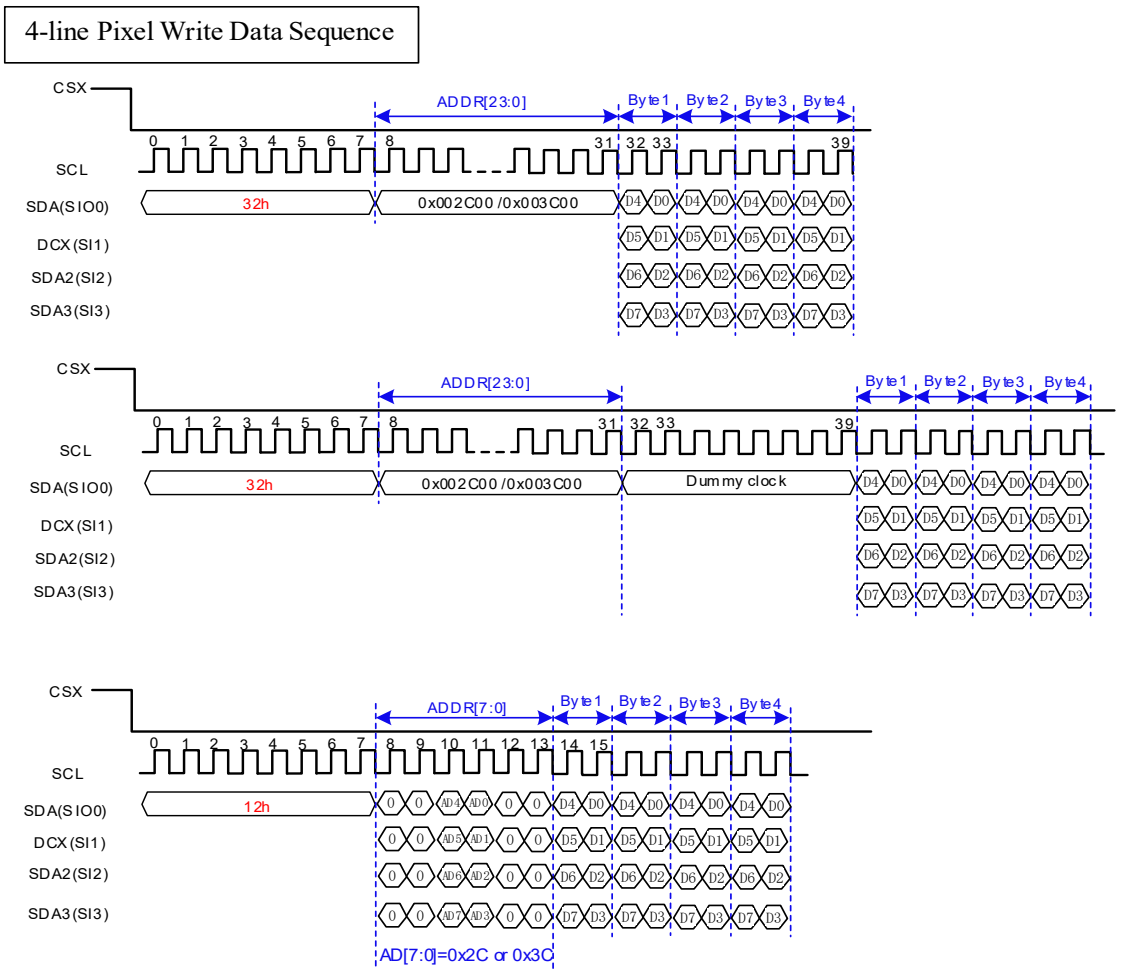


Figure 4-1-3-1-3 4-line Quad SPI write data sequence

4.1.3.2. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from NV3007. For a QSPI read, the host first sends a command that includes a header (03h), address bits, and data bits, and then transmits the following bytes in the opposite direction. The format of the specific sending command is as follows.

QSPI reads support only one wire of read. The specific reading method is that NV3007 stores SDA(input data) lock on the rising edge of SCL(serial clock), and then shifts SDA(output data) to the falling edge of SCL(serial clock).After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit.

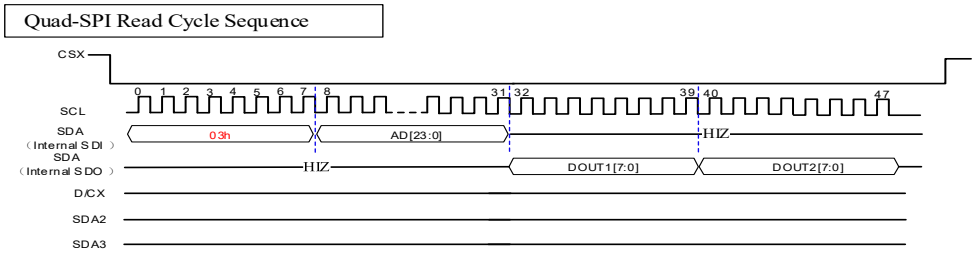


Figure 4-1-3-2 Quad SPI read cycle sequence

4.1.4. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data or frame memory data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

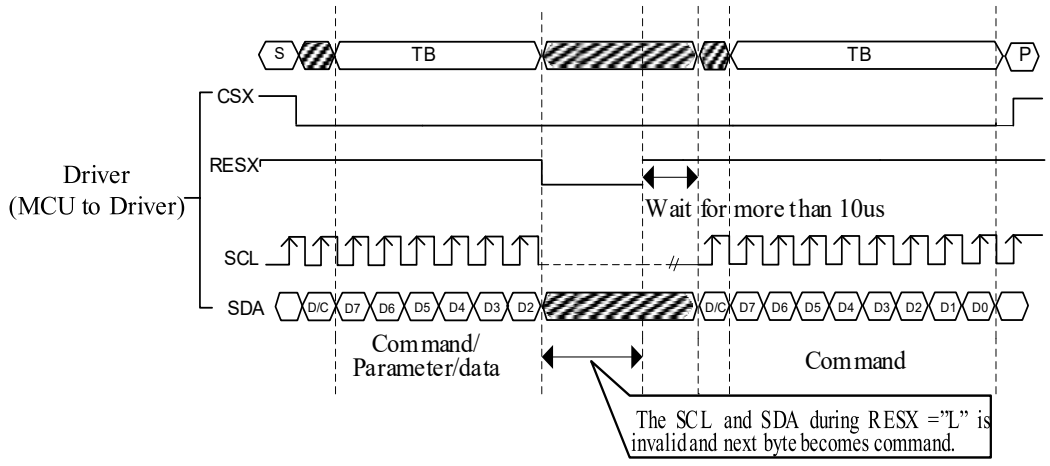


Figure 4-1-4-1 Data Transfer Break and Recovery

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

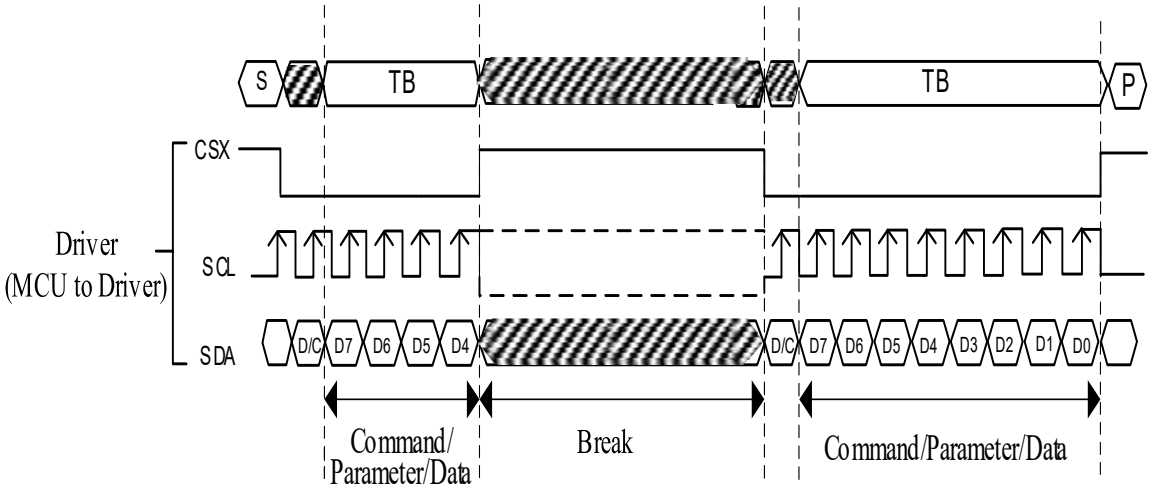


Figure 4-1-4-2 Data Transfer Break and Recovery

If one, two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

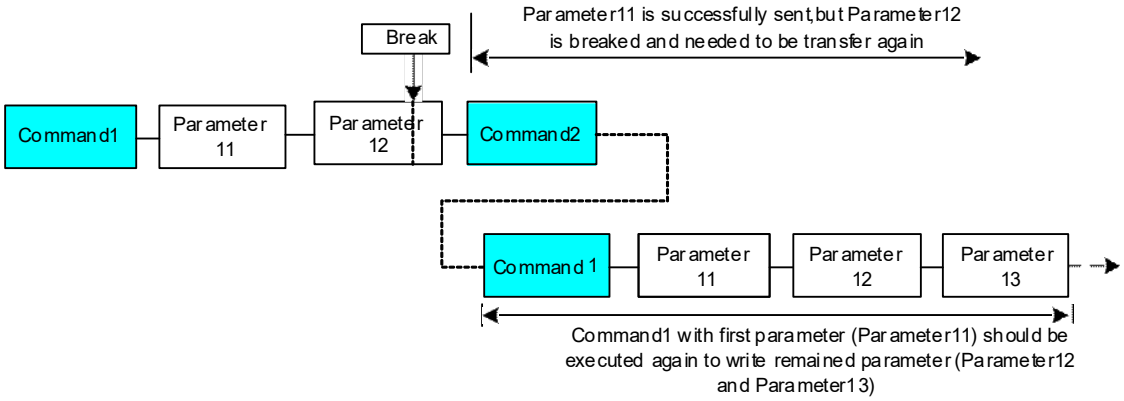


Figure 4-1-4-3 Write interrupts recovery

If one, two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

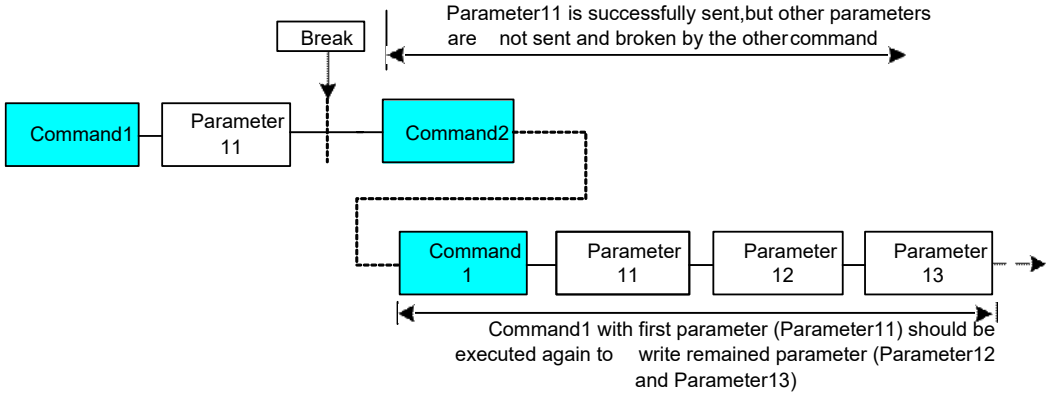
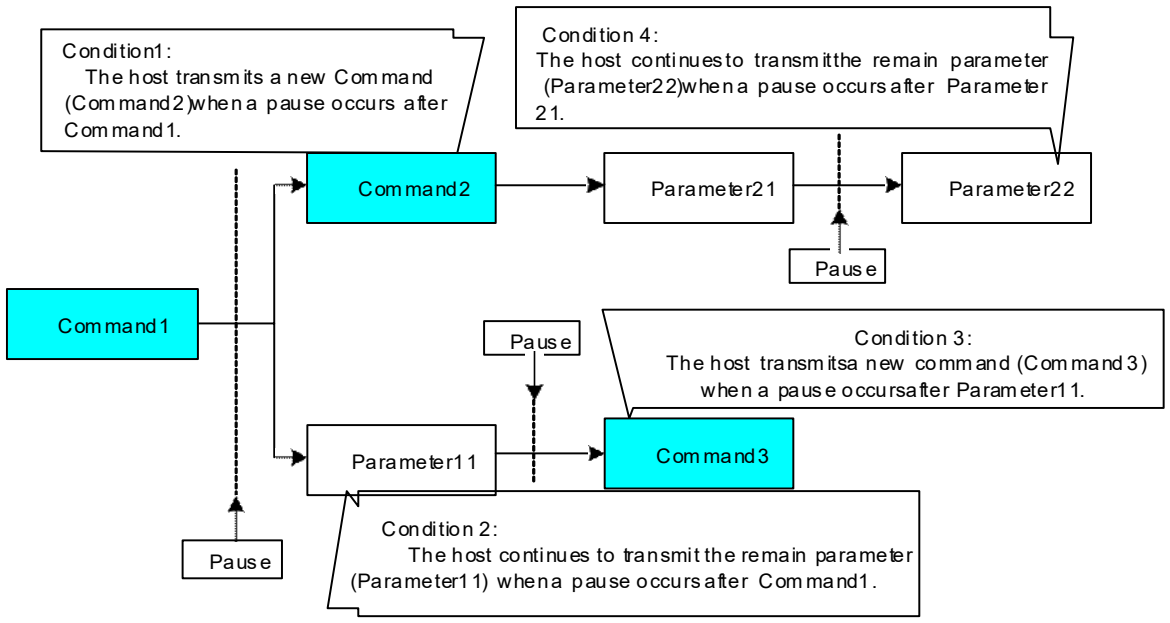


Figure 4-1-4-4 Write interrupts recovery

4.1.5. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then NV3007 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.



4.1.5.1. Serial Interface Pause (3_line)

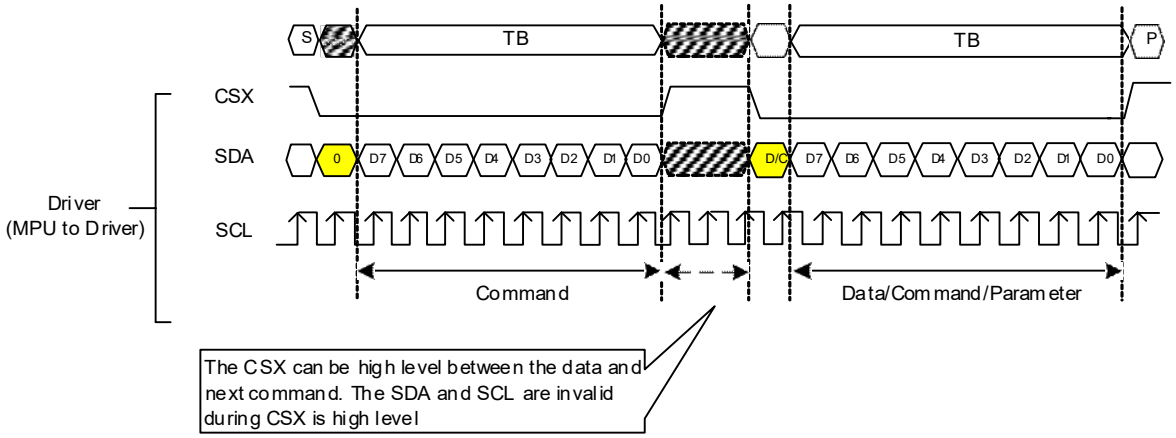


Figure 4-1-5-1 Serial Data Transfer Pause

This applies to the following 4 conditions:

(1).Command-Pause-Command

(2).Command-Pause-Parameter

(3).Parameter-Pause-Command

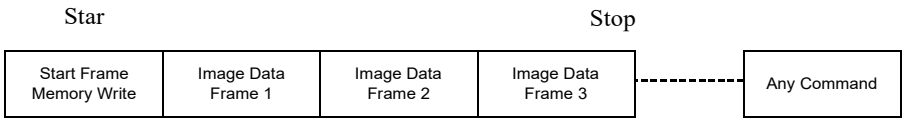
(4).Parameter-Pause-Parameter

4.1.6. Data Transfer Mode

NV3007 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

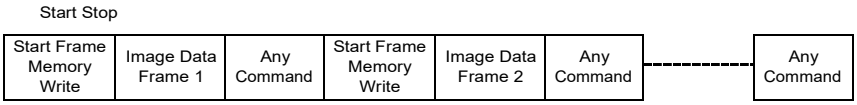
4.1.6.1. Data Transfer Method1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



4.1.6.2. Data Transfer Method2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on serial interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. Display Data Writing Format

In SPI interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bit input

-262k colors, RGB 6, 6, 6 -bit input.

4.2.1. Standard SPI 3-line RGB Format

1) . 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bit input).

In Standard SPI 3-line interface,One pixel (3 sub-pixels) display data is sent by 2 byte transfers when dbi[2:0] bits of 3Ah register are set to “101”.

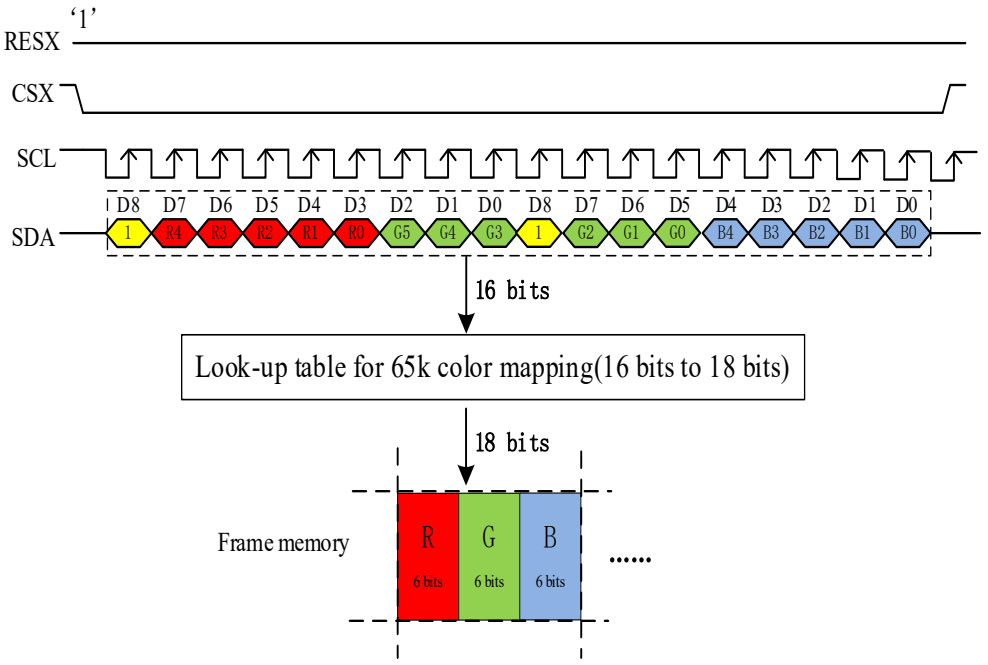


Figure 4-2-1-1 Standard SPI 3-line RGB 5-6-5 Format

2) . 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bit input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when dbi[2:0] bits of 3Ah register are set to “110”.

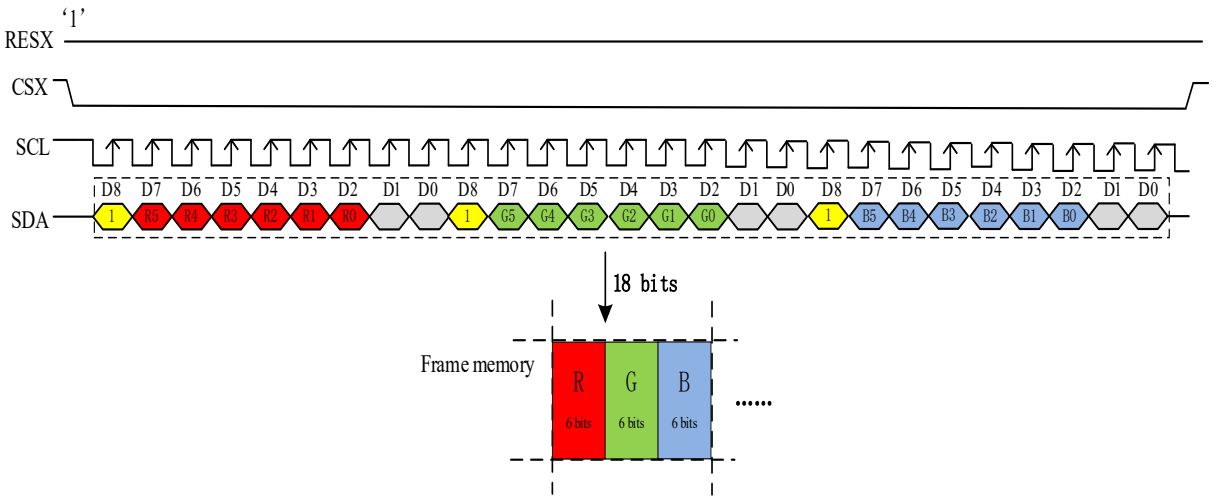


Figure 4-2-1-2 Standard SPI 3-line RGB 6-6-6 Format

4.2.2. Standard SPI 4-line RGB Format

1) . 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bit input).

In Standard SPI 4-line interface,One pixel (3 sub-pixels) display data is sent by 2 byte transfers when dbi[2:0] bits of 3Ah register are set to “101”.

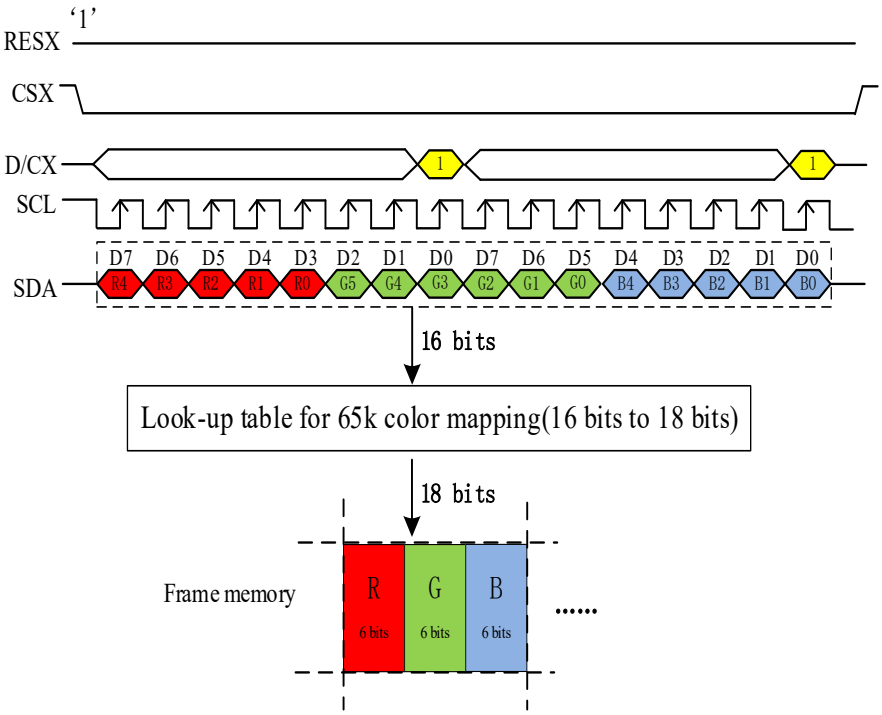


Figure 4-2-2-1 Standard SPI 4-line RGB 5-6-5 Format

2) . 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bit input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when dbi[2:0] bits of 3Ah register are set to “110”.

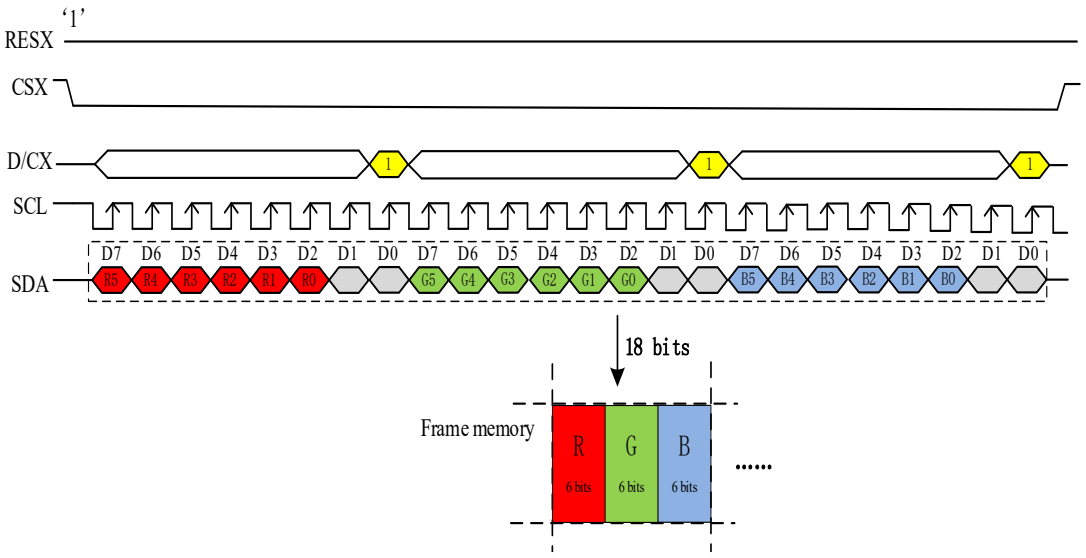


Figure 4-2-1-2 Standard SPI 4-line RGB 6-6-6 Format

4.2.3. 2-data-line mode RGB Format

2-data-lane mode consists of the chip enable input (CSX), the serial clock input (SCL), the serial data Input/output (SDA(SIO0)) and serial data Input (DCX(SIO1)).

1) . 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bit input).

1 pixel/transition(dbi[2:0]='101')

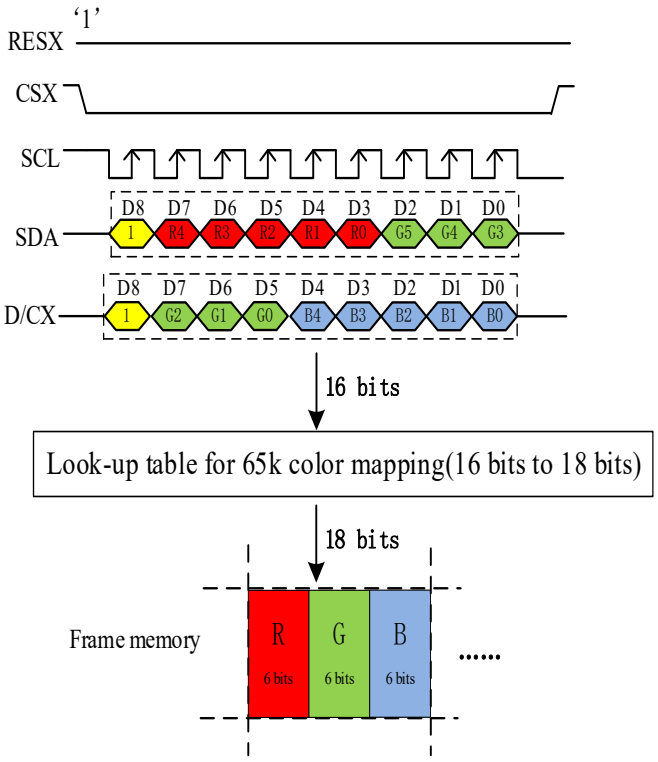


Figure 4-2-3-1 2-data-lane mode RGB 5-6-5 Format

2) . 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bit input).

1 pixel/transition(dbi[2:0]='110',mdt[1:0]='00')

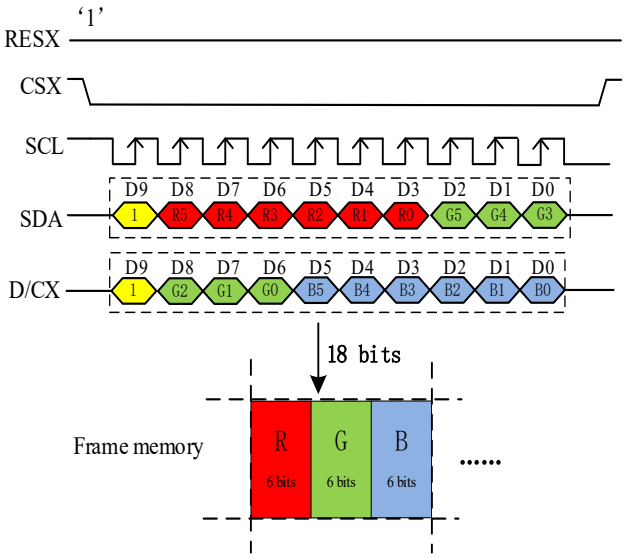


Figure 4-2-3-2 2-data-lane mode RGB 6-6-6 Format 1

2/3pixel/transition(dbi[2:0]='110',mdt[1:0]='01')

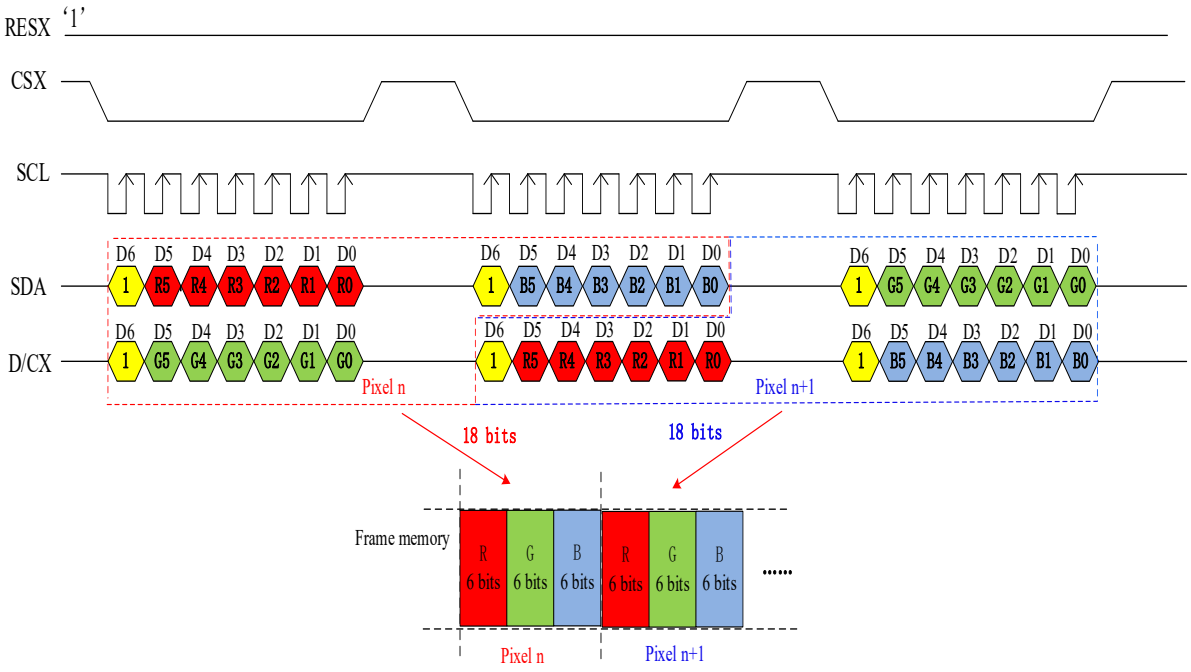


Figure 4-3-3-3 2-data-lane mode RGB 6-6-6 Format 2

4.2.4. Quad SPI 1-line RGB Format

1) . 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bit input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when dbi[2:0] bits of 3Ah register are set to “101”.

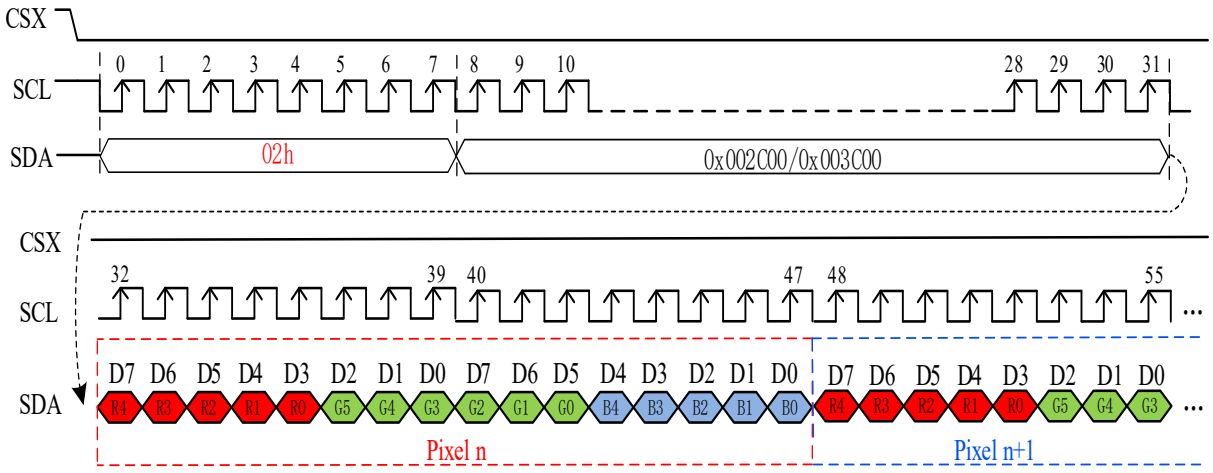


Figure 4-2-4-1 Quad SPI 1-line RGB 5-6-5 Format

2). 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when dbi[2:0] bits of 3Ah register are set to “110”.

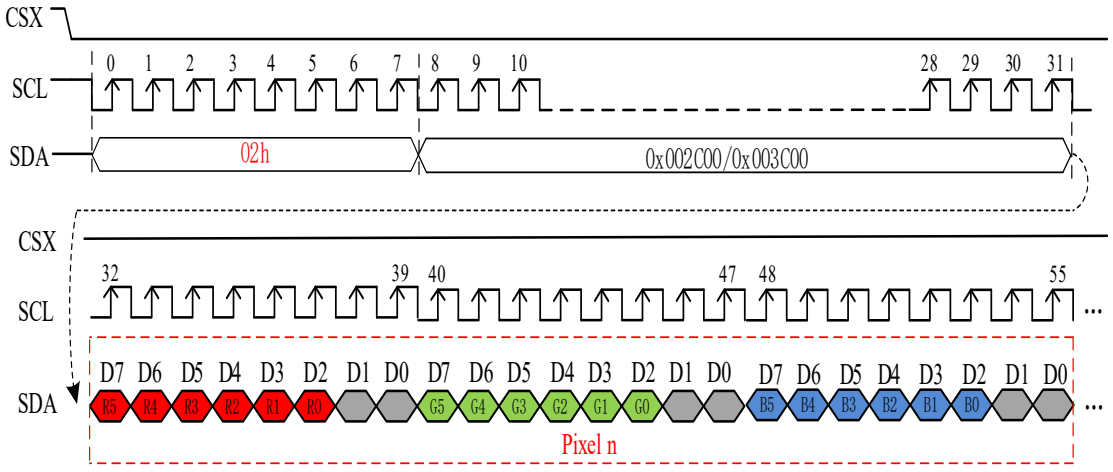


Figure 4-2-4-2 Quad SPI 1-line RGB 6-6-6 Format

4.2.5. Quad SPI 4-line RGB Format

1). 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when dbi[2:0] bits of 3Ah register are set to “101”.

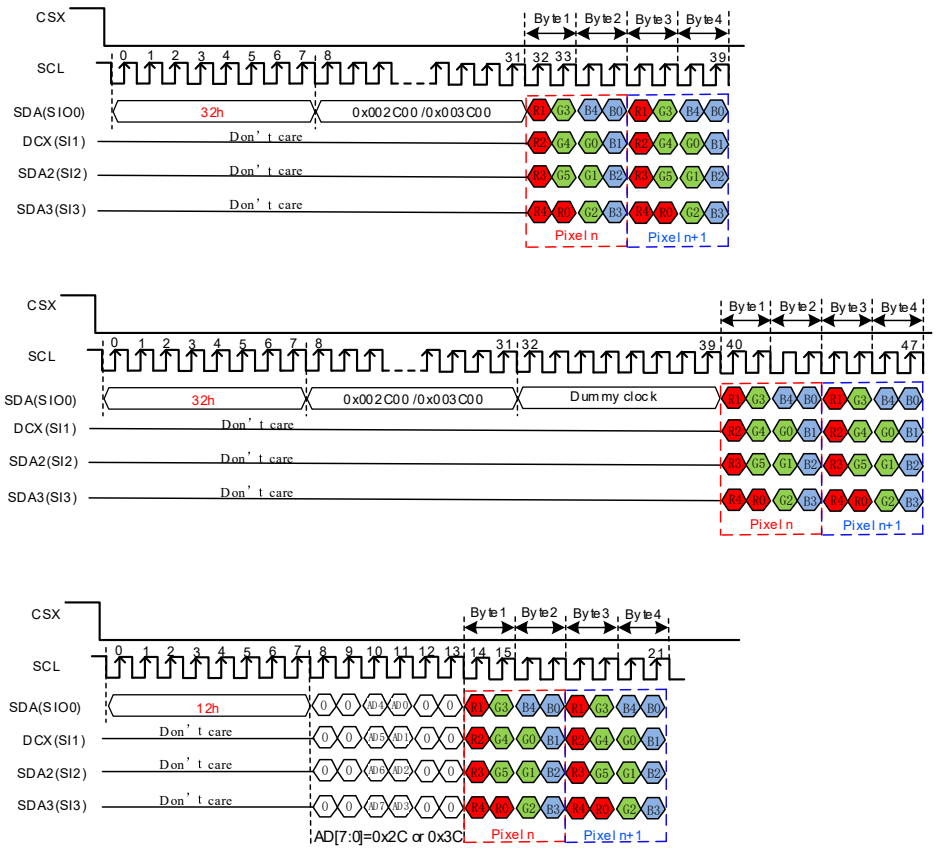


Figure 4-2-5-1 Quad SPI 4-line RGB 5-6-5 Format

2). 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when dbi[2:0] bits of 3Ah register are set to “110”.

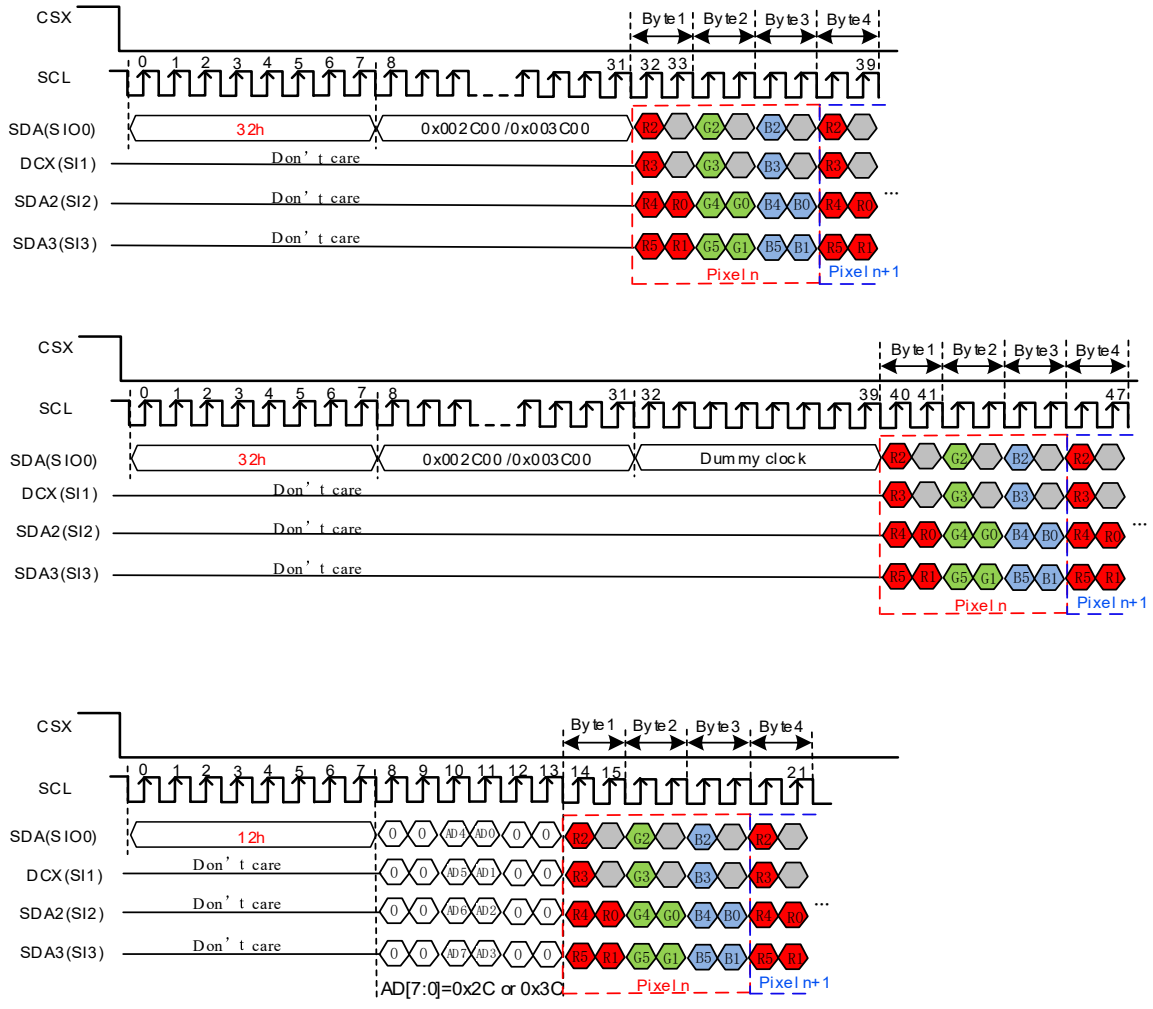


Figure 4-2-5-2 Quad SPI 4-line RGB 6-6-6 Format

5. Function Description

5.1. Display data RAM(DDRAM)

NV3007 has an integrated 168x428x18-bit graphic type static RAM. This 161,784-byte memory allows storing a 168xRGBx428 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

5.1.1. Configuration

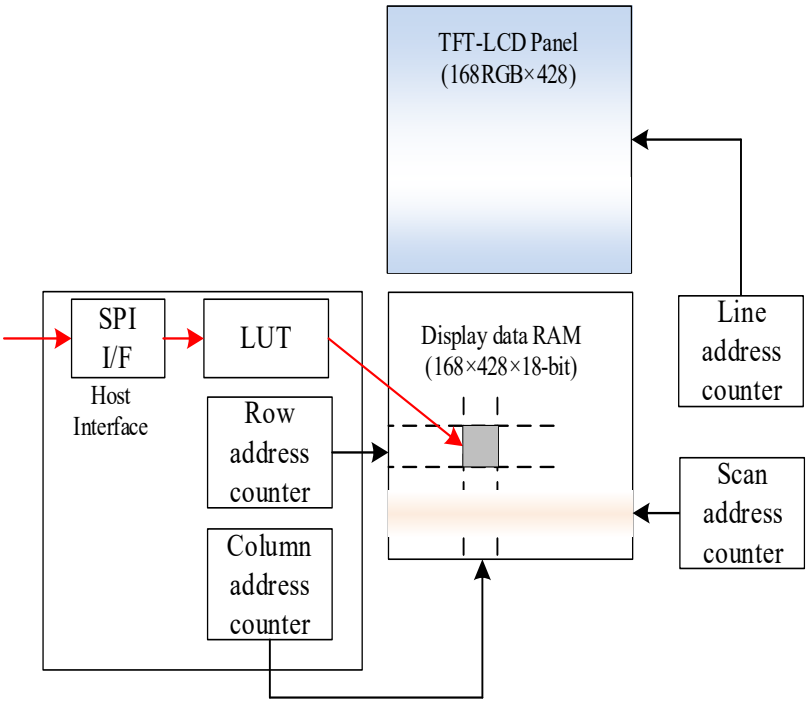


Figure 5-1-1 Configuration diagram

5.1.2. Memory to Display Address Mapping

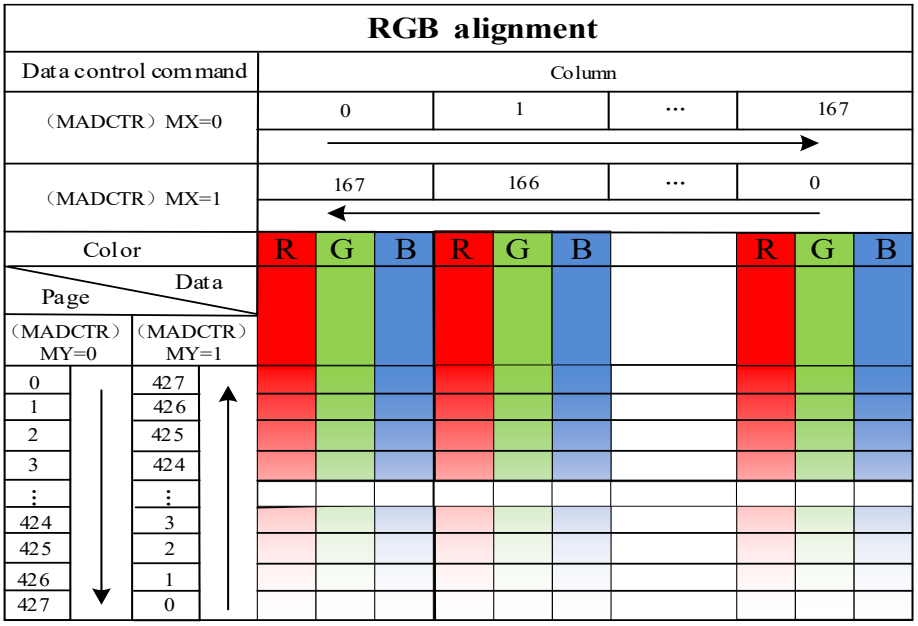


Figure 5-1-2 Memory to display address mapping diagram

5.2. Address Control

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER.The data for one pixel or two pixels is collected(RGB 6-6-6-bit), according to the data formats.As soon as this pixel-data information is complete the "Write access" is activated on the RAM.The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=167(A7h) and Y=0 to Y=427(1ABh).Addresses outside these ranges are not allowed.Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers SC, SP designating the start address and EC, EP designating the end address,

For example:

The window is defined by the following values: SC=0(0h)、SP=0(0h) and EC=167(A7h)、EP=427(1ABh)，Which means the whole display contents will be

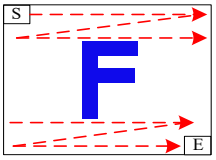
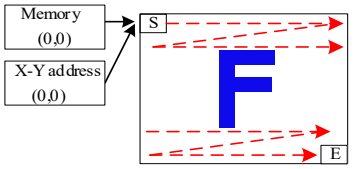
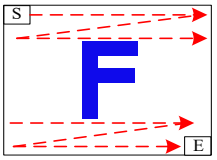
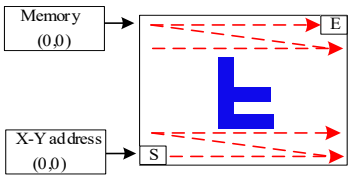
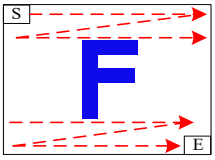
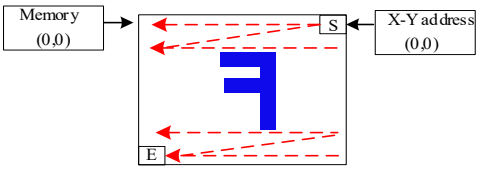
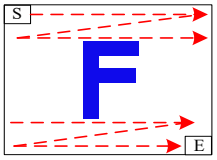
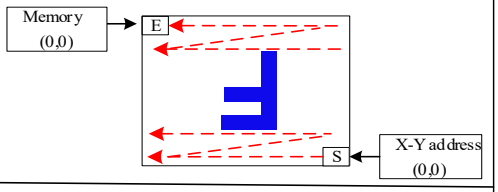
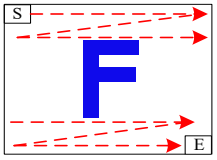
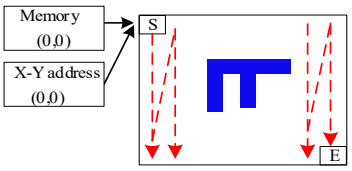
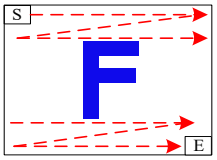
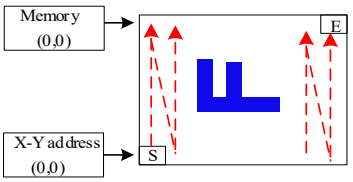
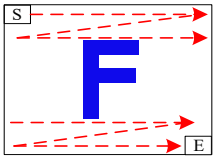
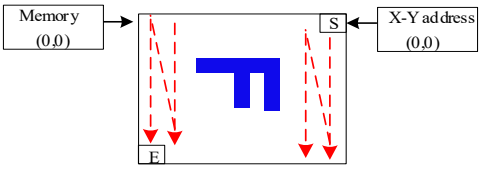
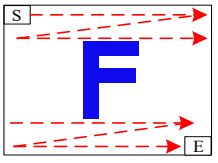
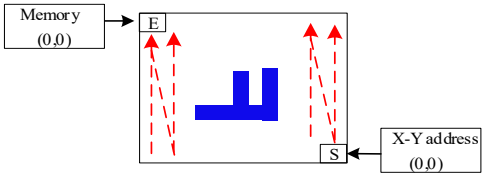
written.

In vertical addressing mode (MV=1), the Y-address increments after each bye, after the last Y-address(Y=EP), Y wraps around to SP and X increments to address the next column.In horizontal addressing mode(V=0), the X-address increments after each byte, after the last X-address (X=EC),X wraps around to SC and Y increments to address the next row. After the every last, address (X=EC and Y=EP) the address pointers wrap around to address (X=SC and Y=SP).

For flexibility in handling a wide variety of display architectures, the commands "COLSET,ROWSET and MADCTL", define flags MX and MY, which allows mirroring of the X-address and Y-address.All combinations of flags are allowed.

For each image condition, the controls for the column and row counters apply as below.

Condition	Column Counter	Row counter
When RAMWR/RAMRD command is accepted	Return to "Start column"	Return to "Start Page"
Complete Pixel Read/Write action	Increment by 1	No change
Column value is larger than "End Column"	Return to "Start column"	Increment by 1
Page value is larger than "End Page"	Return to "Start column"	Return to "Start Page"

Display Data Direction	MADCTR Parameter			Image in the host (MPU)	Image in the driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

5.3. Display Mode

NV3007 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column address is 0000h to 00A7h and row address is 0000h to 01ABh is displayed.

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0)

Normal display on mode

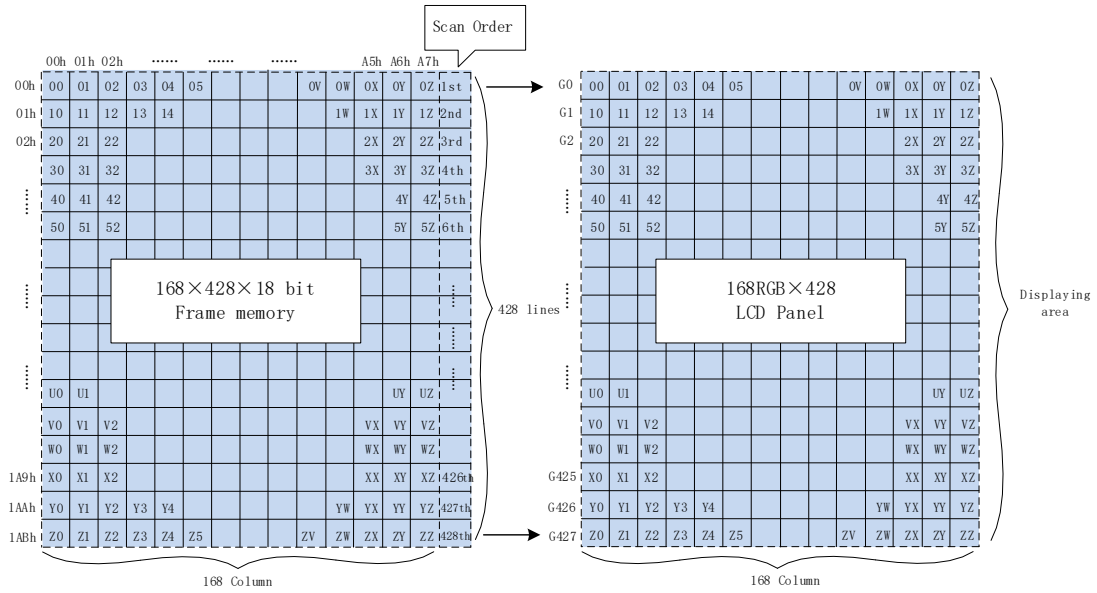


Figure 5-3-1-1 Normal display on mode

Partial display on mode

For example: When sr[8:0]=03h, er[8:0]=1A7h, MADCTL ml='0'

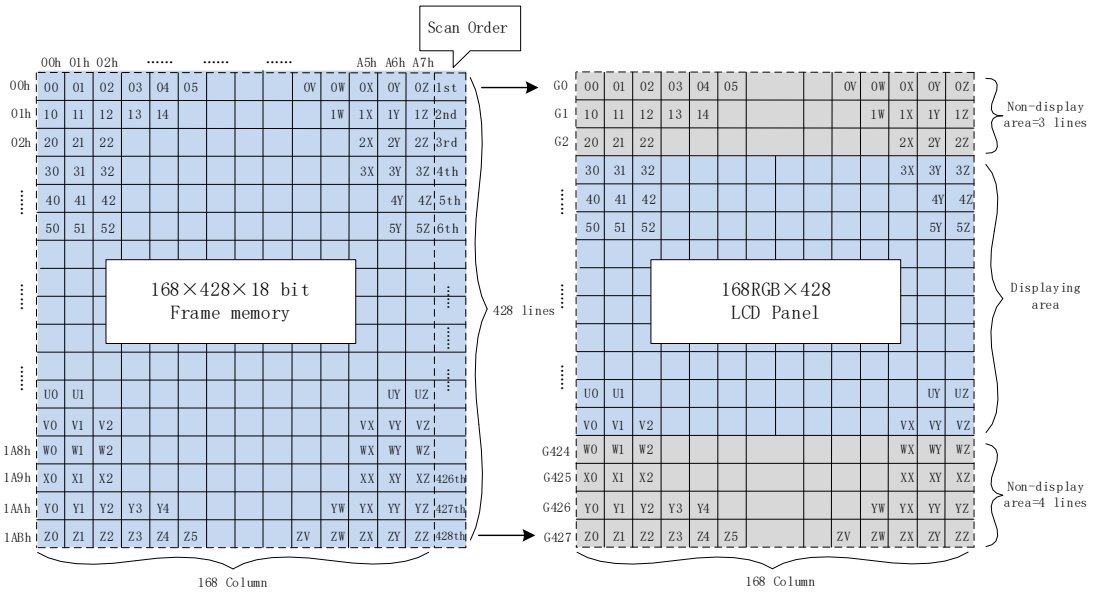


Figure 5-3-1-2 Partial display on mode

5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by TFA, VSA ,BFA bits (R33h) and VSP bits (R37h).

For example: When TFA=2, VSA=423, BFA=3,VSP=4, MADCTL ml='0'

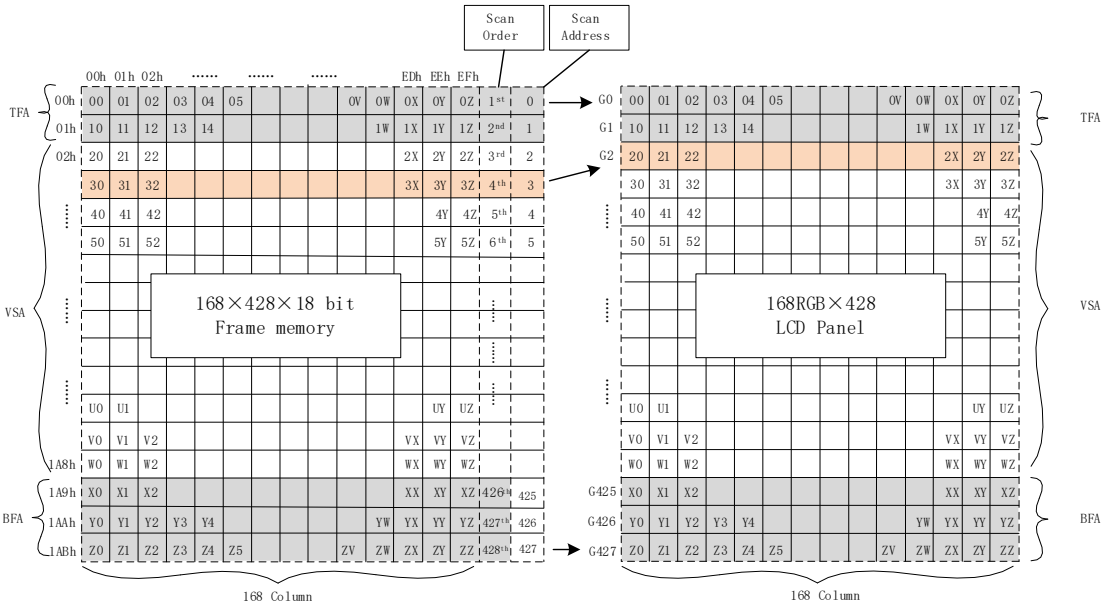


Figure 5-3-2 Vertical scroll display mode

5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off &On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.4.1. Tearing effect line modes

Mode 1： The Tearing Effect Output signal consists of V-Blanking Information only:

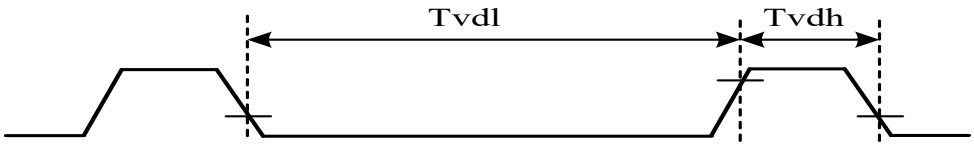


Figure 5-4-1-1 Tearing effect line mode 1

Tvdh= The LCD display is not updated from the Frame Memory

Tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2： The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 428 H-sync pulses per field.

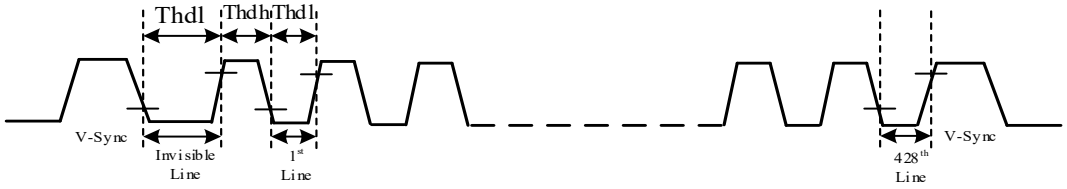


Figure 5-4-1-2 Tearing effect line mode 2

Thdh= The LCD display is not updated from the Frame Memory

Thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

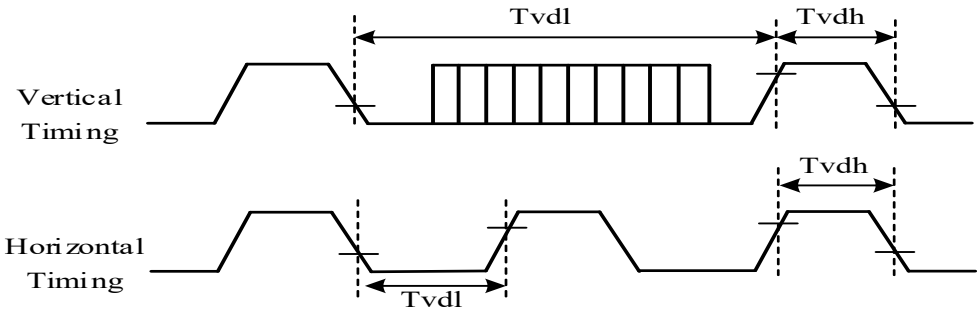
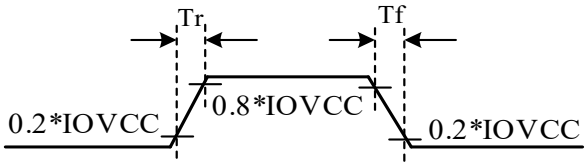


Figure 5-4-2 Tearing effect line timing

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
Tvdl	Vertical Timing Low Duration	TBD	-	ms	-
Tvdh	Vertical Timing High Duration	1000	-	us	-
Thdl	Horizontal Timing Low Duration	TBD	-	us	-
Thdh	Horizontal Timing High Duration	TBD	500	us	-

Table 5-4-2 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate=60 Hz, Ta=25C)

Note:The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

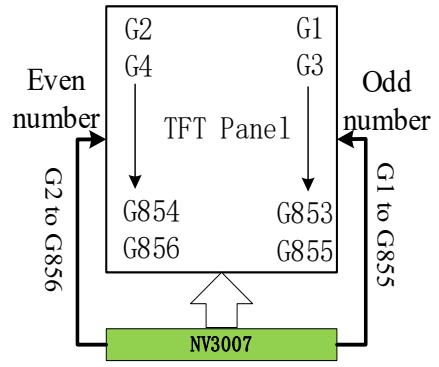
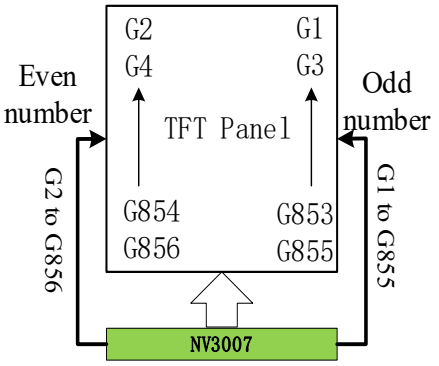
Source driver of NV3007 contains 252channels (S1~S252), is used for driving the source line of a-Si TFT LCD Panel. The source driver converts the digital data from GRAM into the analog voltage for 252 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. GIP driver

GIP driver of NV3007 contains a 24 channels (G1~G24), is used for generate dual-gate control signal on a-Si TFT LCD Panel.

5.7. Scan mode setting

GS: Sets the direction of scan by the gate driver, The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Scan Direction	Gate Output Sequence
0		G1→G2→G3→G4→ …… ……→G854→G855→G856
1		G856→G855→G854→…… ……→G4→G3→G2→G1

5.8. Gamma Correction

NV3007 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make NV3007 available with liquid crystal panels of various characteristics.

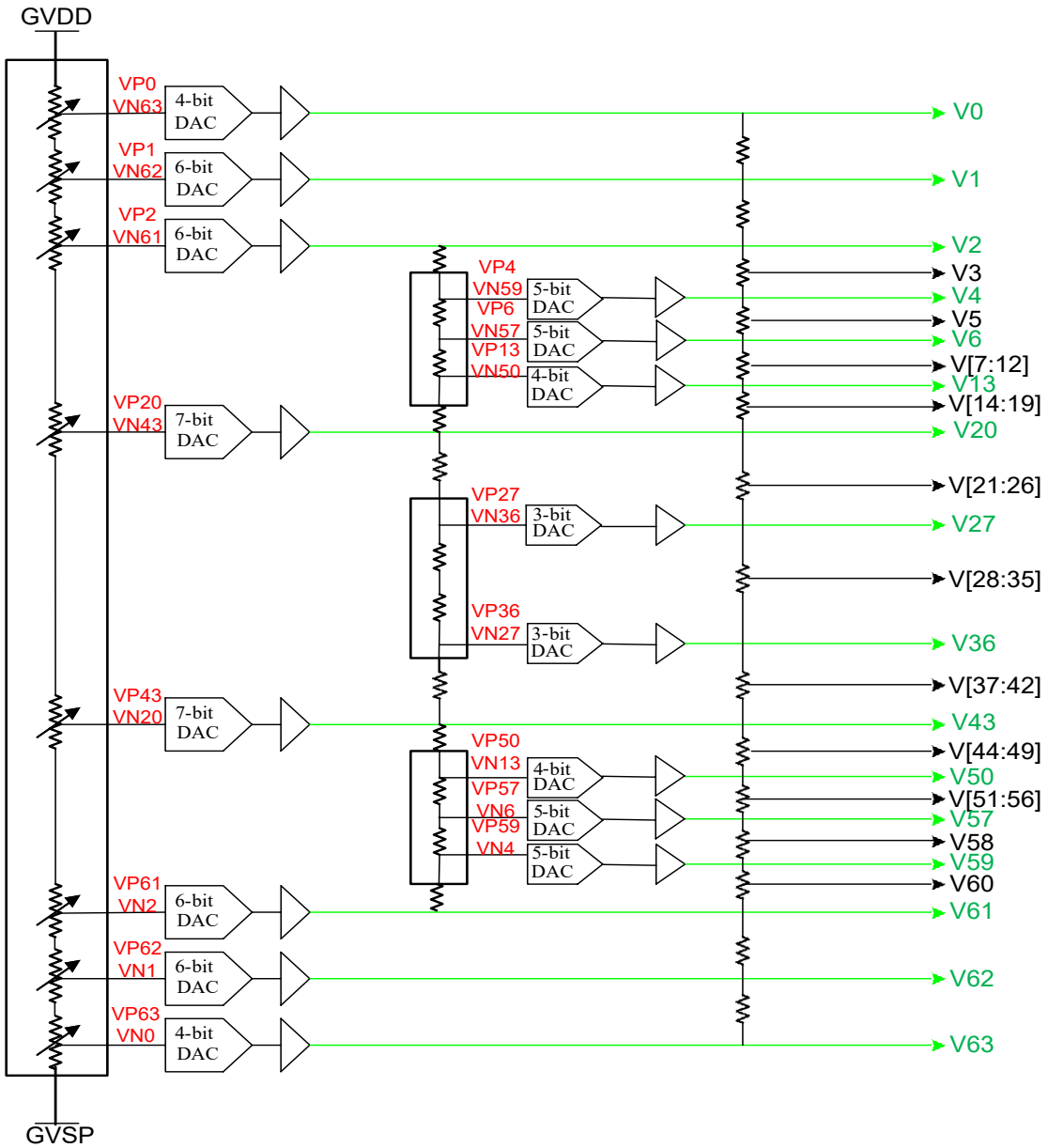


Figure 5-8-1 Gray scale Voltage Generation (Positive)

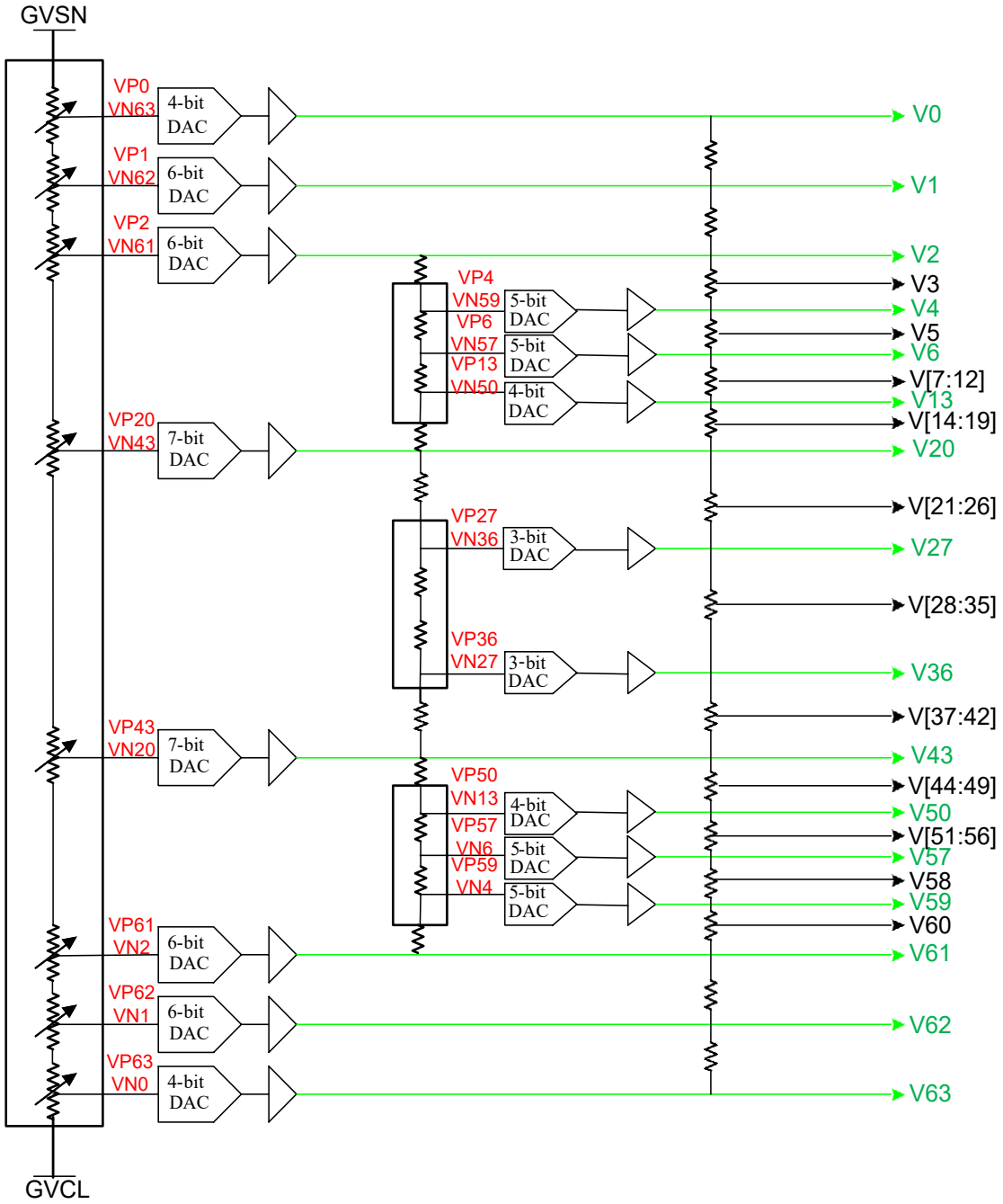


Figure 5-8-2 Gray scale Voltage Generation (Negative)

Applied Voltage to the TFT panel（Dot inversion）

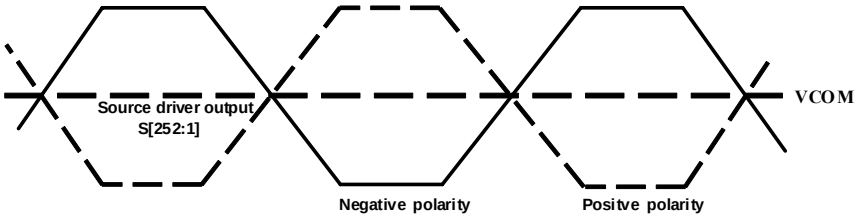


Figure 5-8-3 Relationship between Source Output and VCOM

Gamma Curve

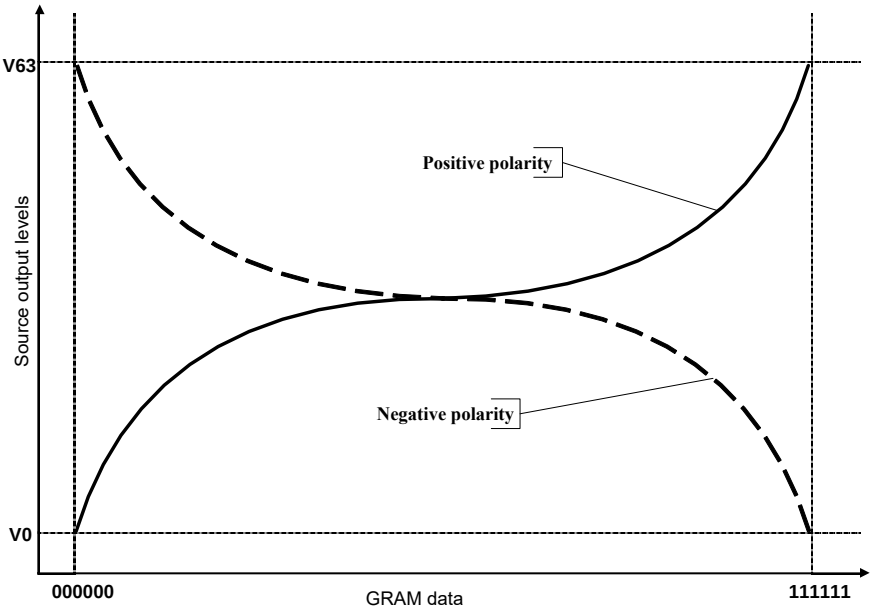


Figure 5-8-4 Gamma curve

5.9. Power Definition

5.9.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the SPI interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note:

1. Transition between modes 1-5 is controllable by MPU commands.

2. Mode 6 is entered only when both Power supplies for I/O and analog circuits are removed.

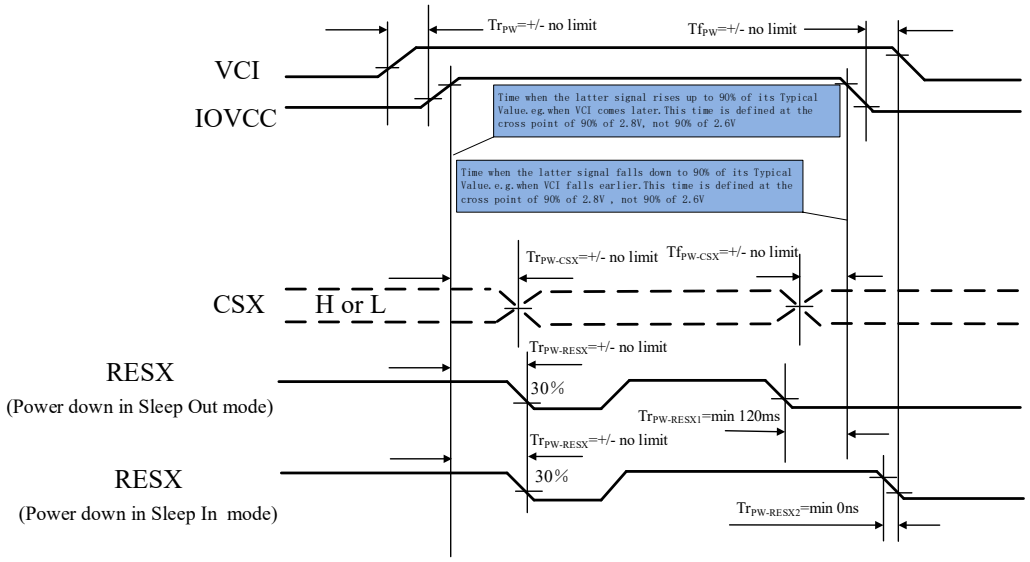
5.9.2. Power On/Off Sequence

IOVCC and VCI can be applied in any order.

VCI and IOVCC can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.



$Tr_{PW\text{-}RESX1}$ is applied to RESX falling in Sleep Out Mode

$Tr_{PW\text{-}RESX2}$ is applied to RESX falling in Sleep In Mode

Notes:

1. There will be no damage to the NV3007 if the power sequences are not met.

2.There will be no abnormal visible effects on the display panel during the Power On/Off Sequence.

3.There will be no abnormal visible effects on the display between the end of Power On Sequence and before receiving the Sleep Out command, and also between receiving the Sleep In command and the Power Off Sequence.

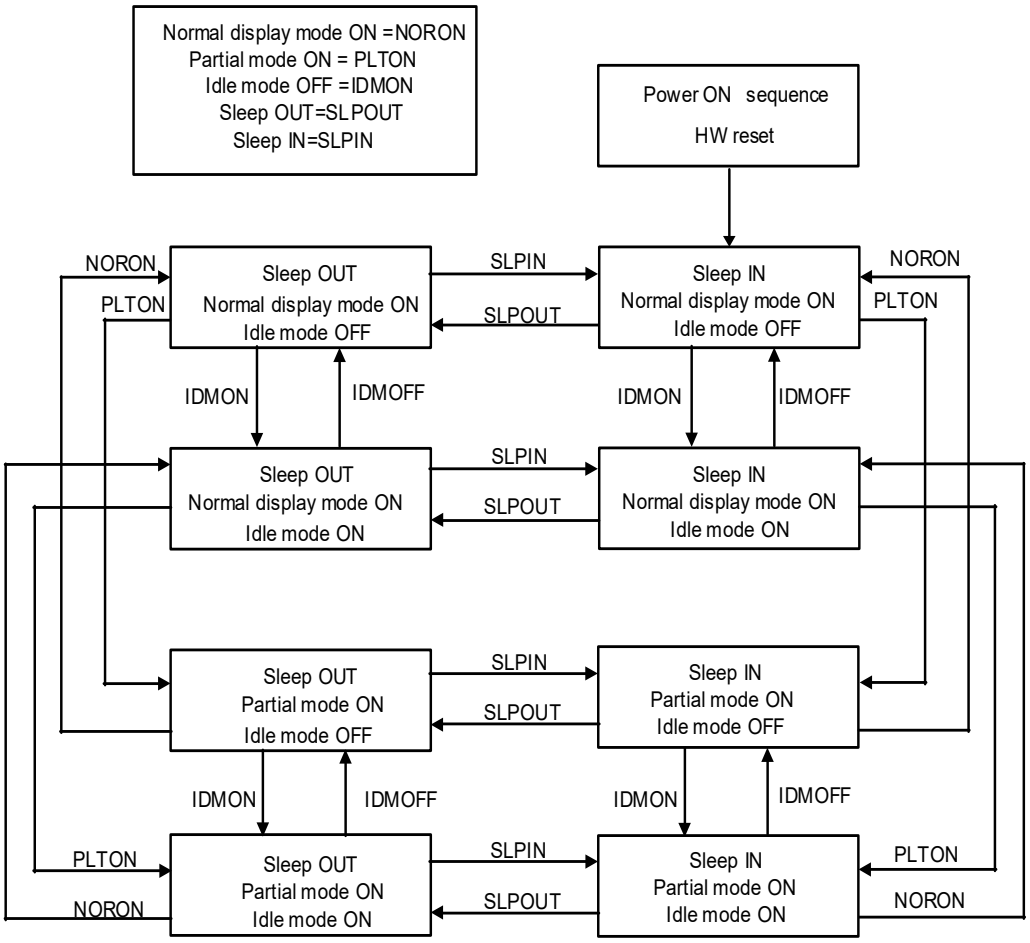
4. If the RESX line is not steadily held by the host during the Power On Sequence as defined above, then it will be necessary to apply the Hardware Reset (RESX) after the completion of the Host Power On Sequence to ensure correct operations. Otherwise, all the functions are not guaranteed.

5.9.3. Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the TFT panel will not display and there will not any visible effect on the display until “Power On Sequence”powers it up.

5.9.4. Power Flow Chart



Notes:

1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.9.5. LCD power generation circuit

5.9.5.1. Power supply circuit

The power circuit of NV3007 is used to generate supply voltages for LCD panel driving.

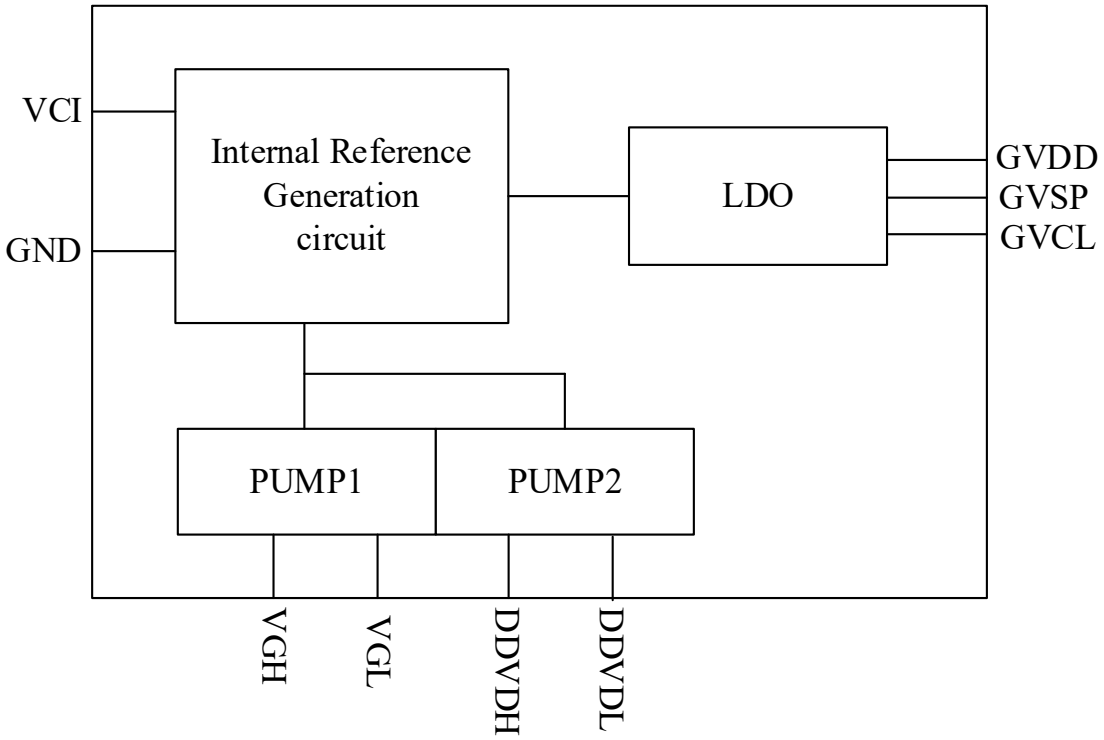


Figure 5-9-5-1 Power supply circuit

5.9.5.2. LCD power generation scheme

The boost voltage generated is shown as below.

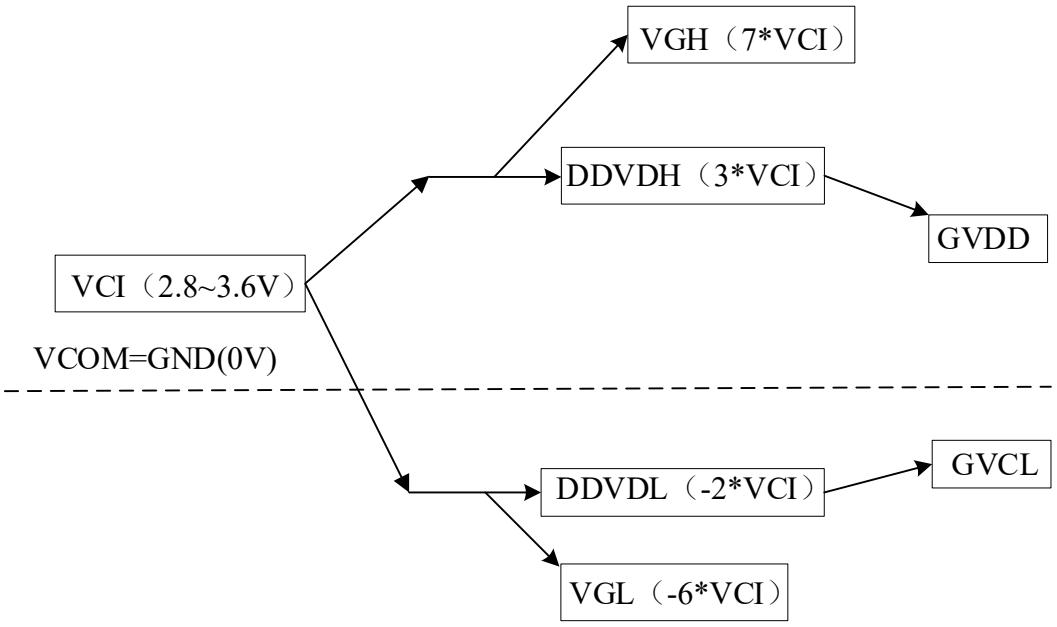


Figure 5-9-5-2 LCD power generation scheme

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5.10. Input/output pin state

5.10.1. Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
SDA	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low

Table 5-10-1 Characteristics of output pins

5.10.2. Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
SDA2	Input invalid	Input valid	Input valid	Input invalid
SDA3	Input invalid	Input valid	Input valid	Input invalid
IM[1:0]	Input invalid	Input valid	Input valid	Input invalid

Table 5-10-2 Characteristics of input pins

6. Command

6.1. Command List

6.1.1. Public Registers Command

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
NOP	00	W									00
RDDIDIF	04	Multi-R	sys_id1[7:0]								30
			sys_id2[7:0]								07
			sys_id3[7:0]								01
RDDST	09	Multi-R	pump_en	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr			/
				dbi[2:0]			color8_en	ptl_on	slpout	normal_on	/
			scroll_on		inv_on	gs	ss	disp_en	te_on		/
					telom						/
SLPIN	10	W									/
SLPOUT	11	W									/
PARMON	12	W									/
NORMON	13	W									/
INVOFF	20	W									/
INVON	21	W									/
DISPOFF	28	W									/
DISPON	29	W									/
COLSET	2A	Multi-W								sc[8]	00
			sc[7:0]								00
										ec[8]	00
			ec[7:0]								EF
ROWSET	2B	Multi-W								sp[8]	00
			sp[7:0]								00
										ep[8]	00
			ep[7:0]								EF
MEMWR	2C	W								cmd_2c_start	00
MEMRD	2E	R									/
PAREA	30	Multi-W								sr[8]	00

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
			sr[7:0]								00
										er[8]	00
			er[7:0]								EF
VSDEF	33	Multi-W								tfa[8]	00
			tfa[7:0]								00
										vsa[8]	00
			vsa[7:0]								F0
										bfa[8]	00
			bfa[7:0]								00
TEOFF	34	W									/
TEON	35	W								telom	00
MADCTRL	36	W	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr	sys_mh			00
VSSAD	37	Multi-W								vsp[8]	00
			vsp[7:0]								00
IDLEOFF	38	W									/
IDLEON	39	W									/
PFSET	3A	W						dbi[2:0]			06
WRMEMC	3C	W									/
HSDEF	3D	Multi-W								lfa[8]	00
			lfa[7:0]								00
										hsa[8]	00
			hsa[7:0]								F0
										rfa[8]	00
			rfa[7:0]								00
HSSAD	3E	Multi-W								hsp[8]	00
			hsp[7:0]								00

6.1.2. Private Registers Command

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
IFCTRL1	40	W				sdo_hiz					00
IFCTRL2	41	W								spi_2dat_en	00
IFCTRL3	42	W				qspi_bgr			qspi_dummy	qspi_sbyte	00
IFCTRL4	43	W				endian	epf[1:0]		mdt[1:0]		04
TECTRL1	44	Multi-W						sts[10:8]			00
			sts[7:0]								00
TECTRL2	45	Multi-R						sts[10:8]			/
			sts[7:0]								/
TECTRL3	46	W				te_oe			te_pol	te_extend	00
TECTRL4	47	Multi-W						te_v_start[10:8]			00
			te_v_start[7:0]								00
								te_v_end[10:8]			00
			te_v_end[7:0]								00
TECTRL5	48	Multi-W								te_h_start[8]	00
			te_h_start[7:0]								00
										te_h_end[8]	00
			te_h_end[7:0]								00
SCANCTRL	49	W						gs		ss	01
OTPCTRL1	4A	W		otp_ptm[1:0]		otp_pwe	otp_prd	otp_pprog	otp_vpp_sel	otp_vpp_src_sel	00
OTPCTRL2	4B	W	otp_pa[7:0]								00
OTPCTRL3	4C	W	otp_pdin[7:0]								00
OTPCTRL4	4D	Multi-R	otp_rd_dat[7:0]								/
											/
USRMAD	4F	W	usr_my	usr_mx	usr_mv	usr_ml	usr_bgr	usr_mh			00
ITCTRL1	53	W	inter_vbp[7:0]								0C
ITCTRL2	54	W		inter_vfp[6:0]							08

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
ITCTRL3	55	W	inter_hbp[7:0]								25
ITCTRL4	56	W	inter_hfp[7:0]								25
IBIASCTRL	57	W			bias_sd_adj[1:0]		bias_gma_adj[1:0]		bias_adj[1:0]		2A
LVDCTRL	59	W		lvd_rec_bypass	lvd_rec_goa_sel	lvd_en		1	lvd_sel[1:0]		15
RAMCTRL1	5C	W							mec_restart	mbist_disable	00
RAMCTRL2	5D	W		td1sel_l	td2sel_l	td3sel_l		td1sel_r	td2sel_r	td3sel_r	00
RDBIST	5E	Multi-R	mec_restart	mec_enable	mbist_done	mbist_abort	l_mec_pxl1_hit	l_mec_pxl2_hit	r_mec_pxl1_hit	r_mec_pxl2_hit	/
							l_mec_pxl1_row[8]	l_mec_pxl2_row[8]	r_mec_pxl1_row[8]	r_mec_pxl2_row[8]	/
			l_mec_pxl1_row[7:0]								/
				l_mec_pxl1_col[6:0]							/
			l_mec_pxl2_row[7:0]								/
				l_mec_pxl2_col[6:0]							/
			r_mec_pxl1_row[7:0]								/
				r_mec_pxl1_col[6:0]							/
			r_mec_pxl2_row[7:0]								/
				r_mec_pxl2_col[6:0]							/
GAMCTRL1	60	W					vrp0[3:0]				00
GAMCTRL2	61	W			vrp1[5:0]						06
GAMCTRL3	62	W			vrp2[5:0]						0c
GAMCTRL4	63	W				vrp4[4:0]					0b
GAMCTRL5	64	W				vrp6[4:0]					0a
GAMCTRL6	65	W					vrp13[3:0]				06
GAMCTRL7	66	W		vrp20[6:0]							30
GAMCTRL8	67	W		vrp27[2:0]				vrp36[2:0]			43
GAMCTRL9	68	W		vrp43[6:0]							44
GAMCTRL10	69	W					vrp50[3:0]				08
GAMCTRL11	6A	W				vrp57[4:0]					12
GAMCTRL12	6B	W				vrp59[4:0]					14
GAMCTRL13	6C	W			vrp61[5:0]						29

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
GAMCTRL14	6D	W	vrp62[5:0]								31
GAMCTRL15	6E	W					vrp63[3:0]				0f
GAMCTRL16	6F	W			vj0p63[1:0]				vj1p63[1:0]		00
GAMCTRL17	70	W					vrn0[3:0]				00
GAMCTRL18	71	W	vrn1[5:0]								06
GAMCTRL19	72	W	vrn2[5:0]								0c
GAMCTRL20	73	W				vrn4[4:0]					0a
GAMCTRL21	74	W				vrn6[4:0]					09
GAMCTRL22	75	W					vrn13[3:0]				07
GAMCTRL23	76	W	vrn20[6:0]								30
GAMCTRL24	77	W	vrn27[2:0]					vrn36[2:0]			34
GAMCTRL25	78	W	vrn43[6:0]								44
GAMCTRL26	79	W					vrn50[3:0]				08
GAMCTRL27	7A	W				vrn57[4:0]					13
GAMCTRL28	7B	W				vrn59[4:0]					13
GAMCTRL29	7C	W	vrn61[5:0]								29
GAMCTRL30	7D	W	vrn62[5:0]								31
GAMCTRL31	7E	W					vrn63[3:0]				0f
GAMCTRL32	7F	W			vj0n63[1:0]				vj1n63[1:0]		00
RGLRCTRL1	80	Multi-W									00
			gma_bias_adj[3:0]					dvdd_adj[2:0]			a0
RGLRCTRL2	81	W	bgr_adj[3:0]				vref_adj[3:0]				00
VDDSCTRL	82	W						vdds_trim[2:0]			00
GLDOCTRL1	83	W	gvcl_reg[7:0]								56
GLDOCTRL2	84	W	gvdd_reg[7:0]								d0
GLDOCTRL3	85	W		gvsp_reg[6:0]							3F
ESDCTRL2	8B	W	esd_enable	esd_rd_sram	esd_load_status	esd_reload_otp	esd_force_analog_1	esd_force_clk_1	esd_force_cs_1	esd_force_dc_1	1f
ESDCTRL3	8C	R	esd_det[3:0]					esd_occured			
GLDOCTRL4	8D	W		vcom_ofc_reg[6:0]							00
RDOTPLD	8E	R						por	lvd	otp_loading	/
PWRCTRL1	8F	Multi-W		vgh_clk_sel[2:0]				vgl_clk_sel[2:0]			22
								mv_clk_sel[2:0]			04

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
PWRCTRL2	90	Multi-W	ddvdh_drain_row_on[8]	ddvdh_drain_row_off[8]			ddvdh_drain_frm_on[1:0]		ddvdh_drain_frm_off[1:0]		45
			ddvdh_drain_row_on[7:0]								C8
			ddvdh_drain_row_off[7:0]								2C
PWRCTRL3	91	Multi-W	ddvdh_en_row_on[8]	ddvdh_en_row_off[8]			ddvdh_en_frm_on[1:0]		ddvdh_en_frm_off[1:0]		81
			ddvdh_en_row_on[7:0]								2C
			ddvdh_en_row_off[7:0]								C8
PWRCTRL4	92	Multi-W	ddvdl_en_row_on[8]	ddvdl_en_row_off[8]			ddvdl_en_frm_on[1:0]		ddvdl_en_frm_off[1:0]		81
			ddvdl_en_row_on[7:0]								2C
			ddvdl_en_row_off[7:0]								C8
PWRCTRL5	93	Multi-W	mv_disch_row_on[8]	mv_disch_row_off[8]			mv_disch_frm_on[1:0]		mv_disch_frm_off[1:0]		81
			mv_disch_row_on[7:0]								2D
			mv_disch_row_off[7:0]								C7
PWRCTRL6	94	Multi-W	vgh_en_row_on[8]	vgh_en_row_off[8]			vgh_en_frm_on[1:0]		vgh_en_frm_off[1:0]		44
			vgh_en_row_on[7:0]								00
			vgh_en_row_off[7:0]								2C
PWRCTRL7	95	Multi-W	vgh_disch_row_on[8]	vgh_disch_row_off[8]			vgh_disch_frm_on[1:0]		vgh_disch_frm_off[1:0]		44
			vgh_disch_row_on[7:0]								01
			vgh_disch_row_off[7:0]								8F
PWRCTRL8	96	Multi-W	vgh_drain_row_on[8]	vgh_drain_row_off[8]			vgh_drain_frm_on[1:0]		vgh_drain_frm_off[1:0]		C0
			vgh_drain_row_on[7:0]								2b
			vgh_drain_row_off[7:0]								90
PWRCTRL9	97	Multi-W	vgl_en_row_	vgl_en_row_			vgl_en_frm_on[1:0]		vgl_en_frm_off[1:0]		81

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
			on[8]	off[8]							
			vgl_en_row_on[7:0]								90
			vgl_en_row_off[7:0]								00
PWRCTRL10	98	Multi-W	vgl_disch_row_on[8]	vgl_disch_row_off[8]			vgl_disch_frm_on[1:0]		vgl_disch_frm_off[1:0]		81
			vgl_disch_row_on[7:0]								91
			vgl_disch_row_off[7:0]								63
PWRCTRL11	99	Multi-W	vgl_drain_row_on[8]	vgl_drain_row_off[8]			vgl_drain_frm_on[1:0]		vgl_drain_frm_off[1:0]		81
			vgl_drain_row_on[7:0]								F4
			vgl_drain_row_off[7:0]								64
PWRCTRL12	9A	W			ddvdh_btvs[1:0]		ddvdh_btvs_en				28
PWRCTRL13	9B	W			ddvdl_btvs[1:0]		ddvdl_btvs_en				18
PWRCTRL14	9C	W	vgh_noreg		vgh_bth[1:0]						A0
PWRCTRL15	9D	W						vgh_set[2:0]			03
PWRCTRL16	9E	W	vgl_btrs	vgl_noreg				vgl_set[2:0]			C2
PWRCTRL17	9F	Multi-W	gam_ref_bypass		vdds_en_bypass	vref_en_bypass	vgl_drain_bypass	vgl_disch_bypass	gam_en_bypass	pump_ctrl_en	00
			vgl_en_bypass	vgh_drain_bypass	vgh_disch_bypass	vgh_en_bypass	mv_disch_bypass	ddvdl_en_bypass	ddvdh_en_bypass	ddvdh_drain_bypass	00
			sd_n_en_bypass							sd_en_bypass	04
GOACTRL	A0	Multi-W			1	goa_slpin_sel[2:0]			map_sel[1:0]		28
			goa_vds_slpin_sel[2:0]			goa_gcl_slpin_sel[2:0]			level_sel[1:0]		24
						exit_disp_hiz_enable	exit_disp_hiz_num[3:0]				00
VSTCTRL1	A1	W	goa_vst1_shift[7:0]								8A

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
VSTCTRL2	A2	W	goa_vst2_shift[7:0]								89
VSTCTRL3	A3	W	goa_vst3_shift[7:0]								88
VSTCTRL4	A4	W	goa_vst4_shift[7:0]								87
VSTCTRL5	A5	W	vst_gnd1_period[7:0]								0A
VSTCTRL6	A6	W	vst_gnd2_period[7:0]								0A
VSTCTRL7	A7	W	vst_vci_period[7:0]								0A
VSTCTRL8	A8	W	goa_vst_tchop[8]	goa_vst_tglue[8]	vst_noverlap[1:0]		goa_vst_width[3:0]				04
VSTCTRL9	A9	W	goa_vst_tchop[7:0]								2B
VSTCTRL10	AA	W	goa_vst_tglue[7:0]								00
VENDCTRL1	AB	Multi-W						goa_vend1_shift_start[10:8]			00
			goa_vend1_shift_start[7:0]								04
VENDCTRL2	AC	Multi-W						goa_vend1_shift_end[10:8]			02
			goa_vend1_shift_end[7:0]								7C
VENDCTRL3	AD	Multi-W						goa_vend2_shift_start[10:8]			00
			goa_vend2_shift_start[7:0]								04
VENDCTRL4	AE	Multi-W						goa_vend2_shift_end[10:8]			02
			goa_vend2_shift_end[7:0]								7C
VENDCTRL5	AF	Multi-W					all_gate_hiz_period[3:0]				03
					all_gate_nov_period[5:0]						04
			all_gate_vci_period[7:0]								0A
VENDCTRL6	B0	Multi-W	eclk_gnd1_period[7:0]								0A
			eclk_gnd2_period[7:0]								0A
			eclk_vci_period[7:0]								0A
									eclk_noverlap[1:0]		00
VENDCTRL9	B3	W	vend_gnd1_period[7:0]								0A
VENDCTRL10	B4	W	vend_gnd2_period[7:0]								0A
VENDCTRL11	B5	W	vend_vci_period[7:0]								0A
VENDCTRL12	B6	Multi-W	goa_vend_tchop[8]	goa_vend_tglue[8]	vend_noverlap[1:0]		goa_vend1_glass_sel	goa_vend2_glass_sel	goa_rst_shift2_en	bw_fw_sel	06
			vds_noverlap[3:0]				eck_noverlap[3:0]				00
VENDCTRL13	B7	W	goa_vend_tchop[7:0]								44

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
VENDCTRL14	B8	W	goa_vend_tglue[7:0]								44
CLKCTRL1	B9	W	goa_clk1_shift[7:0]								82
CLKCTRL2	BA	W	goa_clk2_shift[7:0]								81
CLKCTRL3	BB	W	goa_clk3_shift[7:0]								80
CLKCTRL4	BC	W	goa_clk4_shift[7:0]								01
CLKCTRL5	BD	W	goa_clk5_shift[7:0]								86
CLKCTRL6	BE	W	goa_clk6_shift[7:0]								85
CLKCTRL7	BF	W	goa_clk7_shift[7:0]								84
CLKCTRL8	C0	W	goa_clk8_shift[7:0]								83
CLKCTRL9	C1	W	clk_gnd1_period[7:0]								0A
CLKCTRL10	C2	W	clk_gnd2_period[7:0]								0A
CLKCTRL11	C3	W	clk_vci_period[7:0]								0A
CLKCTRL12	C4	W	goa_clk_tchop[8]	goa_clk_tglue[8]	clk_noverlap[1:0]		goa_clk_width[3:0]				03
CLKCTRL13	C5	W	goa_clk_tchop[7:0]								2B
CLKCTRL14	C6	W	goa_clk_tglue[7:0]								00
CLKCTRL15	C7	W					duty_block[3:0]				00
CLKCTRL16	C8	Multi-W		goa_clk1_switch[10:8]				goa_clk2_switch[10:8]			22
				goa_clk3_switch[10:8]				goa_clk4_switch[10:8]			22
CLKCTRL17	C9	W	goa_clk1_switch[7:0]								73
CLKCTRL18	CA	W	goa_clk2_switch[7:0]								74
CLKCTRL19	CB	W	goa_clk3_switch[7:0]								75
CLKCTRL20	CC	W	goa_clk4_switch[7:0]								76
CLKCTRL21	CD	Multi-W		goa_clk5_switch[10:8]				goa_clk6_switch[10:8]			22
				goa_clk7_switch[10:8]				goa_clk8_switch[10:8]			22
CLKCTRL22	CE	W	goa_clk5_switch[7:0]								6F
CLKCTRL23	CF	W	goa_clk6_switch[7:0]								70
CLKCTRL24	D0	W	goa_clk7_switch[7:0]								71
CLKCTRL25	D1	W	goa_clk8_switch[7:0]								72
RSTCTRL1	D2	W	goa_rst_shift1[7:0]								8E
RSTCTRL2	D3	Multi-W						goa_rst_shift2[10:8]			02
			goa_rst_shift2[7:0]								75
RSTCTRL3	D4	W	rst_gnd1_period[7:0]								0A
RSTCTRL4	D5	W	rst_gnd2_period[7:0]								0A
RSTCTRL5	D6	W	rst_vci_period[7:0]								0A

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
RSTCTRL6	D7	W			rst_noverlap[1:0]		goa_rst_width1[3:0]				04
		W	goa_rst_width2[7:0]								03
RSTCTRL7	D8	W							goa_rst_tchop1[8]	goa_rst_tchop2[8]	00
		W	goa_rst_tchop1[7:0]								56
		W	goa_rst_tchop2[7:0]								00
RSTCTRL8	D9	W							goa_rst_tglue1[8]	goa_rst_tglue2[8]	00
		W	goa_rst_tglue1[7:0]								2B
		W	goa_rst_tglue2[7:0]								7F
RDID1	DA	R	sys_id1[7:0]								30
RDID2	DB	R	sys_id2[7:0]								07
RDID3	DC	R	sys_id3[7:0]								01
WRID1	DD	W	sys_id1[7:0]								30
WRID2	DE	W	sys_id2[7:0]								07
WRID3	DF	W	sys_id3[7:0]								01
SOUCTRL1	E0	W	ld_start[8]	ld_end[8]	srcpop_en_start[8]	srcpop_en_end[8]	srcnop_en_start[8]	srcnop_en_end[8]	fr_prec_start[8]	fr_prec_end[8]	00
SOUCTRL2	E1	Multi-W	ld_start[7:0]								03
							sd_bias_adj[3:0]				0A
SOUCTRL3	E2	W	ld_end[7:0]								04
SOUCTRL4	E3	W	srcpop_en_start[7:0]								01
SOUCTRL5	E4	W	srcpop_en_end[7:0]								14
SOUCTRL6	E5	W	srcnop_en_start[7:0]								01
SOUCTRL7	E6	W	srcnop_en_end[7:0]								19
SOUCTRL8	E7	W	fr_prec_start[7:0]								16
SOUCTRL9	E8	W	fr_prec_end[7:0]								29
SOUCTRL10	E9	W	pol_ctrl	pol_init	ofc_ctrl	ofc_init	odd_even_ctrl	fr_sd_en_start[8]	fr_sd_en_end[8]	pol_ctrl2	20
SOUCTRL11	EA	W	fr_sd_en_start[7:0]								2B
SOUCTRL12	EB	W	fr_sd_en_end[7:0]								C1
SOUCTRL13	EC	W	pol_switch[8]	be_prec_sta	be_prec_end[	chopper_sel[2:0]			be_sd_en	be_sd_en_e	00

Name	ADDR (Hex)	Access	D7	D6	D5	D4	D3	D2	D1	D0	Def (Hex)
				rt[8]	8]				_start[8]	nd[8]	
SOUCTRL14	ED	W	be_prec_start[7:0]								07
SOUCTRL15	EE	W	be_prec_end[7:0]								1B
SOUCTRL16	EF	W	be_sd_en_start[7:0]								1D
SOUCTRL17	F0	W	be_sd_en_end[7:0]								C1
SOUCTRL18	F1	W	pol_switch[7:0]								14
SOUCTRL19	F2	Multi-W		sd_n_en_option	source_precharge_disable		ofc_phase_syc	usr_rev	normal_black	pts	68
			fr_sd_n_en_start[7:0]								1B
			be_sd_n_en_start[7:0]								0B
			fr_sd_n_en_start[8]	be_sd_n_en_start[8]	precharge_gray[5:0]						20
CPTEST1	F4	W								clear_cmd	00
CPTEST2	F5	Multi-W			clear_dat_r[5:0]						00
					clear_dat_g[5:0]						00
					clear_dat_b[5:0]						00
FSMCTRL	F9	W			clear_2frame_disable	1		poff_xon_disable	disp_blk_lvd_en	wait_disp_disable	12
PADCTRL	FB	W	atest_en	osc_test_oe							00
RDSTATE	FC	R						cur_state[2:0]			/
RD_PWR_STATUS	FD	Multi-R					gam_en	vref_en	vdds_en	gam_ref_en	/
							vgl_en	vgh_en	ddvdl_en	ddvdh_en	/

6.2. Description of Public Registers Command

6.2.1. No operation(00h)

Command Set		NOP								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								00h
Description	This command is an empty command.									
Restriction	-									

6.2.2. Read display ID(04h)

Command Set		RDDIDIF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	sys_id1[7:0]								30h
2nd Parameter		sys_id2[7:0]								07h
3rd Parameter		sys_id3[7:0]								01h
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.									
Restriction	-									

6.2.3. Read display status (09h)

Command Set		RDDST								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	pump_en	sys_my	sys_mx	sys_mv	sys_ml	sys_bgr			/
2nd Parameter			dbi[2:0]			color8_en	ptl_on	slpout	normal_on	/
3rd Parameter		scroll_on		inv_on	gs	ss	disp_en	te_on		/
4th Parameter				telom						/
Description	pump_en: Booster Voltage Status. "0"= Booster Off; "1"=Booster On; sys_my: Page Address Order. "0"= Top to Bottom (When memory data access control D7 = '0'); "1"= Bottom to Top (When memory data access control D7 = '1'); sys_mx: Column Address Order. "0"= Left to Right (When memory data access control D6 = '0'); "1"= Right to Left (When memory data access control D6 = '1'); sys_mv: Page/Column Order "0"= Normal Mode (When memory data access control D5 = '0') "1"= Reverse Mode (When memory data access control D5 = '1') sys_ml: Line Address Order "0"= LCD Refresh Top to Bottom (When memory data access control D4 = '0') "1"= LCD Refresh Bottom to Top (When memory data access control D4 = '1') sys_bgr: RGB/BGR Order "0"= RGB (When memory data access control D3 = '0') "1"= BGR (When memory data access control D3 = '1') dbi[2:0]: Interface color pixel format definition "101" = 16 Bit/Pixel(RGB 565) "110" = 18 Bit/Pixel(RGB 666) color8_en: Idle Mode On/Off "0"= Idle Mode Off "1"= Idle Mode On ptl_on: Partial Mode On/Off "0" = Partial Mode Off "1"= Partial Mode On slpout: Sleep In/Out "0"= Sleep In Mode "1"= Sleep Out Mode									

	normal_on: Display Normal Mode On/Off “0”= Display Normal Mode Off “1”= Display Normal Mode On scroll_on: Vertical Scrolling Status “0”= Vertical Scrolling is Off “1”= Display Normal Mode On inv_on: Inversion Status “0”= Inversion is Off “1”= Inversion is On gs: Gate scan direction “0”= Gate scan direction is 1→856 “1”= Gate scan direction is 856→1 ss: selects the shift direction of outputs of the source driver “0”= Source output S252→S1 “1”= Source output S1→S252 disp_en: Display On/Off “0”= Display is Off “1”= Display is On te_on: Tearing Effect Line On/Off “0”= Tearing Effect Line Off “1”= Tearing Effect Line On telom: Tearing Effect Output Line Mode “0”= Mode 1, V-Blanking only “1”= Mode 2, both H-Blanking and V-blanking
Restriction	-

6.2.4. Sleep In(10h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">SLPIN</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">No Parameter</td><td>/</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the LCD module to enter the minimum power consumption mode.
In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.
The interface and memory are still working and the memory keeps it’s contents.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120 msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>SLPIN</td></tr><tr><td>HW Reset</td><td>SLPIN</td></tr></table></td></tr>
</table>

6.2.5. Sleep Out(11h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">SLPOUT</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">No Parameter</td><td>/</td></tr>
<tr><td>Description</td><td colspan="10">This command turns off sleep mode.
In this mode e.g. the DC/DC converter is enabled. Internal oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep in Command (10h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the clock circuits to stabilize.
It will be necessary to wait 120msec after sending sleep out command (when in sleep in mode) before sending an sleep in command.
The display module runs the self-diagnostic functions after this command is received.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>SLPIN</td></tr><tr><td>HW Reset</td><td>SLPIN</td></tr></table></td></tr>
</table>

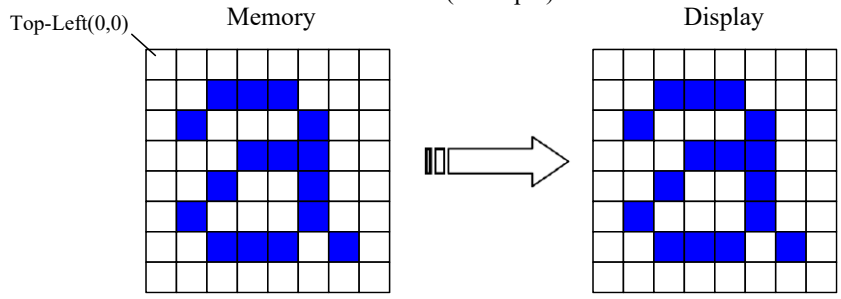
6.2.6. Partial mode on(12h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">PARMON</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">No Parameter</td><td>/</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on partial mode.The partial mode is described by the Partial Area command (30h).
To leave Partial mode, the Normal Display On command (13h) should be written.
Note: If a command is written in a frame cycle,the command becomes effective from the next frame.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect during Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode on, Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value(D7 to D0)</th></tr><tr><td>Power On Sequence</td><td>Normal Display On</td></tr><tr><td>HW Reset</td><td>Normal Display On</td></tr></table></td></tr>
</table>

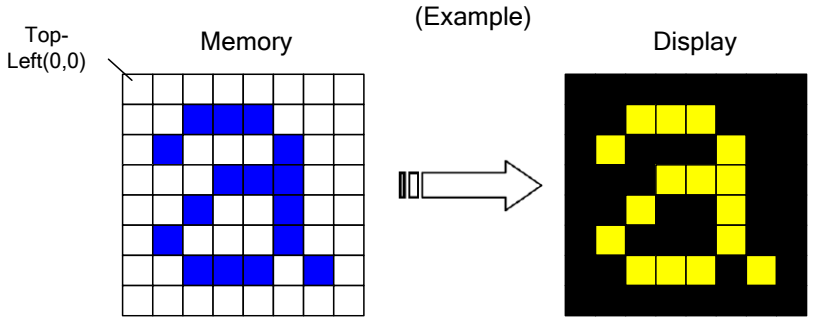
6.2.7. Normal display mode on(13h)

Command Set		NORMON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								/
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode on command (12h)									
Restriction	-									

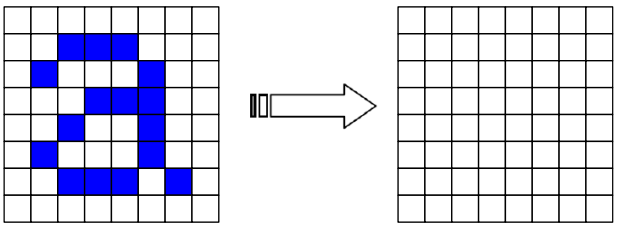
6.2.8. Display inversion off(20h)

Command Set		INVOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								/
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. (Example) Top-Left(0,0) Memory Display 									
Restriction	-									

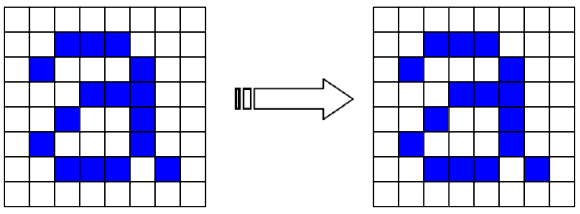
6.2.9. Display inversion on(21h)

Command Set		INVON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								/
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written. 									
Restriction	-									

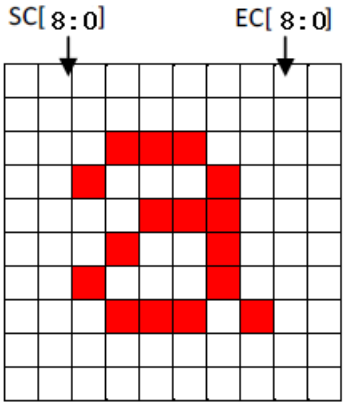
6.2.10. Display off(28h)

Command Set		DISPOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								/
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Memory Display 									
Restriction	-									

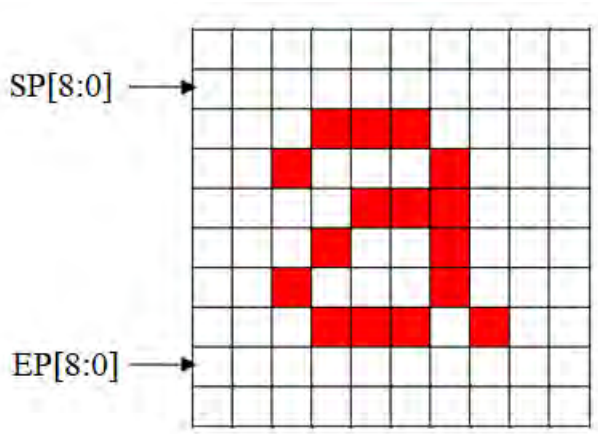
6.2.11. Display on(29h)

Command Set		DISPON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								/
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory Display 									
Restriction	-									

6.2.12. Column address set(2Ah)

Command Set		COLSET								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								sc[8]	00h
2nd Parameter		sc[7:0]								00h
3rd Parameter									ec[8]	00h
4th Parameter		ec[7:0]								EFh
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [8:0] and EC [8:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory. 									
Restriction	-									

6.2.13. Row address set(2Bh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">ROWSET</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td rowspan="4">Multi-W</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>sp[8]</td><td>00h</td></tr>
<tr><td>2nd Parameter</td><td colspan="8">sp[7:0]</td><td>00h</td></tr>
<tr><td>3rd Parameter</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>ep[8]</td><td>00h</td></tr>
<tr><td>4th Parameter</td><td colspan="8">ep[7:0]</td><td>EFh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [8:0] and EP [8:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

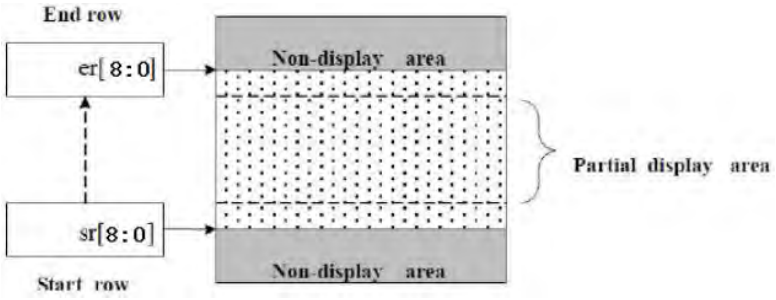
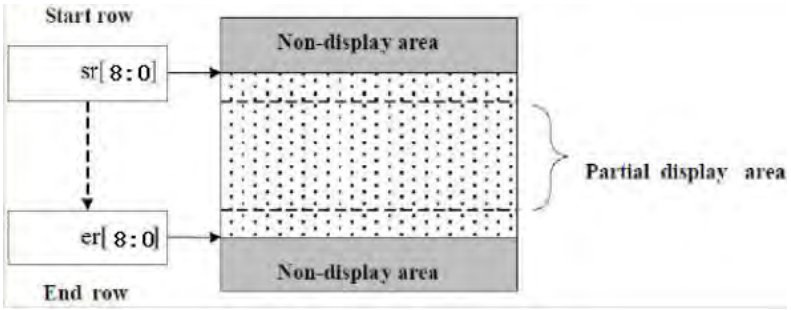
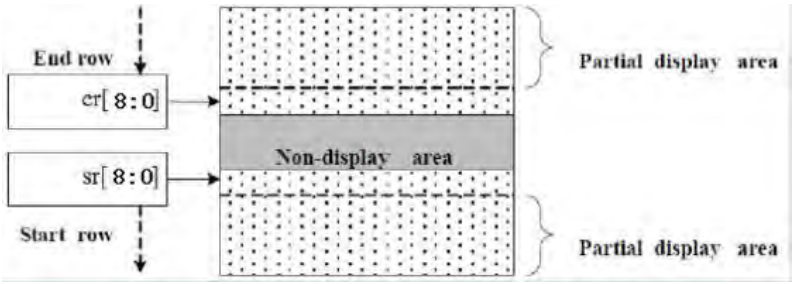
6.2.14. Memory write(2Ch)

Command Set		MEMWR								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No parameter								/
Description	This command is used to transfer data from MPU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start page positions. (The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then 18-bit data is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write.									
Restriction	-									

6.2.15. Memory read(2Eh)

Command Set		MEMRD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read	No Parameter								
Description	This command is used to transfer data from frame memory to MPU. When this command is accepted, the column register and the page register are reset to the Start Column/Start page positions. Frame Read can be cancelled by sending any other command.									
Restriction	-									

6.2.16. Partial area(30h)

Command Set		PAREA								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								sr[8]	00h
2nd Parameter		sr[7:0]								00h
3rd Parameter									er[8]	00h
4th Parameter		er[7:0]								EFh
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (sr[8:0]) and the second the End Row (er[8:0]), as illustrated in the figures below. sr[8:0] and er[8:0] refer to the Frame Memory row address counter. If End Row > Start Row, when MADCTL ml='1'.  If End Row > Start Row, when MADCTL ml='0'.  If End Row < Start Row, when MADCTL ml='0'.  									
Restriction	-									

6.2.17. Vertical scrolling definition(33h)

Command Set		VSDEF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								tfa[8]	00h
2nd Parameter		tfa[7:0]								00h
3rd Parameter									vsa[8]	00h
4th Parameter		vsa[7:0]								F0h
5th Parameter									bfa[8]	00h
6th Parameter		bfa[7:0]								00h

Description

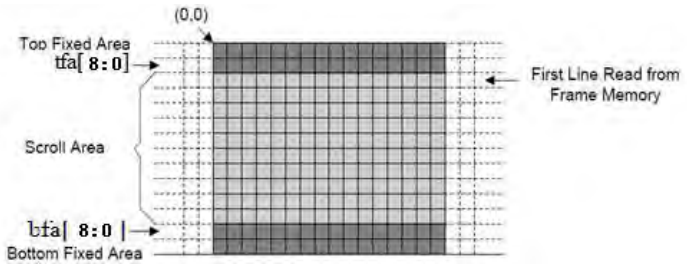
This command defines the Vertical Scrolling Area of the display.

When MADCTL ml = '0'

The 1st&2nd parameter tfa[8:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd&4th parameter vsa[8:0] describes the height of the Vertical Scrolling Area(in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th& 6th parameter bfa[8:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). tfa[8:0], vsa[8:0] and bfa[8:0] refer to the Frame Memory Line Pointer.



When MADCTL ml = '1'

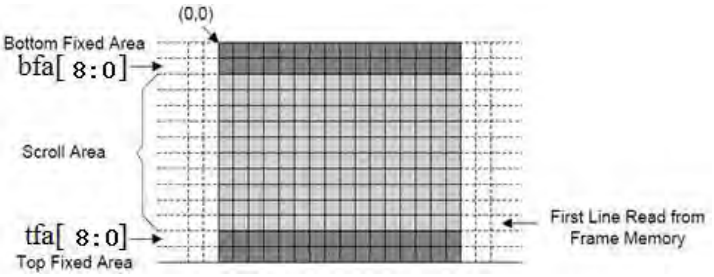
The 1st&2nd parameter tfa[8:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd&4th parameter vsa[8:0] describes the height of the Vertical Scrolling Area(in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start

Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th&6th parameter bfa[8:0] describes the Bottom Fixed Area (in No. of lines

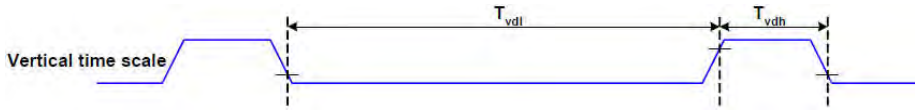
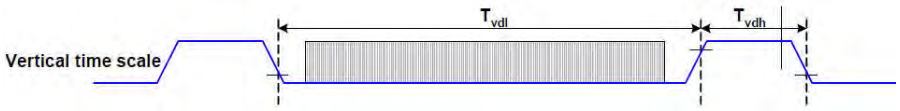
from Top of the Frame Memory and Display).

	
Restriction	-

6.2.18. Te off(34h)

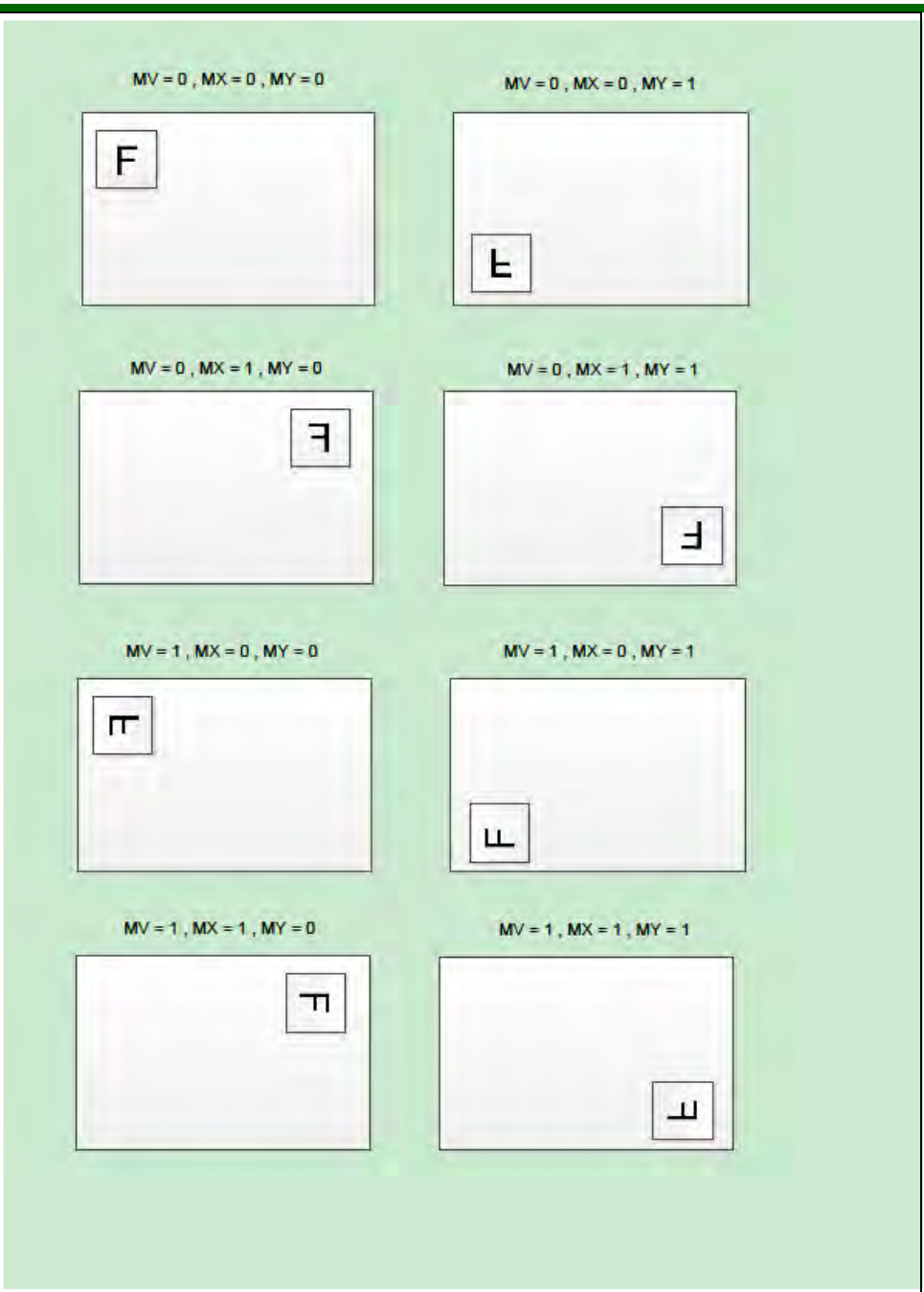
Command Set		TEOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No Parameter								/
Description	This command is used to turn off (Active Low) the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when tearing effect output is already off.									

6.2.19. Te on(35h)

Command Set		TEON								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write								telom	00h
Description	This command is used to turn on the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ml. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. When telom =’0’: The Tearing Effect output line consists of V-Blanking information only:  When telom =’1’: The Tearing Effect output Line consists of both V-Blanking and H-Blanking information:  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.									
Restriction	This command has no effect when tearing effect output is already on.									

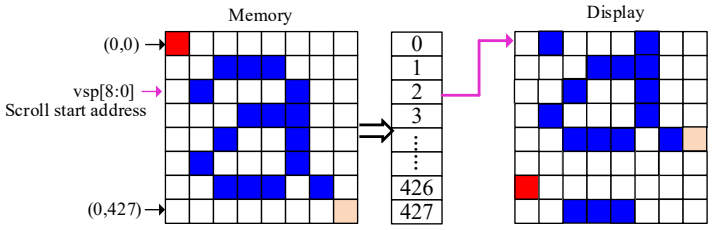
6.2.20. Memory access control(36h)

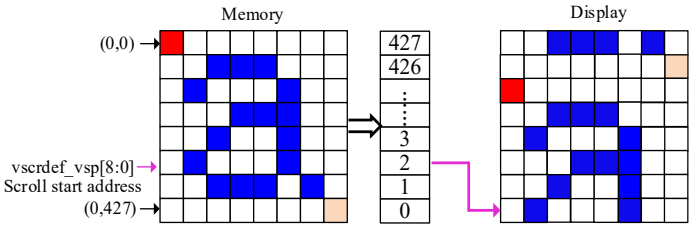
<table>
<tr><th colspan="2">Command Set</th><th colspan="9">MADCTRL</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td>sys_my</td><td>sys_mx</td><td>sys_mv</td><td>sys_ml</td><td>sys_bgr</td><td>sys_mh</td><td></td><td></td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command defines read/write scanning direction of frame memory.
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>D7</td><td>sys_my</td><td>Page Address Order</td></tr>
<tr><td>D6</td><td>sys_mx</td><td>Column Address Order</td></tr>
<tr><td>D5</td><td>sys_mv</td><td>Page/Column Order</td></tr>
<tr><td>D4</td><td>sys_ml</td><td>Line Address Order</td></tr>
<tr><td>D3</td><td>sys_bgr</td><td>RGB/BGR Order</td></tr>
<tr><td>D2</td><td>sys_mh</td><td>Column Address Scan Order</td></tr>
</table>
-Bit Assignment
Bit D7- Page Address Order
“0” = Top to Bottom (When MADCTL D7=”0”).
“1” = Bottom to Top (When MADCTL D7=”1”).
Bit D6- Column Address Order
“0” = Left to Right (When MADCTL D6=”0”).
“1” = Right to Left (When MADCTL D6=”1”).
Bit D5- Page/Column Order
“0” = Normal Mode (When MADCTL D5=”0”).
“1” = Reverse Mode (When MADCTL D5=”1”)
Bit D4- Line Address Order
“0” = LCD Refresh Top to Bottom (When MADCTL D4=”0”)
“1” = LCD Refresh Bottom to Top (When MADCTL D4=”1”)
Bit D3- RGB/BGR Order
“0” = RGB (When MADCTL D3=”0”)
“1” = BGR (When MADCTL D3=”1”)
Bit D2- Column Address Scan Order
“0” = LCD Refresh Left to Right (When MADCTL D2=”0”)
“1” = LCD Refresh Right to Left (When MADCTL D2=”1”)</td></tr>
</table>



Restriction	-

6.2.21. Vertical scrolling start address(37h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">VSSAD</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>1st Parameter</td><td rowspan="2">Multi-W</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>vsp[8]</td><td>00h</td></tr>
<tr><td>2nd Parameter</td><td colspan="8">vsp[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used together with Vertical scrolling (33h).
These two commands describe the scrolling area and the scrolling mode.
The Vertical scrolling start address command has one parameter which describes which line in the Frame Memory will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
When ml='0'
Example:When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 428 and vsp = '2'.
 

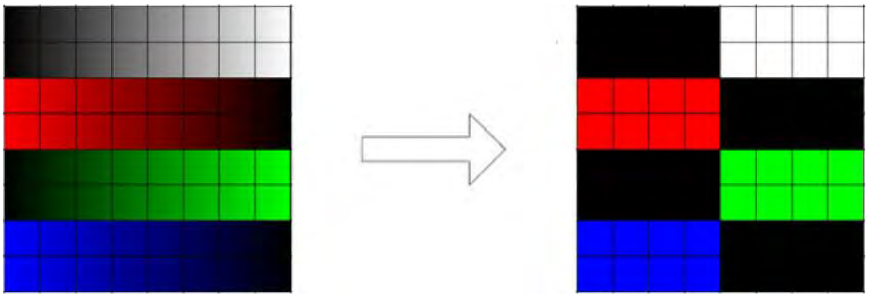
When ml='1'
Example:When Top Fixed Area = Bottom Fixed Area = 00, vertical scrolling area = 428 and vsp = '2'.
 

Note: When new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect.
vsp refers to the Frame Memory line pointer.</td></tr>
<tr><td>Restriction</td><td colspan="10">Since the value of the vertical scrolling start address is absolute (with reference to the frame memory), it must not enter the fixed area (defined by vertical scrolling (33h)- otherwise undesirable image will be displayed on the panel).</td></tr>
</table>

6.3.22. Idle mode off(38h)

Command Set		IDLEOFF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No parameter								/
Description	This command is used to recover from idle mode on. In the idle off mode 1. LCD can display 65k or 262k colors. 2. Normal frame frequency is applied.									
Restriction	This command has no effect when module is already in idle off mode.									

6.2.23. Idle mode on(39h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">IDLEON</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">No parameter</td><td>/</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into idle mode on.
There will be no abnormal visible effect on the display mode change transition.
In the idle on mode,
1. Color expression is reduced. The colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.
2. 8-Color mode frame frequency is applied.
3. Exit from idle mode on by idle mode off (38h) command.
Memory Pannel Display
 
<table>
<tr><td>Color</td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B4 B1 B0</td></tr>
<tr><td>Black</td><td>0xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr>
<tr><td>Blue</td><td>0xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr>
<tr><td>Red</td><td>1xxxxx</td><td>0xxxxx</td><td>0xxxxx</td></tr>
<tr><td>Magenta</td><td>1xxxxx</td><td>0xxxxx</td><td>1xxxxx</td></tr>
<tr><td>Green</td><td>0xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr>
<tr><td>Cyan</td><td>0xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr>
<tr><td>Yellow</td><td>1xxxxx</td><td>1xxxxx</td><td>0xxxxx</td></tr>
<tr><td>White</td><td>1xxxxx</td><td>1xxxxx</td><td>1xxxxx</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in idle on mode.</td></tr>
</table>

6.2.24. Pixel format set(3Ah)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">PFSET</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">dbi[2:0]</td><td>06h</td></tr>
<tr><td>Description</td><td colspan="10">dbi[2:0] is the pixel format of system interface.
<table>
<tr><th>dbi[2]</th><th>dbi[1]</th><th>dbi[0]</th><th>system interface format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits/pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits/pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
</table>

6.2.25. Write memory continue(3Ch)

Command Set		WRMEMC								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	No parameter								/
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write memory continue or memory write command. If mv= '0': Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the end column (caset_ec) value. The column register is then reset to caset_sc and the page register is incremented. Pixels are written to the frame memory until the page register equals the end page (paset_ep) value and the column register equals the caset_ec value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored. If mv= '1': Data is written continuing from the pixel location after the write range of the previous memory write or write memory continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the end page (paset_ep) value. The page register is then reset to paset_sp and the column register is incremented. Pixels are written to the frame memory until the column register equals the end column (caset_ec) value and the page register equals the paset_ep value, or the host processor sends another command. If the number of pixels exceeds (caset_ec-caset_sc+1)*(paset_ep-paset_sp+1) the extra pixels are ignored.									
Restriction	A memory write should follow a column address set or page address set to define the write address. Otherwise, data written with write memory continue is written to undefined addresses.									

6.2.26. Horizontal scrolling definition(3Dh)

Command Set		HSDEF								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								lfa[8]	00h
2nd Parameter		lfa[7:0]								00h
3rd Parameter									hsa[8]	00h
4th Parameter		hsa[7:0]								F0h
5th Parameter									rfa[8]	00h
6th Parameter		rfa[7:0]								00h

Description

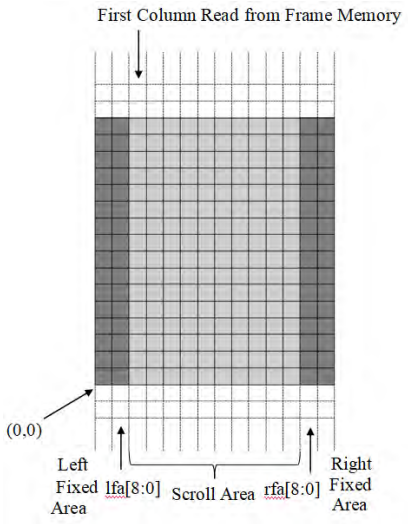
This command defines the Horizontal Scrolling Area of the display.

When MADCTL mh = '0'

The 1st&2nd parameter lfa[8:0] describes the Left Fixed Area (in No. of columns from left of the Frame Memory and Display).

The 3rd&4th parameter hsa[8:0] describes the width of the Horizontal Scrolling Area(in No. of columns of the Frame Memory [not the display] from the Horizontal Scrolling Start Address). The first column read from Frame Memory appears immediately after the right most column of the Left Fixed Area.

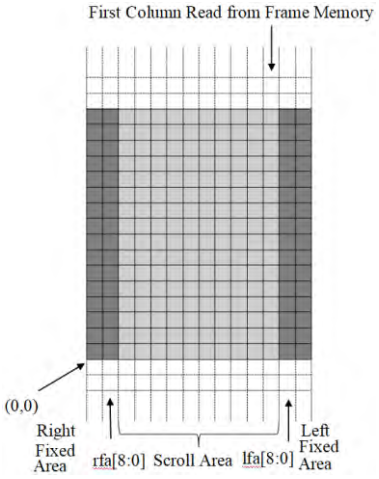
The 5th& 6th parameter rfa[8:0] describes the Right Fixed Area (in No. of columns from Right of the Frame Memory and Display). lfa[8:0], hsa[8:0] and rfa[8:0] refer to the Frame Memory Column Pointer.



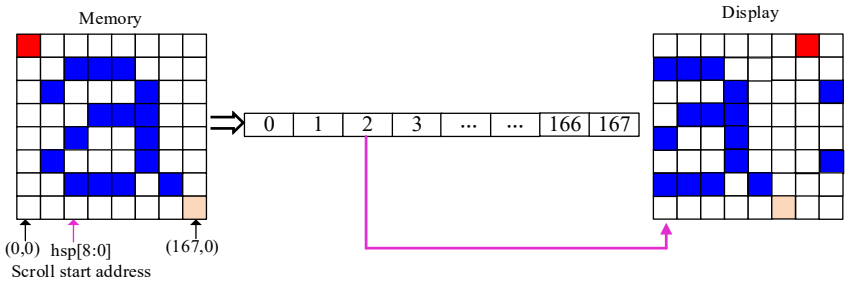
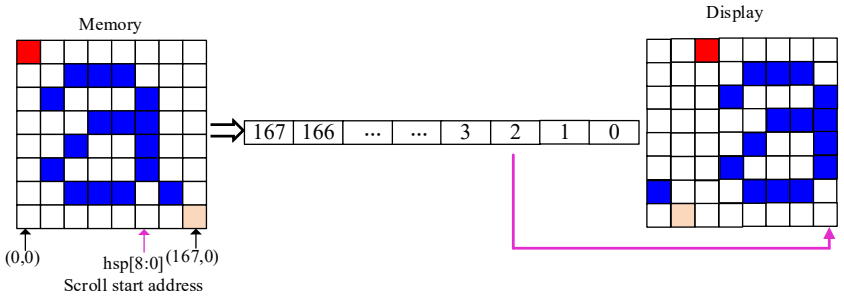
When MADCTL mh = '1'

The 1st&2nd parameter lfa[8:0] describes the Left Fixed Area (in No. of columns from right of the Frame Memory and Display).

The 3rd&4th parameter hsa[8:0] describes the width of the Horizontal Scrolling Area(in

	No. of columns of the Frame Memory [not the display] from the Horizontal Scrolling Start Address). The first column read from Frame Memory appears immediately after the right most line of the Left Fixed Area. The 5th&6th parameter rfa[8:0] describes the Right Fixed Area (in No. of columns from Left of the Frame Memory and Display). 
Restriction	-

6.2.27. Horizontal scrolling start address(3Eh)

Command Set		HSSAD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								hsp[8]	00h
2nd Parameter		hsp[7:0]								00h
Description	This command is used together with Horizontal scrolling (3Dh). These two commands describe the scrolling area and the scrolling mode. The Horizontal Scrolling Start Address command has one parameter which describes which column in the Frame Memory will be written as the first column after the last column of the Left Fixed Area on the display as illustrated below: When ml='0' Example:When Left Fixed Area = Right Fixed Area = 00, horizontal scrolling area = 168 and hsp = '2'.  When ml='1' Example:When Left Fixed Area = Right Fixed Area = 00, horizontal scrolling area = 168 and hsp = '2'.  Note: When new pointer position and picture data are sent, the result on the display will happen at the next panel scan to avoid tearing effect. hsp refers to the Frame Memory column pointer.									
Restriction	-									

6.3. Description of Private Registers Command 1

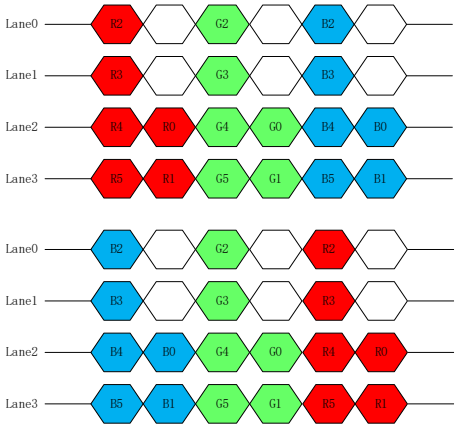
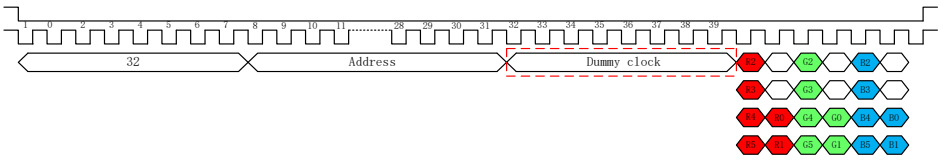
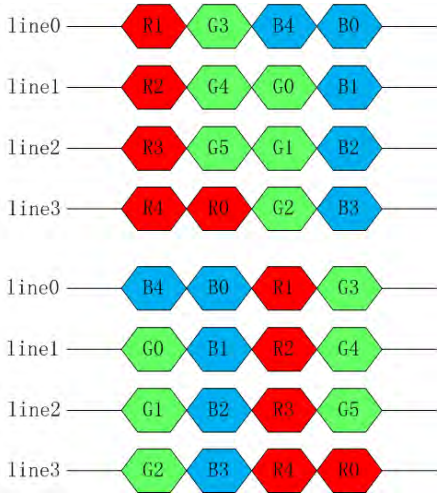
6.3.1. Interface control 1(40h)

Command Set		IFCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write				sdo_hiz					00h
Description	sdo_hiz : SDO enable signal. “0” =disable “1” =enable									
Restriction	Should set “FF=A5” before configure this registers									

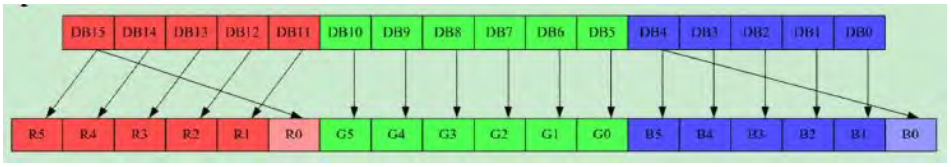
6.3.2. Interface control 2(41h)

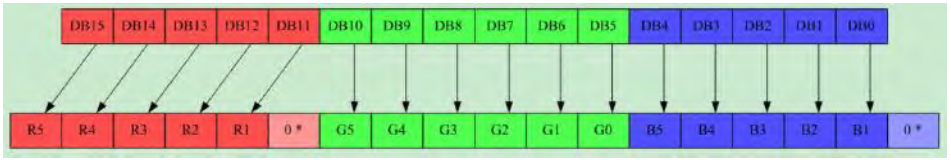
Command Set		IFCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write								spi_2dat_en	00h
Description	spi_2dat_en : spi 2-data line mode enable signal. “0” =disable “1” =enable									
Restriction	Should set “FF=A5” before configure this registers									

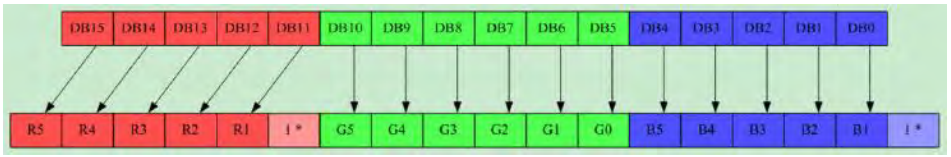
6.3.3. Interface control 3(42h)

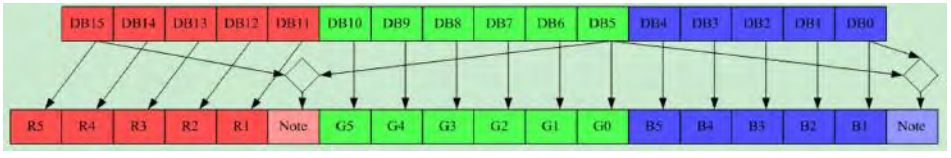
Command Set		IFCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write				qspi_bgr			qspi_dummy	qspi_sbyte	00h
Description	When interface is QSPI: qspi_bgr : when op code = 8'h12 or 8'h32, and dbi(3AH) = 3'b110, this signal can change the order in which the sub-pixels are received.  qspi_dummy : When op code = 8'h32,this signal determines whether there are 8 dummy clocks.  qspi_sbyte : When op code = 8'h12 or 8'h32, and dbi(3AH) = 3'b101,this signal can change the order of the received bytes.  									
Restriction	Should set "FF=A5" before configure this registers									

6.3.4. Interface control 4(43h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">IFCTRL4</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td></td><td></td><td>endian</td><td colspan="2">epf[1:0]</td><td colspan="2">mdt[1:0]</td><td>04h</td></tr>
<tr><td>Description</td><td colspan="10">endian : When dbi(3AH) = 3’b101, this signal can change the order of the received bytes.
epf :
epf = 00
 

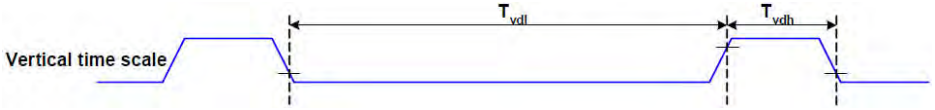
epf = 01
 

Note: Exception
1. R0 = 1 when R5~R1 = 1111
2. B0 = 1 when B4~B1 = 1111
epf = 10
 

Note: Exception
1. R0 = 0 when R5~R1 = 0000
2. B0 = 0 when B4~B1 = 0000
epf = 11
 

Note:
1. If DB15~DB11 = DB10~DB6, R0 = DB5, else R0 = DB15
2. If DB4~DB0 = DB10~DB16, B0 = DB5, else B0 = DB0
mdt : When interface is Dual-SPI Interface, and dbi(3AH) = 3’b110, this signal select the method of display data transferring.</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.3.5. Tearing effect control 1(44h)

Command Set		TECTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W						sts[10:8]			00h
2nd Parameter		sts[7:0]								00h
Description	This command turns on the display module's tearing effect output signal on the TE signal line when the display module reaches line sts. The TE signal is not affected by changing mv. The tearing effect line on has one parameter that describes the tearing effect output line mode. The tearing effect output line consist of V-blanking information only.  Note: That set tear scanline with sts = '0' is equivalent to tearing effect line on with telom= '0'. The tearing effect output line shall be low when the display module is in sleep mode.									
Restriction	This command takes effect on the frame following the current frame.Therefore, if the tear effect (TE) output is already on, the TE output shall continue to operate as programmed by the previous tearing effect line on or set tear scanline command until the end of the frame.									

6.3.6. Tearing effect control 2(45h)

Command Set		TECTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R						sts[10:8]			/
2nd Parameter		sts[7:0]								/
Description	The display module returns the current scanline sts, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.When in sleep in mode, the value returned by get scanline is undefined.									
Restriction	-									

6.3.7. Tearing effect control 3(46h)

Command Set		TECTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write				te_oe			te_pol	te_ext end	00h
Description	te_oe : TE signal output Enable/Disable “0”: Disable “1”: Enable te_pol :This signal can change TE polarity. te_extend :This signal enables the TE signal extension mode, which supports configuring the TE waveform with register values.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.8. Tearing effect control 4(47h)

Command Set		TECTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W						te_v_start[10:8]			00h
2nd Parameter		te_v_start[7:0]								00h
3rd Parameter							te_v_end[10:8]			00h
4th Parameter		te_v_end[7:0]								00h
Description	When the TE extension mode is turned on: te_v_start[10:0] : Specifies on which line of a frame the TE signal begins te_v_end[10:0] : Specify which line of a frame the TE signal is closed.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.9. Tearing effect control 5(48h)

Command Set		TECTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W								te_h_start[8]	00h
2nd Parameter		te_h_start[7:0]								00h
3rd Parameter									te_h_end[8]	00h
4th Parameter		te_h_end[7:0]								00h
Description	When the TE extension mode is turned on, and telom =1'b1: te_h_start[8:0] : Specifies which column of a row the TE signal begins. te_h_end[8:0] : Specifies from which column of a row the TE signal is closed.									
Restriction	Should set "FF=A5" before configure this registers									

6.3.10. Scan direction control(49h)

Command Set		SCANCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write						gs		ss	01h
Description	gs: Gate scan direction gs="0": Gate scan direction is 1→856; gs="1": Gate scan direction is 856→1. ss: selects the shift direction of outputs of the source driver. ss="0": Source output S252→S1; ss="1":Source output S1→S252.									
Restriction	Should set "FF=A5" before configure this registers									

6.3.11. OTP control 1(4Ah)

Command Set		OTPCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write		otp_ptm[1:0]		otp_pwe	otp_prd	otp_pprog	otp_vpp_sel	otp_vpp_src_sel	00h
Description	otp_ptm[1:0] : test mode enable signal. otp_pwe :define program cycle. otp_prd : define read cycle. otp_pprog :program mode enable signal. otp_vpp_sel :select the work voltage (8V~8.5V during program cycle and 1.35V~1.65V in read cycle). otp_vpp_src_sel :The program voltage Source is provided by external or by the chip. "1": Program voltage Generate From Chip. "0": Program voltage Generate From Outside.									
Restriction	Should set "FF=A5" before configure this registers									

6.3.12. OTP control 2(4Bh)

Command Set		OTPCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	otp_pa[7:0]								00h
Description	otp_pa[7:0] : Set the OTP program address.									
Restriction	Should set "FF=A5" before configure this registers									

6.3.13. OTP control 3(4Ch)

Command Set		OTPCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	otp_pdin[7:0]								00h
Description	otp_pdin[7:0] :Specify OTP program data.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.14. OTP control 4(4Dh)

Command Set		OTPCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	otp_rd_dat[7:0]								/
2nd Parameter										/
Description	otp_rd_dat[7:0] : Read OTP output data.									
Restriction	-									

6.3.15. Memory access control(4Fh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">USRMAD</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td>usr_my</td><td>usr_mx</td><td>usr_mv</td><td>usr_ml</td><td>usr_bgr</td><td>usr_mh</td><td></td><td></td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command defines read/write scanning direction of frame memory.
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>D7</td><td>usr_my</td><td>Page Address Order</td></tr>
<tr><td>D6</td><td>usr_mx</td><td>Column Address Order</td></tr>
<tr><td>D5</td><td>usr_mv</td><td>Page/Column Order</td></tr>
<tr><td>D4</td><td>usr_ml</td><td>Line Address Order</td></tr>
<tr><td>D3</td><td>usr_bgr</td><td>RGB/BGR Order</td></tr>
<tr><td>D2</td><td>sys_mh</td><td>Column Address Scan Order</td></tr>
</table>
-Bit Assignment
Bit D7- Page Address Order
“0” = Top to Bottom (When MADCTL D7=”0”).
“1” = Bottom to Top (When MADCTL D7=”1”).
Bit D6- Column Address Order
“0” = Left to Right (When MADCTL D6=”0”).
“1” = Right to Left (When MADCTL D6=”1”).
Bit D5- Page/Column Order
“0” = Normal Mode (When MADCTL D5=”0”).
“1” = Reverse Mode (When MADCTL D5=”1”)
Bit D4- Line Address Order
“0” = LCD Refresh Top to Bottom (When MADCTL D4=”0”)
“1” = LCD Refresh Bottom to Top (When MADCTL D4=”1”)
Bit D3- RGB/BGR Order
“0” = RGB (When MADCTL D3=”0”)
“1” = BGR (When MADCTL D3=”1”)
Bit D2- Column Address Scan Order
“0” = LCD Refresh Left to Right (When MADCTL D2=”0”)
“1” = LCD Refresh Right to Left (When MADCTL D2=”1”)
The function is the same as 36H.</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.3.16. Internal timing control 1(53h)

Command Set		ITCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	inter_vbp[7:0]								0Ch
Description	inter_vbp[7:0] : set internal vertical back-porch width.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.17. Internal timing control 2(54h)

Command Set		ITCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write		inter_vfp[6:0]							08h
Description	inter_vfp[6:0] : set internal vertical front-porch width.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.18. Internal timing control 3(55h)

Command Set		ITCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	inter_hbp[7:0]								25h
Description	inter_hbp[7:0] : set internal horizontal back-porch width.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.19. Internal timing control 4(56h)

Command Set		ITCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	inter_hfp[7:0]								25h
Description	inter_hfp[7:0] : set internal horizontal front-porch width.									
Restriction	Should set “FF=A5” before configure this registers									

6.3.20. Ibias control(57h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">IBIASCTRL</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td></td><td colspan="2">bias_sd_adj[1:0]</td><td colspan="2">bias_gma_adj[1:0]</td><td colspan="2">bias_adj[1:0]</td><td>2Ah</td></tr>
<tr><td>Description</td><td colspan="10">bias_sd_adj[1:0]: bias for source block
bias_gma_adj[1:0] : bias for gamma block.
bias_adj[1:0]: Bias for other analog blocks
<table><tr><th>bias_sd_adj[1:0]
bias_gma_adj[1:0]
bias_adj[1:0]</th><th>Ib(Unit: uA)</th></tr><tr><td>00</td><td>0.50</td></tr><tr><td>01</td><td>0.75</td></tr><tr><td>10</td><td>1.00</td></tr><tr><td>11</td><td>1.25</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.3.21. LVD control(59h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">LVDCTRL</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td>lvd_rec_bypass</td><td>lvd_rec_goa_sel</td><td>lvd_en</td><td></td><td>1</td><td colspan="2">lvd_sel[1:0]</td><td>15h</td></tr>
<tr><td>Description</td><td colspan="10">lvd_rec_bypass:
‘0’: GOA turns on the precharge function when LVD recovers
‘1’: GOA turns off the precharge function when LVD recovers
lvd_rec_goa_sel:
‘0’: GOA precharges to VGL when LVD recovers
‘1’: GOA precharges to GND when LVD recovers
lvd_en: LVD enable signal.
<table><tr><th>lvd_en</th><th>Description</th></tr><tr><td>0</td><td>Disable LVD</td></tr><tr><td>1</td><td>Enable LVD</td></tr></table>
lvd_sel[1:0]: LVD threshold selection signal
<table><tr><th>lvd_sel[1:0]</th><th>LVD threshold(Unit:V)</th></tr><tr><td>00</td><td>2.2</td></tr><tr><td>01</td><td>2.3</td></tr><tr><td>10</td><td>2.4</td></tr><tr><td>11</td><td>2.5</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.3.22. RAMCTRL 1(5Ch)

Command Set		RAMCTRL1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write							mec_restart	mbist_disable	00h
Description	mec_restart :When the memory bist is finished, turn the bist function back on at any time. mbist_disable : bist enable signal									
Restriction	Should set “FF=A5” before configure this registers									

6.3.23. RAMCTRL 2(5Dh)

Command Set		RAMCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write		td1sel_l	td2sel_l	td3sel_l		td1sel_r	td2sel_r	td3sel_r	00h
Description	td1sel_l/td1sel_r: select the delay time of internal pre-charge control signal. td2sel_l/td2sel_r: select the delay time of word line control signal td3sel_l/td3sel_r: select the delay time of internal read enable signal									
Restriction	Should set “FF=A5” before configure this registers									

6.3.24. RDBIST(5Eh)

Command Set		RDBIST								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R	mec_restart	mec_enable	mbist_done	mbist_abort	l_mec_pxl1_hit	l_mec_pxl2_hit	r_mec_pxl1_hit	r_mec_pxl2_hit	/
2nd Parameter						l_mec_pxl1_row[8]	l_mec_pxl2_row[8]	r_mec_pxl1_row[8]	r_mec_pxl2_row[8]	/
3rd Parameter		l_mec_pxl1_row[7:0]								/
4th Parameter			l_mec_pxl1_col[6:0]							/
5th Parameter		l_mec_pxl2_row[7:0]								/
6th Parameter			l_mec_pxl2_col[6:0]							/
7th Parameter		r_mec_pxl1_row[7:0]								/
8th Parameter			r_mec_pxl1_col[6:0]							/
9th Parameter		r_mec_pxl2_row[7:0]								/
10th Parameter			r_mec_pxl2_col[6:0]							/
Description	This read address returns memory bist result information : mec_restart :When the memory bist is finished, turn the bist function back on at any time. mec_enable :Memory bist enable signal. mbist_done :Memory bist finished flag. mbist_abort :A signal indicating that RAM has three or more bad spots. l_mec_pxl1_hit :The signal indicating the first bad point on the left side of RAM. l_mec_pxl2_hit :A signal indicating the second bad point on the left side of RAM. r_mec_pxl1_hit :A signal indicating the first bad spot on the right side of RAM. r_mec_pxl2_hit :A signal indicating the second bad spot on the right side of RAM. l_mec_pxl1_row[8:0] : The row where the first bad spot is on the left side of RAM. l_mec_pxl1_col[6:0] : The column where the first bad spot is on the left side of RAM. l_mec_pxl2_row[8:0] : The row where the second bad spot is on the left side of RAM. l_mec_pxl2_col[6:0] : The column where the second bad spot is on the left side of RAM. r_mec_pxl1_row[8:0] : The row where the first bad spot is on the right side of RAM. r_mec_pxl1_col[6:0] : The column where the first bad spot is on the right side of RAM. r_mec_pxl2_row[8:0] : The row where the second bad spot is on the right side of RAM. r_mec_pxl2_col[6:0] : The column where the second bad spot is on the right side of RAM.									
Restriction	-									

6.4. Description of Private Registers Command 2

6.4.1. Gamma control(60~7Fh)

Command Set		GAMCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
60h	Write					vrp0[3:0]				00h
61h	Write			vrp1[5:0]						06h
62h	Write			vrp2[5:0]						0ch
63h	Write				vrp4[4:0]					0bh
64h	Write				vrp6[4:0]					0ah
65h	Write					vrp13[3:0]				06h
66h	Write		vrp20[6:0]							30h
67h	Write		vrp27[2:0]				vrp36[2:0]			43h
68h	Write		vrp43[6:0]							44h
69h	Write					vrp50[3:0]				08h
6Ah	Write				vrp57[4:0]					12h
6Bh	Write				vrp59[4:0]					14h
6Ch	Write			vrp61[5:0]						29h
6Dh	Write			vrp62[5:0]						31h
6Eh	Write					vrp63[3:0]				0fh
6Fh	Write			vj0p63[1:0]				vj1p63[1:0]		00h
70h	Write					vrn0[3:0]				00h
71h	Write			vrn1[5:0]						06h
72h	Write			vrn2[5:0]						0ch
73h	Write				vrn4[4:0]					0ah
74h	Write				vrn6[4:0]					09h
75h	Write					vrn13[3:0]				07h
76h	Write		vrn20[6:0]							30h
77h	Write		vrn27[2:0]				vrn36[2:0]			34h
78h	Write		vrn43[6:0]							44h
79h	Write					vrn50[3:0]				08h

7Ah	Write				vrn57[4:0]				13h
7Bh	Write				vrn59[4:0]				13h
7Ch	Write			vrn61[5:0]					29h
7Dh	Write			vrn62[5:0]					31h
7Eh	Write					vrn63[3:0]			0fh
7Fh	Write			vj0n63[1:0]				vj1n63[1:0]	00h
Description	Gamma register trimming								
Restriction	Should set “FF=A5” before configure this registers								

6.4.2. Regulator control(80~81h)

<table>
<tr><th colspan="2">Command Set</th><th colspan="8">RGLRCTRL</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td rowspan="2">80h</td><td rowspan="2">Multi-W</td><td colspan="8"></td><td>00</td></tr>
<tr><td colspan="4">gma_bias_adj[3:0]</td><td></td><td colspan="3">dvdd_adj[2:0]</td><td>a0h</td></tr>
<tr><td>81h</td><td>Write</td><td colspan="4">bgr_adj[3:0]</td><td colspan="4">vref_adj[3:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">
gma_bias_adj[3:0]： Gamma OP bias adjustment signal
gma_bias_adj[3:2]: GammaP OP bias adjustment
gma_bias_adj[1:0]: GammaN OP bias adjustment
<table>
<tr><th>gma_bias_adj[3:2]
gma_bias_adj[1:0]</th><th>Ib(Unit: uA)</th></tr>
<tr><td>00</td><td>0.50</td></tr>
<tr><td>01</td><td>0.67</td></tr>
<tr><td>10</td><td>1.00</td></tr>
<tr><td>11</td><td>2.00</td></tr>
</table>
dvdd_adj[2:0]: dvdd trimming signal
<table>
<tr><th>dvdd_adj[2:0]</th><th>DVDD (unit:V)</th><th>dvdd_adj[2:0]</th><th>DVDD (unit:V)</th></tr>
<tr><td>000</td><td>1.55</td><td>100</td><td>1.60</td></tr>
<tr><td>001</td><td>1.50</td><td>101</td><td>1.65</td></tr>
<tr><td>010</td><td>1.45</td><td>110</td><td>1.70</td></tr>
<tr><td>011</td><td>1.40</td><td>111</td><td>1.76</td></tr>
</table>
bgr_adj[3:0]: bandgap trimming
<table>
<tr><th>bgr_adj[3:0]</th><th>VBG(V)</th><th>bgr_adj[3:0]</th><th>VBG(V)</th></tr>
<tr><td>0000</td><td>1.300</td><td>1000</td><td>1.288</td></tr>
<tr><td>0001</td><td>1.311</td><td>1001</td><td>1.276</td></tr>
<tr><td>0010</td><td>1.323</td><td>1010</td><td>1.265</td></tr>
<tr><td>0011</td><td>1.334</td><td>1011</td><td>1.253</td></tr>
<tr><td>0100</td><td>1.346</td><td>1100</td><td>1.241</td></tr>
<tr><td>0101</td><td>1.357</td><td>1101</td><td>1.230</td></tr>
<tr><td>0110</td><td>1.369</td><td>1110</td><td>1.218</td></tr>
<tr><td>0111</td><td>1.380</td><td>1111</td><td>1.207</td></tr>
</table>
vref_adj[3:0]: vref trimming
<table>
<tr><th>vref_adj[3:0]</th><th>VREF (unit:V)</th><th>vref_adj[3:0]</th><th>VREF (unit:V)</th></tr>
<tr><td>0000</td><td>2.00</td><td>1000</td><td>2.03</td></tr>
<tr><td>0001</td><td>1.98</td><td>1001</td><td>2.05</td></tr>
<tr><td>0010</td><td>1.96</td><td>1010</td><td>2.07</td></tr>
<tr><td>0011</td><td>1.94</td><td>1011</td><td>2.09</td></tr>
<tr><td>0100</td><td>1.92</td><td>1100</td><td>2.11</td></tr>
<tr><td>0101</td><td>1.90</td><td>1101</td><td>2.13</td></tr>
<tr><td>0110</td><td>1.88</td><td>1110</td><td>2.15</td></tr>
<tr><td>0111</td><td>1.82</td><td>1111</td><td>2.19</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.4.3. VDDS control(82h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">VDDSCTRL</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">vdds_trim[2:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">vdds_trim[2:0]: vdds trimming signal
<table>
<tr><th>vdds_adj[2:0]</th><th>VDDS(unit:V)</th><th>vdds_adj[2:0]</th><th>VDDS (unit:V)</th></tr>
<tr><td>000</td><td>1.824</td><td>100</td><td>1.980</td></tr>
<tr><td>001</td><td>1.691</td><td>101</td><td>2.166</td></tr>
<tr><td>010</td><td>1.576</td><td>110</td><td>2.389</td></tr>
<tr><td>011</td><td>1.475</td><td>111</td><td>2.629</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.4.4. Gamma ldo control 1(83h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">GLDOCTRL1</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">gvcl_reg[7:0]</td><td>56h</td></tr>
<tr><td>Description</td><td colspan="10">gvcl_reg[7:0]:GVCL LDO output voltage level adjustment
<table><tr><td>gvcl_reg[7:0]</td><td>Value(V)</td></tr><tr><td>0011 1111</td><td>-4.20</td></tr><tr><td>…</td><td>-12.5mV/Step</td></tr><tr><td>0101 0110</td><td>-3.91</td></tr><tr><td>…</td><td>-12.5mV/Step</td></tr><tr><td>1111 1111</td><td>-1.8</td></tr></table>
Note:GVCL > DDVDL + 0.2V</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.4.5. Gamma ldo control2(84h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">GLDOCTRL2</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">gvdd_reg[7:0]</td><td>d0h</td></tr>
<tr><td>Description</td><td colspan="10">gvdd_reg[7:0]:GVDD LDO output voltage level adjustment
<table><tr><th>gvdd_reg[7:0]</th><th>Value(V)</th></tr><tr><td>0100 0000</td><td>4.40</td></tr><tr><td>…</td><td>12.5mV/Step</td></tr><tr><td>1101 0000</td><td>6.20</td></tr><tr><td>…</td><td>12.5mV/Step</td></tr><tr><td>1110 0000</td><td>6.40</td></tr></table>
Note: GVDD < DDVDH - 0.2V</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.4.6. Gamma ldo control 3(85h)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">GLDOCTRL3</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td colspan="6">gvsp_reg[6:0]</td><td>3Fh</td></tr>
<tr><td>Description</td><td colspan="10">gvsp_reg[6:0]:GVSP LDO output voltage level adjustment
<table>
<tr><th>gvsp_reg[6:0]</th><th>Value(V)</th></tr>
<tr><td>111 1111</td><td>1.90</td></tr>
<tr><td>…</td><td>12.5mV/Step</td></tr>
<tr><td>011 1111</td><td>1.10</td></tr>
<tr><td>…</td><td>12.5mV/Step</td></tr>
<tr><td>000 0000</td><td>0.31</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.4.7. ESD control 2(8Bh)

Command Set		ESDCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	esd_enable	esd_rd_sram	esd_load_sram	esd_reload_otp	esd_force_analog_1	esd_force_clk_1	esd_force_cs_1	esd_force_dc_1	1fh
Description	esd_enable :ESD function enable signal. esd_rd_sram : Read sram protect bits to test register. esd_load_sram :Enable signal whether to load SRAM information after ESD occurs. esd_reload_otp :Enable signal for whether to reload OTP after ESD occurs. esd_force_analog_1 :Enable signal whether the analog power supply is protected after ESD occurs. esd_force_clk_1 :Enable signal whether to protect the interface clock after ESD occurs. esd_force_cs_1 :Enable signal whether to protect the interface chip selection signal after ESD occurs. esd_force_dc_1 :Enable signal whether to protect interface DCX signal after ESD occurs.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.8. ESD control 3(8Ch)

Command Set		ESDCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read	esd_det[3:0]					esd_occured			/
Description	When this address is read, the flag information is obtained whether or not ESD has occurred: esd_det[3:0] : Whether ESD has occurred in analog circuits. esd_occured :Has ESD occurred in digital circuits.									
Restriction	-									

6.4.9. Gamma Shift(8Dh)

Command Set		GAMShift								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write		vcom_ofc_reg[6:0]							00h
Description	vcom_ofc_reg[6:0]: GVDD = gvdd_reg[7:0] + vcom_ofc_reg [6:0] GVCL = gvcl_reg[7:0] + vcom_ofc_reg [6:0] GVSP = gvsp_reg[6:0] + vcom_ofc_reg [6:0]									
Restriction	Should set “FF=A5” before configure this registers									

6.4.10. RDOTPLD(8Eh)

Command Set		RDOTPLD								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read						por	lvd	otp_loading	/
Description	When you read this address, you get some internal state information: por :Whether POR is occurring. lvd :Whether low voltage is detected. otp_loading :Whether the OTP is loading.									
Restriction	-									

6.4.11. Pump control 1(8Fh)

<table>
<tr><td colspan="2">Command Set</td><td colspan="9">PWRCTRL1</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>1st Parameter</td><td rowspan="2">Multi-W</td><td></td><td colspan="3">vgh_clk_sel[2:0]</td><td></td><td colspan="3">vgl_clk_sel[2:0]</td><td>22h</td></tr>
<tr><td>2nd Parameter</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">mv_clk_sel[2:0]</td><td>04h</td></tr>
<tr><td>Description</td><td colspan="10">
vgh_clk_sel[2:0] : VGH circuit clock selection.
vgl_clk_sel[2:0] : VGL circuit clock selection.
mv_clk_sel[2:0] : MV circuit clock selection.
vgh_clk_sel[2:0] is used to set the operation frequency of VGH pump.
<table>
<tr><th>vgh_clk_sel[2:0]</th><th>Frequency</th></tr>
<tr><td>000</td><td>1/28*OSC</td></tr>
<tr><td>001</td><td>1/16*OSC</td></tr>
<tr><td>010</td><td>1/12*OSC</td></tr>
<tr><td>011</td><td>1/8*OSC</td></tr>
<tr><td>100</td><td>1/6*OSC</td></tr>
<tr><td>101</td><td>1/4*OSC</td></tr>
<tr><td>110</td><td>1/12*OSC</td></tr>
<tr><td>111</td><td>1/12*OSC</td></tr>
</table>
vgl_clk_sel[2:0] is used to set the operation frequency of VGL pump.
<table>
<tr><th>vgl_clk_sel[2:0]</th><th>Frequency</th></tr>
<tr><td>000</td><td>1/28*OSC</td></tr>
<tr><td>001</td><td>1/16*OSC</td></tr>
<tr><td>010</td><td>1/12*OSC</td></tr>
<tr><td>011</td><td>1/8*OSC</td></tr>
<tr><td>100</td><td>1/6*OSC</td></tr>
<tr><td>101</td><td>1/4*OSC</td></tr>
<tr><td>110</td><td>1/12*OSC</td></tr>
<tr><td>111</td><td>1/12*OSC</td></tr>
</table>
mv_clk_sel[2:0] is used to set the operation frequency of MV pump.
<table>
<tr><th>mv_clk_sel[2:0]</th><th>Frequency</th></tr>
<tr><td>000</td><td>1/28*OSC</td></tr>
<tr><td>001</td><td>1/16*OSC</td></tr>
<tr><td>010</td><td>1/12*OSC</td></tr>
<tr><td>011</td><td>1/8*OSC</td></tr>
<tr><td>100</td><td>1/6*OSC</td></tr>
<tr><td>101</td><td>1/4*OSC</td></tr>
<tr><td>110</td><td>1/6*OSC</td></tr>
<tr><td>111</td><td>1/6*OSC</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.4.12. Pump control 2(90h)

Command Set		PWRCTRL2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	ddvdh_drain_row_on[8]	ddvdh_drain_row_off[8]			ddvdh_drain_frm_on[1:0]		ddvdh_drain_frm_off[1:0]		45h
2nd Parameter		ddvdh_drain_row_on[7:0]								C8h
3rd Parameter		ddvdh_drain_row_off[7:0]								2Ch
Description	ddvdh_drain_frm_on[1:0] : Roughly select the frame from which the ddvdh_drain starts. ddvdh_drain_frm_off[1:0] : Roughly select the frame from which the ddvdh_drain ends. ddvdh_drain_row_on[8:0] : Select exactly which row the ddvdh_drain starts. ddvdh_drain_row_off[8:0] : Select exactly which row the ddvdh_drain ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.13. Pump control 3(91h)

Command Set		PWRCTRL3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	ddvdh_en_row_on[8]	ddvdh_en_row_off[8]			ddvdh_en_frm_on[1:0]		ddvdh_en_frm_off[1:0]		81h
2nd Parameter		ddvdh_en_row_on[7:0]								2Ch
3rd Parameter		ddvdh_en_row_off[7:0]								C8h
Description	ddvdh_en_frm_on[1:0] : Roughly select the frame from which the ddvdh_en starts. ddvdh_en_frm_off[1:0] : Roughly select the frame from which the ddvdh_en ends. ddvdh_en_row_on[8:0] : Select exactly which row the ddvdh_en starts. ddvdh_en_row_off[8:0] : Select exactly which row the ddvdh_en ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.14. Pump control 4(92h)

Command Set		PWRCTRL4								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	ddvdl_en_row_on[8]	ddvdl_en_row_off[8]			ddvdl_en_frm_on[1:0]		ddvdl_en_frm_off[1:0]		81h
2nd Parameter		ddvdl_en_row_on[7:0]								2Ch
3rd Parameter		ddvdl_en_row_off[7:0]								C8h
Description	ddvdl_en_frm_on[1:0] : Roughly select the frame from which the ddvdl_en starts. ddvdl_en_frm_off[1:0] : Roughly select the frame from which the ddvdl_en ends. ddvdl_en_row_on[8:0] : Select exactly which row the ddvdl_en starts. ddvdl_en_row_off[8:0] : Select exactly which row the ddvdl_en ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.15. Pump control 5(93h)

Command Set		PWRCTRL5								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	mv_disch_row_on[8]	mv_disch_row_off[8]			mv_disch_frm_on[1:0]		mv_disch_frm_off[1:0]		81h
2nd Parameter		mv_disch_row_on[7:0]								2Dh
3rd Parameter		mv_disch_row_off[7:0]								C7h
Description	mv_disch_frm_on[1:0] : Roughly select the frame from which the mv_disch starts. mv_disch_frm_off[1:0] : Roughly select the frame from which the mv_disch ends. mv_disch_row_on[8:0] : Select exactly which row the mv_disch starts. mv_disch_row_off[8:0] : Select exactly which row the mv_disch ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.16. Pump control 6(94h)

Command Set		PWRCTRL6								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	vgh_en_row_on[8]	vgh_en_row_off[8]			vgh_en_frm_on[1:0]		vgh_en_frm_off[1:0]		44h
2nd Parameter		vgh_en_row_on[7:0]								00h
3rd Parameter		vgh_en_row_off[7:0]								2Ch
Description	vgh_en_frm_on[1:0] : Roughly select the frame from which the vgh_en starts. vgh_en_frm_off[1:0] : Roughly select the frame from which the vgh_en ends. vgh_en_row_on[8:0] : Select exactly which row the vgh_en starts. vgh_en_row_off[8:0] : Select exactly which row the vgh_en ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.17. Pump control 7(95h)

Command Set		PWRCTRL7								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	vgh_disch_row_on[8]	vgh_disch_row_off[8]			vgh_disch_frm_on[1:0]		vgh_disch_frm_off[1:0]		44h
2nd Parameter		vgh_disch_row_on[7:0]								01h
3rdParameter		vgh_disch_row_off[7:0]								8Fh
Description	vgh_disch_frm_on[1:0] : Roughly select the frame from which the vgh_disch starts. vgh_disch_frm_off[1:0] : Roughly select the frame from which the vgh_disch ends. vgh_disch_row_on[8:0] : Select exactly which row the vgh_disch starts. vgh_disch_row_off[8:0] : Select exactly which row the vgh_disch ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.18. Pump control 8(96h)

Command Set		PWRCTRL8								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	vgh_drain_row_on[8]	vgh_drain_row_off[8]			vgh_drain_frm_on[1:0]		vgh_drain_frm_off[1:0]		C0h
2nd Parameter		vgh_drain_row_on[7:0]								2bh
3rd Parameter		vgh_drain_row_off[7:0]								90h
Description	vgh_drain_frm_on[1:0] : Roughly select the frame from which the vgh_drain starts. vgh_drain_frm_off[1:0] : Roughly select the frame from which the vgh_drain ends. vgh_drain_row_on[8:0] : Select exactly which row the vgh_drain starts. vgh_drain_row_off[8:0] : Select exactly which row the vgh_drain ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.19. Pump control 9(97h)

Command Set		PWRCTRL9								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	vgl_en_row_on[8]	vgl_en_row_off[8]			vgl_en_frm_on[1:0]		vgl_en_frm_off[1:0]		81h
2nd Parameter		vgl_en_row_on[7:0]								90h
3rd Parameter		vgl_en_row_off[7:0]								00h
Description	vgl_en_frm_on[1:0] : Roughly select the frame from which the vgh_en starts. vgl_en_frm_off[1:0] : Roughly select the frame from which the vgh_en ends. vgl_en_row_on[8:0] : Select exactly which row the vgh_en starts. vgl_en_row_off[8:0] : Select exactly which row the vgh_en ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.20. Pump control 10(98h)

Command Set		PWRCTRL10								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	vgl_disch_row_on[8]	vgl_disch_row_off[8]			vgl_disch_frm_on[1:0]		vgl_disch_frm_off[1:0]		81h
2nd Parameter		vgl_disch_row_on[7:0]								91h
3rd Parameter		vgl_disch_row_off[7:0]								63h
Description	vgl_disch_frm_on[1:0] : Roughly select the frame from which the vgl_disch starts. vgl_disch_frm_off[1:0] : Roughly select the frame from which the vgl_disch ends. vgl_disch_row_on[8:0] : Select exactly which row the vgl_disch starts. vgl_disch_row_off[8:0] : Select exactly which row the vgl_disch ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.21. Pump control 11(99h)

Command Set		PWRCTRL11								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	vgl_drain_row_on[8]	vgl_drain_row_off[8]			vgl_drain_frm_on[1:0]		vgl_drain_frm_off[1:0]		81h
2nd Parameter		vgl_drain_row_on[7:0]								F4h
3rd Parameter		vgl_drain_row_off[7:0]								64h
Description	vgl_drain_frm_on[1:0] : Roughly select the frame from which the vgl_drain starts. vgl_drain_frm_off[1:0] : Roughly select the frame from which the vgl_drain ends. vgl_drain_row_on[8:0] : Select exactly which row the vgl_drain starts. vgl_drain_row_off[8:0] : Select exactly which row the vgl_drain ends on.									
Restriction	Should set “FF=A5” before configure this registers									

6.4.22. Pump control 12(9Ah)

Command Set		PWRCTRL12								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write			ddvdh_btvs[1:0]		ddvdh_btvs_en				28h
Description	ddvdh_btvs_en: Enable the clamp function of DDVDH. ddvdh_btvs[1:0]: Setting the clamp level of DDVDH.									
Restriction	Should set “FF=A5” before configure this registers									

ddvdh_btvs[1:0]	DDVDH(Unit:V)
00	6.2
01	6.4
10	**6.6**
11	6.8

Condition :In the sleep out + display off status, clock frequency is F_{osc}/6 (VCI=IOVCC=3.3V)

6.4.23. Pump control 13(9Bh)

Command Set		PWRCTRL13								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write			ddvdl_btvs[1:0]		ddvdl_btvs_en				18h
Description	ddvdl_btvs_en: Enable the clamp function of DDVDL. ddvdl_btvs[1:0]: Setting the clamp level of DDVDL. Condition :In the sleep out + display off status, clock frequency is F_{osc}/6 (VCI=IOVCC=3.3V)									
Restriction	Should set “FF=A5” before configure this registers									

ddvdl_btvs[1:0]	DDVDL(Unit:V)
00	-4.0
01	**-4.4**
10	-4.8
11	-5.0

6.4.24. Pump control 14(9Ch)

Command Set		PWRCTRL14								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	vgh_noreg		vgh_bth[1:0]						A0h
Description	vgh_noreg: Enable the clamp function of VGH. vgh_bth[1:0]: Select the VGH pump ratio.									
Restriction	Should set “FF=A5” before configure this registers									

vgh_noreg	Clamp
0	disable
1	enable

vgh_bth[1:0]	Ratio
00	5*VCI
01	6*VCI
10	**7*VCI**
11	8*VCI

6.4.25. Pump control 15(9Dh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">PWRCTRL15</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td></td><td></td><td></td><td></td><td></td><td colspan="3">vgh_set[2:0]</td><td>03h</td></tr>
<tr><td>Description</td><td colspan="10">vgh_set[2:0]: Setting the clamp level of VGH.
<table><tr><th>vgh_set[2:0]</th><th>VGH(Unit:V)</th></tr><tr><td>000</td><td>12.0</td></tr><tr><td>001</td><td>12.5</td></tr><tr><td>010</td><td>13.0</td></tr><tr><td>011</td><td>13.5</td></tr><tr><td>100</td><td>14.0</td></tr><tr><td>101</td><td>14.5</td></tr><tr><td>110</td><td>15.0</td></tr><tr><td>111</td><td>15.5</td></tr></table>Condition :In the sleep out + display off status, VGH pump ration select 8*VCI, clock frequency is F_{osc}/8 (VCI=IOVCC=3.3V)</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this register</td></tr>
</table>

6.4.26. Pump control 16(9Eh)

<table>
<tr><th colspan="2">Command Set</th><th colspan="9">PWRCTRL16</th></tr>
<tr><th>Command</th><th>Write/ Read</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Parameter</td><td>Write</td><td>vgl_btrs</td><td>vgl_noreg</td><td></td><td></td><td></td><td colspan="3">vgl_set[2:0]</td><td>C2h</td></tr>
<tr><td>Description</td><td colspan="10">vgl_btrs: Select the VGH pump ratio.
<table><tr><th>vgl_btrs</th><th>Ratio</th></tr><tr><td>0</td><td>-5*VCI</td></tr><tr><td>1</td><td>-6*VCI</td></tr></table>vgl_noreg: Enable the clamp function of VGL.
<table><tr><th>vgl_noreg</th><th>Clamp</th></tr><tr><td>0</td><td>disable</td></tr><tr><td>1</td><td>enable</td></tr></table>vgl_set[2:0]: Setting the clamp level of VGL.
<table><tr><th>vgl_set[2:0]</th><th>VGL(Unit:V)</th></tr><tr><td>000</td><td>-9.0</td></tr><tr><td>001</td><td>-9.5</td></tr><tr><td>010</td><td>-10.0</td></tr><tr><td>011</td><td>-10.5</td></tr><tr><td>100</td><td>-11.0</td></tr><tr><td>101</td><td>-11.5</td></tr><tr><td>110</td><td>-12.0</td></tr><tr><td>111</td><td>-12.5</td></tr></table>Condition :In the sleep out + display off status, VGL pump ration select -6*VCI, clock frequency is F_{osc}/8 (VCI=IOVCC=3.3V)</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this register</td></tr>
</table>

6.4.27. Pump control 17(9Fh)

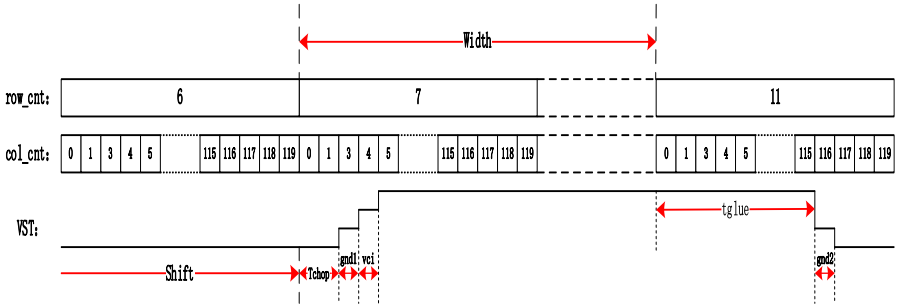
Command Set		PWRCTRL17								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W	gam_ref_bypass		vdds_en_bypass	vref_en_bypass	vgl_drain_bypass	vgl_disch_bypass	gam_en_bypass	pump_ctrl_en	00h
2nd Parameter		vgl_en_bypass	vgh_drain_bypass	vgh_disch_bypass	vgh_en_bypass	mv_disch_bypass	ddvdl_en_bypass	ddvdh_en_bypass	ddvdh_drain_bypass	00h
3rd Parameter		sd_n_en_bypass							sd_en_bypass	04h
Description	When entering test mode, use the following signal to turn off the corresponding power supply: pump_ctrl_en :Power master switch, can turn off all power supplies. gam_ref_bypass :Turn off the gam_ref. vdds_en_bypass :Turn off the vdds_en. vref_en_bypass :Turn off the vref_en. vgl_drain_bypass :Turn off the vgl_drain. vgl_disch_bypass :Turn off the vgl_disch. gam_en_bypass :Turn off the gam_en. vgl_en_bypass :Turn off the vgl_en. vgh_drain_bypass :Turn off the vgh_drain. vgh_disch_bypass :Turn off the vgh_disch. vgh_en_bypass :Turn off the vgh_en. mv_disch_bypass :Turn off the mv_disch. ddvdl_en_bypass :Turn off the ddvdl_en. ddvdh_en_bypass :Turn off the ddvdh_en. ddvdh_drain_bypass :Turn off the ddvdh_drain. sd_en_bypass :Turn off the sd_p_en. sd_n_en_bypass: Turn off the sd_n_en.									
Restriction	Should set “FF=A5” before configure this registers									

6.5. Description of Private Registers Command 3

6.5.1. GOA control(A0h)

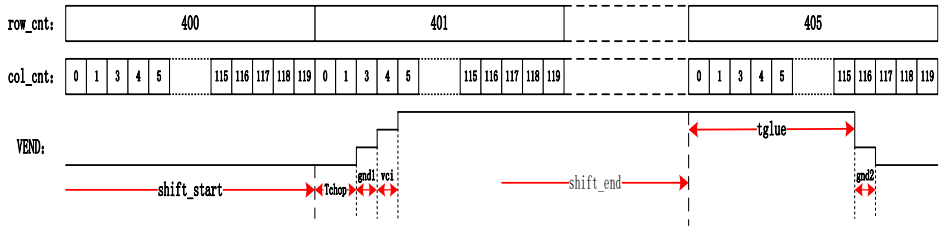
<table>
<tr><td colspan="2">Command Set</td><td colspan="9">GOACTRL</td></tr>
<tr><td>Command</td><td>Write/ Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>1st Parameter</td><td rowspan="3">Multi-W</td><td></td><td></td><td>1</td><td colspan="3">goa_slpin_sel[2:0]</td><td colspan="2">map_sel[1:0]</td><td>28h</td></tr>
<tr><td>2nd Parameter</td><td colspan="3">goa_vds_slpin_sel[2:0]</td><td colspan="3">goa_gcl_slpin_sel[2:0]</td><td colspan="2">level_sel[1:0]</td><td>24h</td></tr>
<tr><td>3rd Parameter</td><td></td><td></td><td></td><td>exit_disp_hiz_enable</td><td colspan="4">exit_disp_hiz_num[3:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">map_sel[1:0]: map_sel=2‘b01 only, others reserved
goa_slpin_sel[2:0] : When the current state is sleep in, Select the goa PAD(CLK、STV0、STV1、STV2、VGL) output voltage.
goa_vds_slpin_sel[2:0]:When the current state is sleep in, Select the goa PAD(VDS、VSD)output voltage.
goa_gcl_slpin_sel[2:0]:When the current state is sleep in, Select the goa PAD(GCH)output voltage
level_sel[1:0]: Level selection when all gate on
<table><tr><td>level_sel[1:0]</td><td>Level selection</td></tr><tr><td>00</td><td>VGH</td></tr><tr><td>01</td><td>VGL</td></tr><tr><td>10</td><td>GND</td></tr><tr><td>11</td><td>HIZ</td></tr></table>
exit_disp_hiz_enable: When LVD adopts the strategy of scanning two more frames, all GOA signals are processed HIZ for a period of time to prevent non-overlapping, and then scan for the two frames
‘0’ : Turn off the function
‘1’ : Turn on the function
exit_disp_hiz_num[3:0]: This register represents the duration of HIZ when LVD occurs using the strategy of scanning two more frames</td></tr>
<tr><td>Restriction</td><td colspan="10">Should set “FF=A5” before configure this registers</td></tr>
</table>

6.5.2. GOA VST control(A1h~AAh)

Command Set		VSTCTR								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A1h	Write	goa_vst1_shift[7:0]								8Ah
A2h	Write	goa_vst2_shift[7:0]								89h
A3h	Write	goa_vst3_shift[7:0]								88h
A4h	Write	goa_vst4_shift[7:0]								87h
A5h	Write	vst_gnd1_period[7:0]								0Ah
A6h	Write	vst_gnd2_period[7:0]								0Ah
A7h	Write	vst_vci_period[7:0]								0Ah
A8h	Write	goa_vst_tchop[8]	goa_vst_tglue[8]	vst_noverlap[1:0]		goa_vst_width[3:0]				04h
A9h	Write	goa_vst_tchop[7:0]								2Bh
AAh	Write	goa_vst_tglue[7:0]								00h
Description	goa_vst1_shift[7:0]~goa_vst4_shift[7:0] : Specifies the row on which the VST begins. shift[7]=1， Shift = vbp – shift[6:0]； shift[7]=0， Shift = vbp + shift[6:0]；  vst_gnd1_period[7:0] : Specifies the time when the VST voltage is raised to GND. vst_gnd2_period[7:0] : Specifies the time when the VST voltage will fall back to GND. vst_vci_period[7:0] : Specifies the time when the VST voltage is raised to VCI. vst_noverlap[1:0] : VST switching interval between different power supplies. goa_vst_width[3:0] : The time interval during which the VST is maintained at the VGH voltage. goa_vst_tchop[8:0] :Specifies which column the VST should be raised from. goa_vst_tglue[8:0] : Specifies the column from which the VST starts to pull low.									
Restriction	Should set “FF=A5” before configure this registers									

6.5.3. GOAVEND control(ABh~B8h)

Command Set		VENDCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
ABh (1st Parameter)	Multi-W						goa_vend1_shift_start[10:8]			00h
ABh (2nd Parameter)		goa_vend1_shift_start[7:0]								04h
ACh (1st Parameter)	Multi-W						goa_vend1_shift_end[10:8]			02h
ACh (2nd Parameter)		goa_vend1_shift_end[7:0]								7Ch
ADh (1st Parameter)	Multi-W						goa_vend2_shift_start[10:8]			00h
ADh (2nd Parameter)		goa_vend2_shift_start[7:0]								04h
AEh (1st Parameter)	Multi-W						goa_vend2_shift_end[10:8]			02h
AEh (2nd Parameter)		goa_vend2_shift_end[7:0]								7Ch
AFh (1st Parameter)	Multi-W					all_gate_hiz_period[3:0]				03h
AFh (2nd Parameter)				all_gate_nov_period[5:0]						04h
AFh (3rd Parameter)		all_gate_vci_period[7:0]								0Ah
B0h (1st Parameter)	Multi-W	eclk_gnd1_period[7:0]								0Ah
B0h (2nd Parameter)		eclk_gnd2_period[7:0]								0Ah
B0h (3rd Parameter)		eclk_vci_period[7:0]								0Ah
B0h (4th Parameter)								eclk_noverlap[1:0]		00h
B3h	Write	vend_gnd1_period[7:0]								0Ah

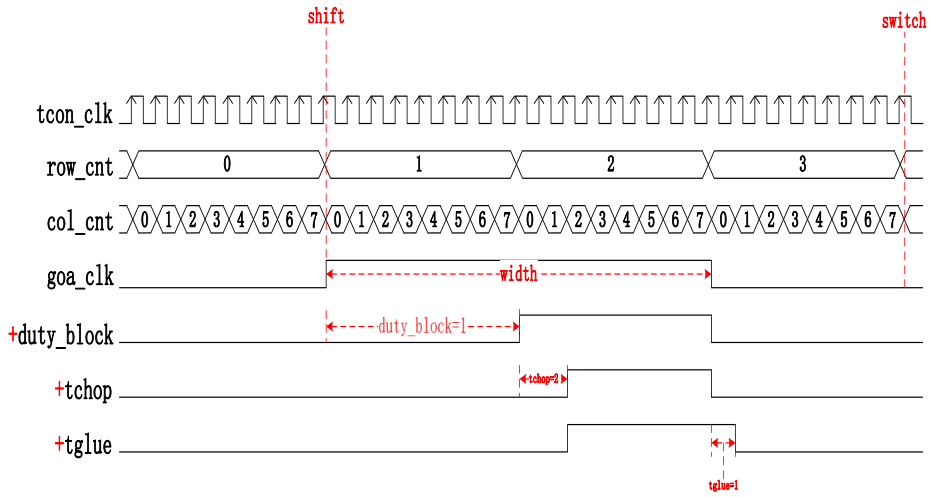
<table>
<tr><td>B4h</td><td>Write</td><td colspan="7">vend_gnd2_period[7:0]</td><td>0Ah</td></tr>
<tr><td>B5h</td><td>Write</td><td colspan="7">vend_vci_period[7:0]</td><td>0Ah</td></tr>
<tr><td>B6h
(1st Parameter)</td><td rowspan="2">Multi-W</td><td>goa_vend_tchop[8]</td><td>goa_vend_tglue[8]</td><td>vend_noverlap[1:0]</td><td>goa_vend1_glass_sel</td><td>goa_vend2_glass_sel</td><td>goa_rst_shift2_en</td><td>bw_fw_sel</td><td>06h</td></tr>
<tr><td>B6h
(2nd Parameter)</td><td colspan="4">vds_noverlap[3:0]</td><td colspan="3">eck_noverlap[3:0]</td><td>00h</td></tr>
<tr><td>B7h</td><td>Write</td><td colspan="7">goa_vend_tchop[7:0]</td><td>44h</td></tr>
<tr><td>B8h</td><td>Write</td><td colspan="7">goa_vend_tglue[7:0]</td><td>44h</td></tr>
<tr><td>Description</td><td colspan="9">goa_vend1_shift_start[10:0] : Specifies the row on which the VEND begins.
Note：Do not add or subtract with vbp, specify a row directly
 

goa_vend1_shift_end[10:0] : Specifies the row on which the VEND ends.
goa_vend2_shift_start[10:0] : Specifies the row on which the VEND begins.
goa_vend2_shift_end[10:0] : Specifies the row on which the VEND ends.
all_gate_hiz_period[3:0] : when all gate on , Specifies the time when the GOA voltage is raised to Hiz
all_gate_nov_period[5:0] : when all gate on , Specifies the time when the GOA voltage will be pulled to Hiz after the VCI
all_gate_vci_period[7:0] :when all gate on , Specifies the time of GOA at VCI level
eclk_gnd1_period[7:0] : Specifies the time when the ECLK voltage is raised to GND.
eclk_gnd2_period[7:0] : Specifies the time when the ECLK voltage will fall back to GND.
eclk_vci_period[7:0] : Specifies the time when the ECLK voltage is raised to VCI.
eclk_noverlap[1:0] : ECLK switching interval between different power supplies.
vend_gnd1_period[7:0] : Specifies the time when the VEND voltage is raised to GND.
vend_gnd2_period[7:0] : Specifies the time when the VEND voltage will fall back to GND.
vend_vci_period[7:0] : Specifies the time when the VEND voltage is raised to VCI.
goa_vend_tchop[8:0]: Specifies which column the VEND should be raised from
goa_vend_tglue[8:0]: Specifies the column from which the VEND starts to pull low.
vend_noverlap[1:0] : VEND switching interval between different power supplies.
goa_vend1_glass_sel : VEND1 Whether to reverse polarity
goa_vend2_glass_sel: VEND2 Whether to reverse polarity
goa_rst_shift2_en : Whether to enable two pulses
bw_fw_sel : bw and fw voltage selection.
vds_noverlap[3:0]: Specifies the time of vds at Hiz level when state machine change from</td></tr>
</table>

	non-display to display eck_noverlap[3:0]: Specifies the time of eck at Hiz level when state machine change from non-display to display
Restriction	Should set “FF=A5” before configure this registers

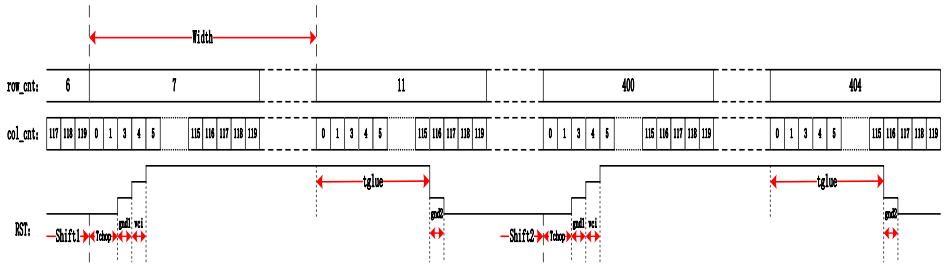
6.5.4. GOACLK control(B9h~D1h)

Command Set		CLKCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B9h	Write	goa_clk1_shift[7:0]								82h
BAh	Write	goa_clk2_shift[7:0]								81h
BBh	Write	goa_clk3_shift[7:0]								80h
BCh	Write	goa_clk4_shift[7:0]								01h
BDh	Write	goa_clk5_shift[7:0]								86h
BEh	Write	goa_clk6_shift[7:0]								85h
BFh	Write	goa_clk7_shift[7:0]								84h
C0h	Write	goa_clk8_shift[7:0]								83h
C1h	Write	clk_gnd1_period[7:0]								0Ah
C2h	Write	clk_gnd2_period[7:0]								0Ah
C3h	Write	clk_vci_period[7:0]								0Ah
C4h	Write	goa_clk_tchop[8]	goa_clk_tglue[8]	clk_noverlap[1:0]		goa_clk_width[3:0]				03h
C5h	Write	goa_clk_tchop[7:0]								2Bh
C6h	Write	goa_clk_tglue[7:0]								00h
C7h	Write					duty_block[3:0]				00h
C8h (1st Parameter)	Multi-W		goa_clk1_switch[10:8]				goa_clk2_switch[10:8]			22h
C8h (2nd Parameter)			goa_clk3_switch[10:8]				goa_clk4_switch[10:8]			22h
C9h	Write	goa_clk1_switch[7:0]								73h
CAh	Write	goa_clk2_switch[7:0]								74h
CBh	Write	goa_clk3_switch[7:0]								75h
CCh	Write	goa_clk4_switch[7:0]								76h
CDh (1st Parameter)	Multi-W		goa_clk5_switch[10:8]				goa_clk6_switch[10:8]			22h
CDh (2nd Parameter)			goa_clk7_switch[10:8]				goa_clk8_switch[10:8]			22h

CEh	Write	goa_clk5_switch[7:0]	6Fh
CFh	Write	goa_clk6_switch[7:0]	70h
D0h	Write	goa_clk7_switch[7:0]	71h
D1h	Write	goa_clk8_switch[7:0]	72h
Description	goa_clk1_shift[7:0]~goa_clk8_shift[7:0] : Specifies the row on which the CLK begins. shift[7]=1，Shift = vbp – shift[6:0]； shift[7]=0，Shift = vbp + shift[6:0]；  clk_gnd1_period[7:0] : Specifies the time when the CLK voltage is raised to GND. clk_gnd2_period[7:0] : Specifies the time when the CLK voltage will fall back to GND. clk_vci_period[7:0] : Specifies the time when the CLK voltage is raised to VCI. clk_noverlap[1:0] : CLK switching interval between different power supplies. goa_clk_width[3:0] : The time interval during which the CLK is maintained at the VGH voltage. goa_clk_tchop[8:0] : Specifies which column the CLK should be raised from. goa_clk_tglue[8:0] : Specifies the column from which the CLK starts to pull low. duty_block[3:0] : Set the duty cycle of CLK signal. goa_clk1_switch[10:0]~goa_clk8_switch[10:0] : Set the CLK on which line to turn off.		
Restriction	Should set “FF=A5” before configure this registers		

6.5.5. GOA RST control(D2h~D9h)

Command Set		RSTCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D2h	Write	goa_rst_shift1[7:0]								8Eh
D3h (1st Parameter)	Multi-W						goa_rst_shift2[10:8]			02h
D3h (2nd Parameter)		goa_rst_shift2[7:0]								75h
D4h	Write	rst_gnd1_period[7:0]								0Ah
D5h	Write	rst_gnd2_period[7:0]								0Ah
D6h	Write	rst_vci_period[7:0]								0Ah
D7h (1st Parameter)	Multi-W			rst_noverlap[1:0]		goa_rst_width1[3:0]				04h
D7h (2nd Parameter)		goa_rst_width2[7:0]								03h
D8h (1st Parameter)	Multi-W							goa_rst_tchop1[8]	goa_rst_tchop2[8]	00h
D8h (2nd Parameter)		goa_rst_tchop1[7:0]								56h
D8h (3rd Parameter)		goa_rst_tchop2[7:0]								00h
D9h (1st Parameter)	Multi-W							goa_rst_tglue1[8]	goa_rst_tglue2[8]	00h
D9h (2nd Parameter)		goa_rst_tglue1[7:0]								2Bh
D9h (3rd Parameter)		goa_rst_tglue2[7:0]								7Fh

Description	goa_rst_shift1[7:0] : Specifies the row on which the RST begins. shift[7]=1，Shift = vbp – shift[6:0]； shift[7]=0，Shift = vbp + shift[6:0]； goa_rst_shift2[7:0] : Specifies the row on which the RST begins Note：Do not add or subtract with vbp, specify a row directly  goa_rst_shift2[10:0] : Specifies the row on which the RST begins. rst_gnd1_period[7:0] : Specifies the time when the RST voltage is raised to GND. rst_gnd2_period[7:0] : Specifies the time when the RST voltage will fall back to GND. rst_vci_period[7:0] : Specifies the time when the RST voltage is raised to VCI. rst_noverlap[1:0] : RST switching interval between different power supplies. goa_rst_width1[3:0] : The time interval during which the first pulse of the RST is maintained at the VGH voltage. goa_rst_width2[7:0] : The time interval during which the second pulse of the the RST is maintained at the VGH voltage. goa_rst_tchop1[8:0] : Specifies which column the first pulse of the RST should be raised from. goa_rst_tchop2[8:0] : Specifies which column the second pulse of the RST should be raised from. goa_rst_tglue1[8:0] : Specifies the column from which the first pulse of the RST starts to pull low. goa_rst_tglue2[8:0] : Specifies the column from which the second pulse of the RST starts to pull low.
Restriction	Should set “FF=A5” before configure this registers

6.5.6. Read ID1(DAh)

Command Set		RDID1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read	sys_id1[7:0]								30h
Description	sys_id1[7:0]:LCD module/driver ID.									
Restriction	-									

6.5.7. Read ID2(DBh)

Command Set		RDID2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read	sys_id2[7:0]								07h
Description	sys_id2[7:0] : LCD module/driver ID.									
Restriction	-									

6.5.8. Read ID3(DCh)

Command Set		RDID3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read	sys_id3[7:0]								01h
Description	sys_id3[7:0] : LCD module/driver ID.									
Restriction	-									

6.5.9. Write ID1(DDh)

Command Set		WRID1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	sys_id1[7:0]								30h
Description	sys_id1[7:0] : Set the LCD module/driverid1 through the interface.									
Restriction	Should set “FF=A5” before configure this registers									

6.5.10. Write ID2(DEh)

Command Set		WRID2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	sys_id2[7:0]								07h
Description	sys_id2[7:0] : Set the LCD module/driverid2 through the interface.									
Restriction	Should set “FF=A5” before configure this registers									

6.5.11. Write ID3(DFh)

Command Set		WRID3								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	sys_id3[7:0]								01h
Description	sys_id3[7:0] : Set the LCD module/driverid3 through the interface.									
Restriction	Should set “FF=A5” before configure this registers									

6.6. Description of Private Registers Command 4

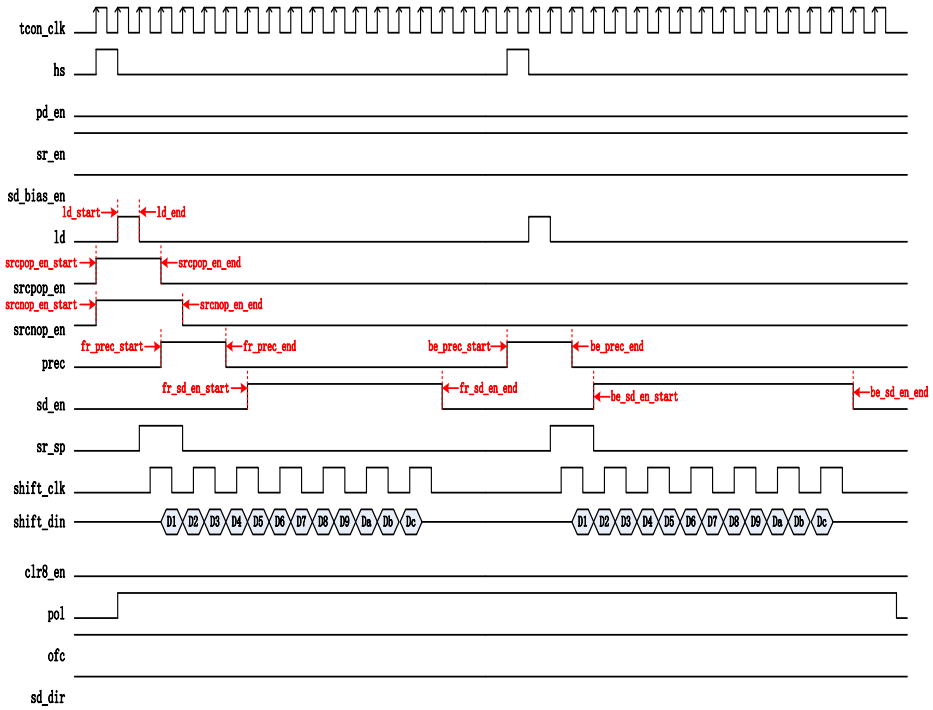
6.6.1. Source control(E0h~F2h)

Command Set		SOUCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E0h	Write	ld_start [8]	ld_end [8]	srcpop _en_st art[8]	srcpop _en_e nd[8]	srcnop _en_st art[8]	srcnop _en_e nd[8]	fr_pre c_start [8]	fr_pre c_end[8]	00h
E1h (1st Parameter)	Multi-W	ld_start[7:0]								03h
E1h (2nd Parameter)						sd_bias_adj[3:0]				0Ah
E2h	Write	ld_end[7:0]								04h
E3h	Write	srcpop_en_start[7:0]								01h
E4h	Write	srcpop_en_end[7:0]								14h
E5h	Write	srcnop_en_start[7:0]								01h
E6h	Write	srcnop_en_end[7:0]								19h
E7h	Write	fr_prec_start[7:0]								16h
E8h	Write	fr_prec_end[7:0]								29h
E9h	Write	pol_ctrl	pol_ini t	ofc_ct rl	ofc_in it	odd_e ven_ct rl	fr_sd_ en_sta rt[8]	fr_sd_ en_en d[8]	pol_ct rl2	20h
EAh	Write	fr_sd_en_start[7:0]								2Bh
EBh	Write	fr_sd_en_end[7:0]								C1h
ECh	Write	pol_sw itch[8]	be_pre c_start[8]	be_pre c_end[8]	chopper_sel[2:0]			be_sd _en_st art[8]	be_sd _en_e nd[8]	00h
EDh	Write	be_prec_start[7:0]								07h
EEh	Write	be_prec_end[7:0]								1Bh
EFh	Write	be_sd_en_start[7:0]								1Dh
F0h	Write	be_sd_en_end[7:0]								C1h
F1h	Write	pol_switch[7:0]								14h
F2h (1st Parameter)	Multi-W		sd_n_e n_opti on	source _prech arge_d isable		ofc_ph ase_sy c	usr_re v	norma l_blac k	pts	68h
F2h (2nd Parameter)		fr_sd_n_en_start[7:0]								1Bh
F2h (3rd Parameter)		be_sd_n_en_start[7:0]								0Bh

F2h (4th Parameter)		fr_sd_n _en_sta rt[8]	be_sd_ n_en_s tart[8]	precharge_gray[5:0]	20h

Description

ld_start[8:0] : Sets the starting column of the ld signal.



ld_end[8:0] : Sets the end column of the ld signal

srcpop_en_start[8:0] : Sets the starting column of the srcpop signal

srcpop_en_end[8:0] : Sets the end column of the srcpop signal

srcnop_en_start[8:0] : Sets the starting column of the srcnop signal

srcnop_en_end[8:0] : Sets the end column of the srcnop signal

fr_prec_start[8:0] : Sets the starting column of the first half of the prec signal

fr_prec_end[8:0] : Sets the end column of the first half of the prec signal

sd_bias_adj[3:0] : Sets the ajustment value of sd_bias

pol_ctrl/pol_ctrl2 : Dot inversion and column Inversion selection

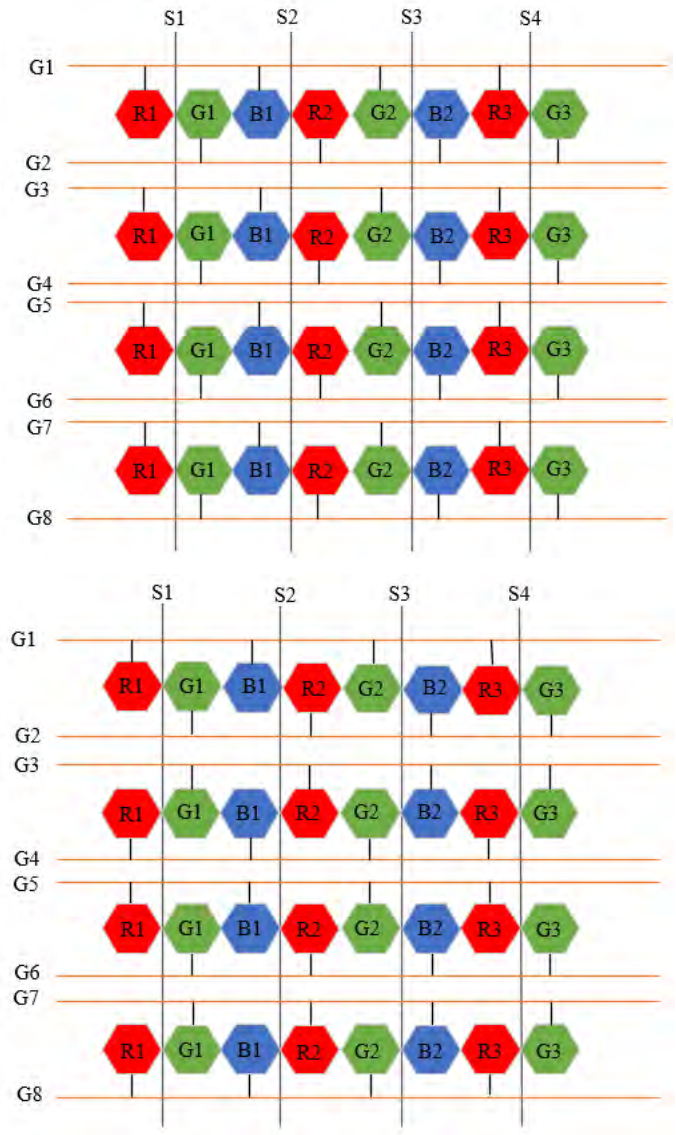
pol_ctrl	pol_ctrl2	POL inversion
0	0	POL column inversion
0	1	POL 1 dot inversion
1	0	POL 2 dot inversion
1	1	POL 4 dot inversion

pol_init :Set the initial value of the pol signal.

ofc_ctrl : ofc signal enable.

ofc_init :Set the initial value of the ofc signal.

odd_even_ctrl : Selection of glass connection.



fr_sd_en_start[8:0] : Sets the starting column of the first half of the sd_en signal.

fr_sd_en_start[8:0] : Sets the starting column of the first half of the sd_en signal.

pol_switch[8:0] : Set the POL signal conversion location.

be_prec_start[8:0] : Sets the starting column of the last half row of the prec signal.

be_prec_end[8:0] : Sets the end column of the last half row prec signal.

chopper_sel[2:0] : Select the mode of ofc signal.

chopper_sel[2:0]	chopper mode
000	2 frames
001	2 frames + 1 line
010	2 frames + 2 line
011	2 frames + 4 line
100	always Low
101	always High
others	2 frames

	be_sd_en_start[8:0] : Sets the starting column of the last half row of the sd_en signal. be_sd_en_end[8:0] : Sets the end column of the last half row sd_en signal. sd_n_en_option : The option of the sd_n_en's rising edge "0" : Align with sd_p_en "1" : The rising edge of sd_n_en is configured independently source_precharge_disable : Whether to disable the precharge function during frame inversion "0" : enable the precharge function during frame inversion "1" : disable the precharge function during frame inversion ofc_phase_syc : The option of phase relation between p_ofc and n_ofc "0" : Same phase "1" : Inverting phase usr_rev : Whether to reverse the display data by bit "0" : no reverse the display data by bit "1" : reverse the display data by bit normal_black :Select whether the screen is always white or always black. pts : Determine source output in a non-display area in the partial display mode. fr_sd_n_en_start[8:0] : Sets the starting column of the last half row of the sd_n_en signal. be_sd_n_en_start[8:0] : Sets the end column of the last half row of the sd_n_en signal. precharge_gray[5:0] : The precharge grayscale value when enable the precharge function during frame inversion
Restriction	Should set "FF=A5" before configure this registers

6.6.2. CP test 1(F4h)

Command Set		CPTEST1								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write								clear_ cmd	00h
Description	clear_cmd : enable signal for writing all pixels data through registers， and display by cmd F5h “0” : disable “1” : enable									
Restriction	Should set “FF=A5” before configure this registers									

6.6.3. CP test 2(F5h)

Command Set		CPTEST2								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-W			clear_dat_r[5:0]						00h
2nd Parameter				clear_dat_g[5:0]						00h
3rd Parameter				clear_dat_b[5:0]						00h
Description	clear_dat_r[5:0] : red subpixel data setting clear_dat_g[5:0] : green subpixel data setting clear_dat_b[5:0] : blue subpixel data setting									
Restriction	Should set “FF=A5” before configure this registers									

6.6.4. FSM Control(F9h)

Command Set		FSMCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write			clear_2frame_disable	1		poff_xon_disable	disp_blk_lvd_en	wait_disp_disable	12h
Description	clear_2frame_disable: The number of frames cleared when the state machine is CLEAR "0" : Fix two frames and exit CLEAR "1" : The command is displayed until the power-off command is executed poff_xon_disable: all gate on enable signal "0" : all gate on is enabled when GOA is powerd off normally "1" : all gate on is disabled when GOA is powerd off normally disp_blk_lvd_en: Whether to enable the LVD monitor function when the state machine is DISP_BLK "0" : Disable the function "1" : Enable the function wait_disp_disable: Whether to disable the wait_disp state "0" : Enable "1" : disable									
Restriction	Should set "FF=A5" before configure this registers									

6.6.5. Pad control (FBh)

Command Set		PADCTRL								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Write	atest_en	osc_test_oe							00h
Description	atest_en : Whether to enable the osc_clk dichotomal signal. osc_test_oe :osc div test output enable.									
Restriction	Should set “FF=A5” before configure this registers									

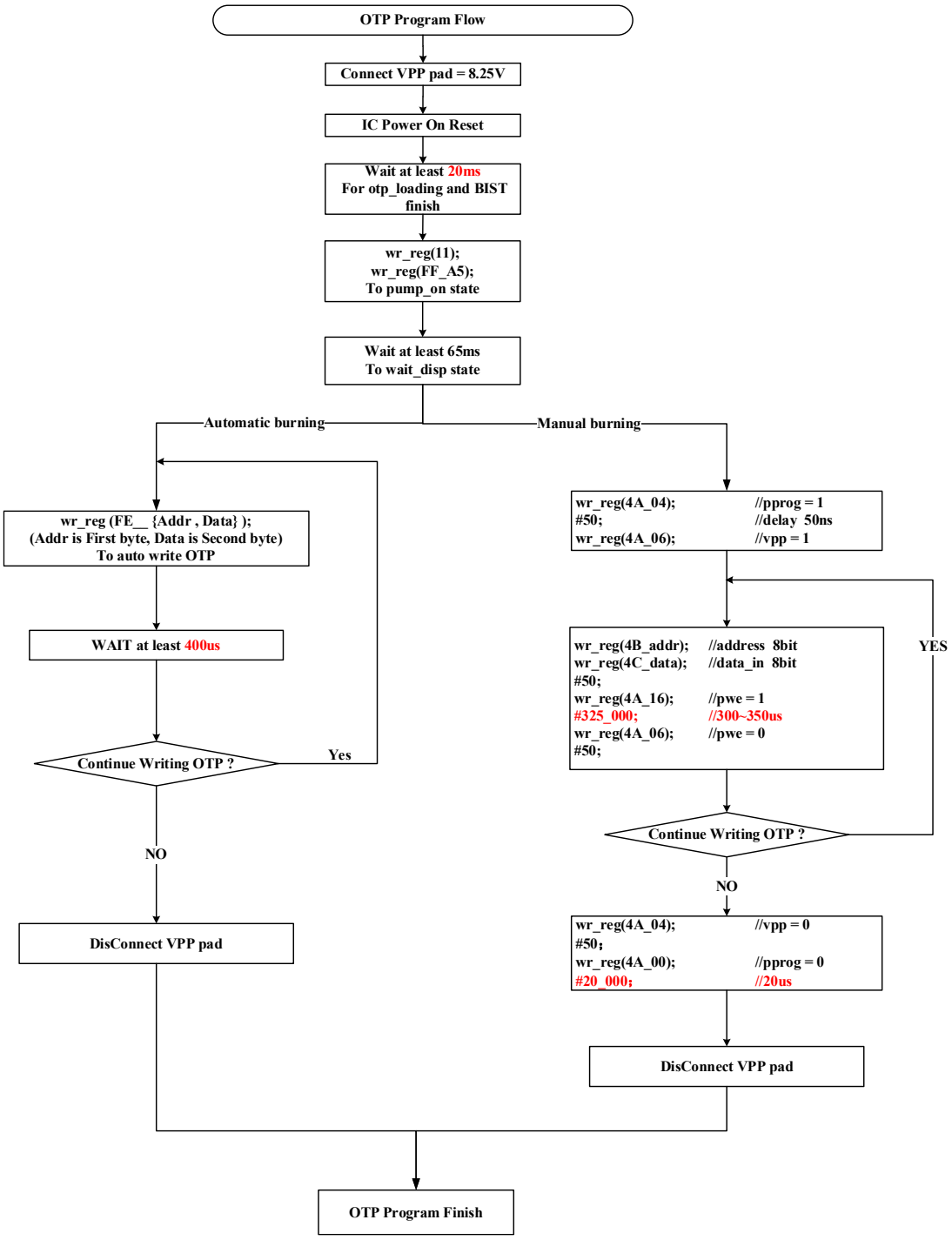
6.6.6. RDSTATE(FCh)

Command Set		RDSTATE								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
Parameter	Read						cur_state[2:0]			/
Description	cur_state[2:0] : Gets the current state information of the state machine.									
Restriction	-									

6.6.7. Read power status(FDh)

Command Set		RD_PWR_STATUS								
Command	**Write/ Read**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1st Parameter	Multi-R					gam_en	vref_en	vdds_en	gam_ref_en	/
2nd Parameter						vgl_en	vgh_en	ddvdl_en	ddvdh_en	/
Description	Reading this address will fetch internal power information.									
Restriction	-									

7. OTP Programming Flow



8. Electrical Characteristics

8.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When NV3007 is used out of the absolute maximum ratings, NV3007 may be permanently damaged. To use NV3007 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, NV3007 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Supply voltage(Digital)	DVDD	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	℃	-35~+85
Storage temperature	Tstg	℃	-40~+100
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

Figure 8-1 Absolute Maximum Ratings

8.2. DC Characteristics

General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.8	3.3	3.6	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.8	3.3	3.6	Note2
Digital Operating voltage	DVDD	V	Digital supply voltage	-	1.55	-	Note2
Gate Driver High Voltage	VGH	V	-	12.0	-	15.5	Note3
Gate Driver Low Voltage	VGL	V	-	-9.0	-	-12.5	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	21	-	28	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7* IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	IGND	-	0.3* IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8* IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	IGND	-	0.2* IOVCC	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or IGND	-0.1	-	+0.1	Note1,2,3
Source Driver							
Source Output Range	Vsout	V	-	GVCL	-	GVDD	Note4
Output Offset Voltage	Voffset	mV	-	-	-	35	Note5

Figure 8-2 General DC Characteristics

Note 1: IOVCC=1.8 to 3.6V, VCI=2.8 to 3.6V, GND=IGND=0V, Ta=-30 to 85 ℃

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, D/CX, RESX, SDA, SDA2, SDA3, SCL, IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: The Max. Value is between measured point of source output and gamma setting value.

8.3. AC Characteristics

8.3.1. Display Serial Interface Timing Characteristics (3-line SPI system)

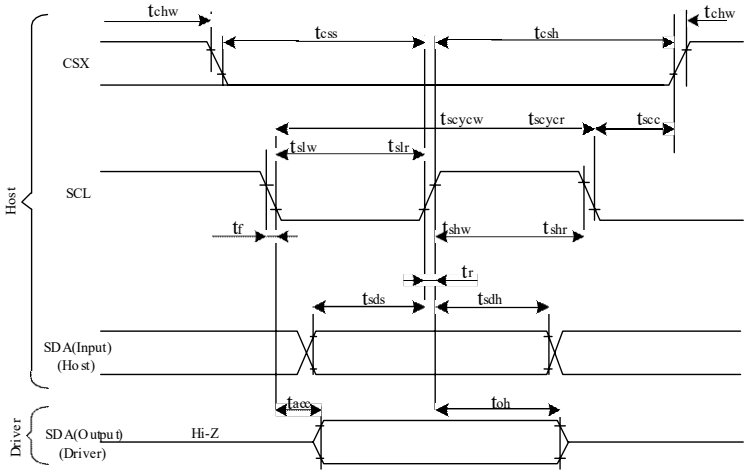


Figure8-3-1 3-line serial Interface Timing Characteristics

Signal	Symbol	Parameter	min	max	Unit
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns
	tshw	SCL "H" Pulse Width (Write)	5	-	ns
	tslw	SCL "L" Pulse Width (Write)	5	-	ns
	tscycr	Serial Clock Cycle (Read)	150	-	ns
	tshr	SCL "H" Pulse Width (Read)	60	-	ns
	tslr	SCL "L" Pulse Width (Read)	60	-	ns
SDA (Input)	tsds	Data setup time (Write)	5	-	ns
	tsdh	Data hold time (Write)	5	-	ns
SDA (Output)	tacc	Access time (Read)	10	50	ns
CSX	tscc	SCL-CSX Time	65	-	ns
	tchw	CSX "H" Pulse Width	40	-	ns
	tcss	CSX-SCL Time	15	-	ns
	tcsh		15	-	ns

Note: Ta =25 °C, IOVCC= 1.8V~3.6V, VCI=2.8V~3.6V, GND=IGND=0V

Table 8-3-1 3-line serial Interface Characteristics

8.3.2. Display Serial Interface Timing Characteristics (4-line SPI system)

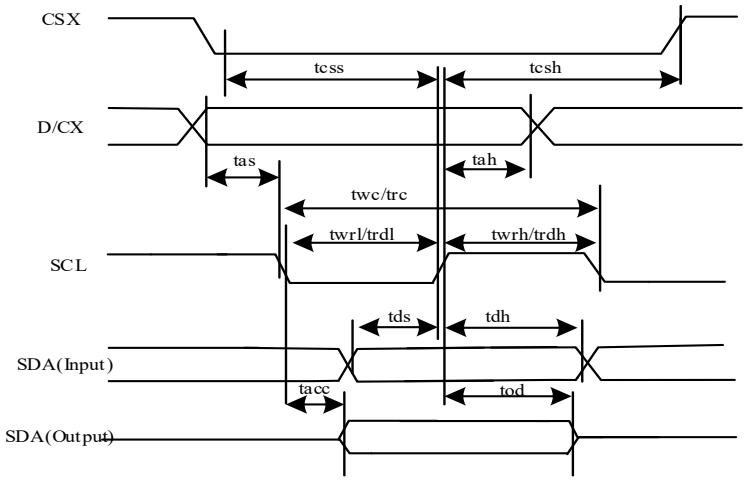


Figure 8-3-2 4-line serial Interface Timing Characteristics

Signal	Symbol	Parameter	min	max	Unit
CSX	tcss	Chip select time (Write)	15	-	ns
	tcsh	Chip select hold time (Read)	15	-	ns
SCL	twc	Serial Clock Cycle (Write)	10	-	ns
	twrh	SCL "H" Pulse Width (Write)	5	-	ns
	twrl	SCL "L" Pulse Width (Write)	5	-	ns
	trc	Serial Clock Cycle (Read)	150	-	ns
	trdh	SCL "H" Pulse Width (Read)	60	-	ns
	trdl	SCL "L" Pulse Width (Read)	60	-	ns
D/CX	tas	D/CX setup time	5	-	ns
	tah	D/CX hold time (Write/Read)	5	-	ns
SDA (Input)	tds	Data setup time (Write)	10	-	ns
	tdh	Data hold time (Write)	10	-	ns
SDA (Output)	tacc	Access time (Read)	10	50	ns

Note: Ta =25 °C, IOVCC= 1.8V~3.6V, VCI=2.8V~3.6V, GND=IGND=0V

Table 8-3-2 4-line serial Interface Characteristics

8.3.3. Display Serial Interface Timing Characteristics (4-line QSPI system)

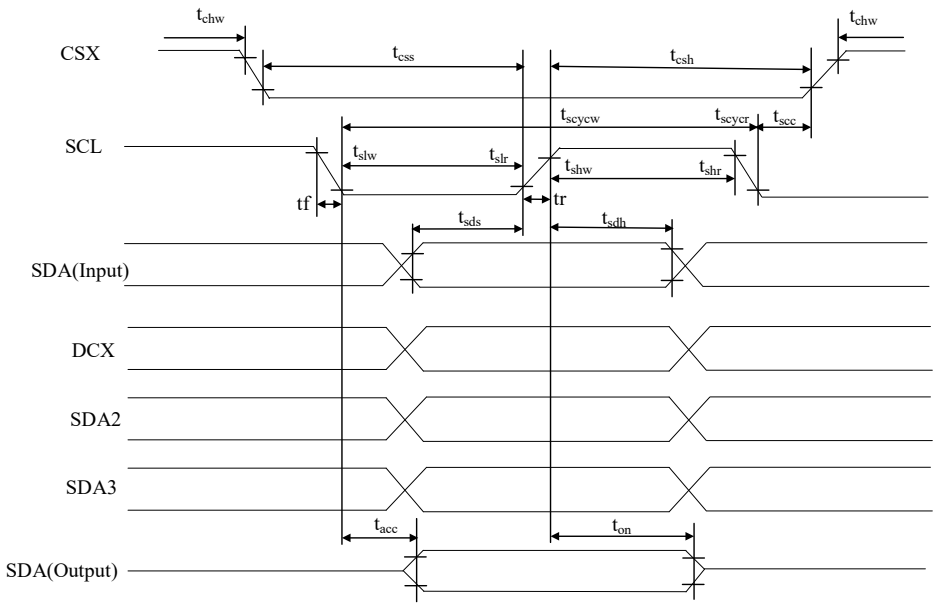


Figure 8-3-3 4-line QSPI Interface Timing Characteristics

Signal	Symbol	Parameter	min	max	Unit
SCL	tscycw	Serial Clock Cycle (Write)	19	-	ns
	tshw	SCL "H" Pulse Width (Write)	9.5	-	ns
	tslw	SCL "L" Pulse Width (Write)	9.5	-	ns
	tscycr	Serial Clock Cycle (Read)	150	-	ns
	tshr	SCL "H" Pulse Width (Read)	60	-	ns
	tslr	SCL "L" Pulse Width (Read)	60	-	ns
SDA (Input)	tsds	Data setup time (Write)	9.5	-	ns
	tsdh	Data hold time (Write)	9.5	-	ns
DCX	tsds	Data setup time (Write)	9.5	-	ns
	tsdh	Data hold time (Write)	9.5	-	ns
SDA2	tsds	Data setup time (Write)	9.5	-	ns
	tsdh	Data hold time (Write)	9.5	-	ns
SDA3	tsds	Data setup time (Write)	9.5	-	ns
	tsdh	Data hold time (Write)	9.5	-	ns
SDA (Output)	tacc	Access time (Read)	10	50	ns
CSX	tscc	SCL-CSX Time	65	-	ns
	tchw	CSX "H" Pulse Width	10	-	ns
	tcss	CSX-SCL Time	33	-	ns
	tcsh		33	-	ns

Note: Ta =25 °C, IOVCC= 1.8V~3.6V, VCI=2.8V~3.6V, GND=IGND=0V

Table 8-3-3 4-line QSPI Interface Characteristics

9. GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPAREDBY
1.0	2024-6-19	First Release	qizhang