High performance mutual capacitor multi-touch chip

1. Summary

CST3240 Series multi-point capacitive touch chip, support single-layer, multi-layer module and a variety of patterns, using multi-channel 7V above high voltage drive, to achieve high performance, high sensitivity real multi-finger touch effect. Compared to the traditional single-voltage drive can provide higher signal-to-noise ratio and anti-interference ability. At the same time, the chip internal self-mutual integrated capacitor induction module, combined with the intelligent scanning algorithm, can achieve rapid response, with excellent noise resistance, waterproof, low power consumption performance.

2. Features

■ High-performance capacitance detection circuit and the DSP module. Self-mutual integrated detection module;
Multi-channel high voltage simultaneous drive, achieve high sensitivity, high signal to noise sampling;
. Dynamic wide range frequency hopping technology, support stronger anti-interference ability;
. Support the passive capacitive touch pen;
. Support standby gesture wake-up function;. support online programming;
. Built-in watchdog;
. Multiple key button support.

■ performance index
. Typical refresh rate of 100Hz;
. Water operation, thumb recognition and large palm inhibition;. Typical power consumption in dynamic mode: 10 mA;
. Typical power consumption in monitoring mode: 4 mA (30 Hz);
. Typical power consumption in sleep mode: 20 uA.

■ capacitive screen support
. Up to 40 drive / induction channels, and support TX / RX interchange;
. Channel suspension / pull-down design support;
. Support traditional DITO and SITO and various patterns;
. Module parameters are automatically adjusted, and the maximum support impedance is up to 60K;
. Cover Lens Thickness support, glass <= 2mm acrylic <=1mm.

■ communication interface
. I2C master / slave communication interface, rate 50 Khz ~ 400 Khz configurable;
GPIO support, a variety of working modes can be matched, built-up resistance mode;
. Built-in 1.8V LDO, compatible with 1.8 V / V DDA interface level can be matched.

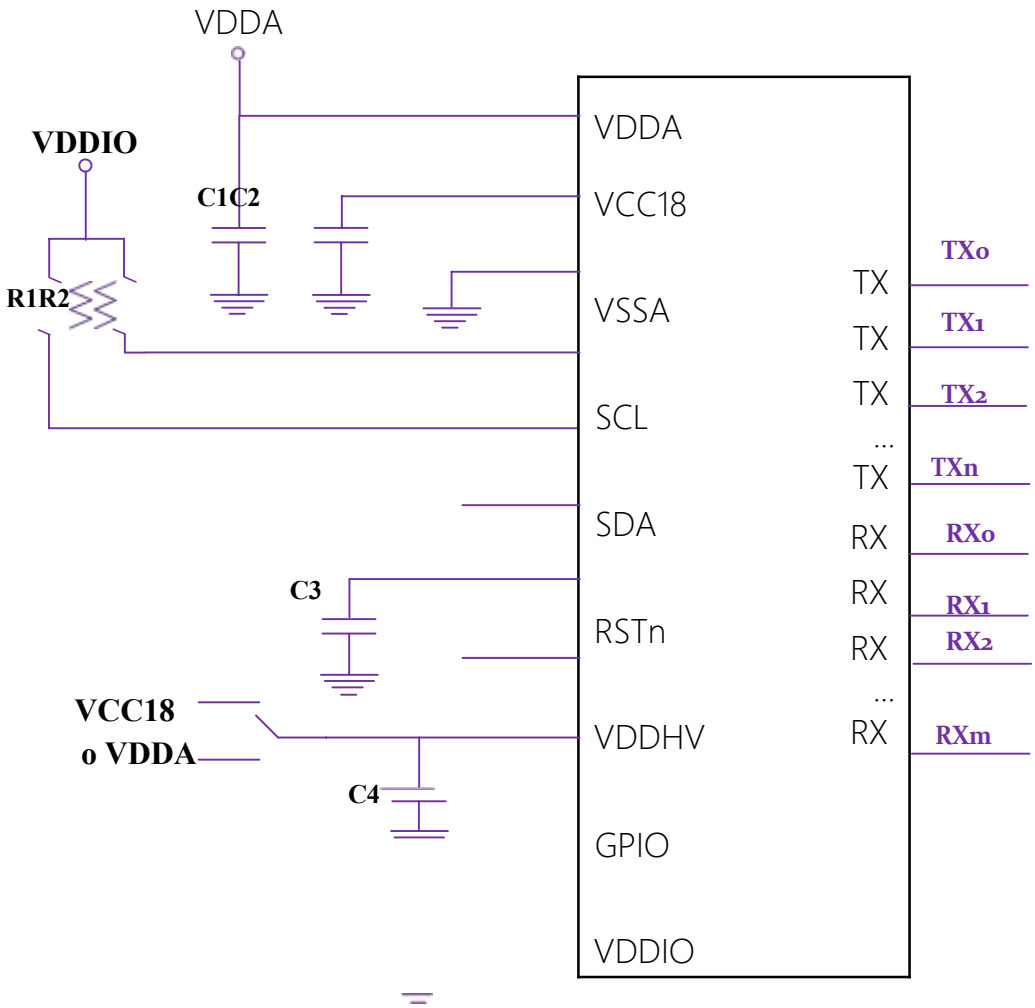
■ power supply
. Single power supply 2.8~3.6V, please refer to the circuit design,
Power supply ripple <= 50 mv;. A small number of peripheral devices.

■ Package type: QFN52L 6 * 6.

3. Application

Mobile phones, tablets, laptops, touchpad, etc.

4. Typical application circuit diagram



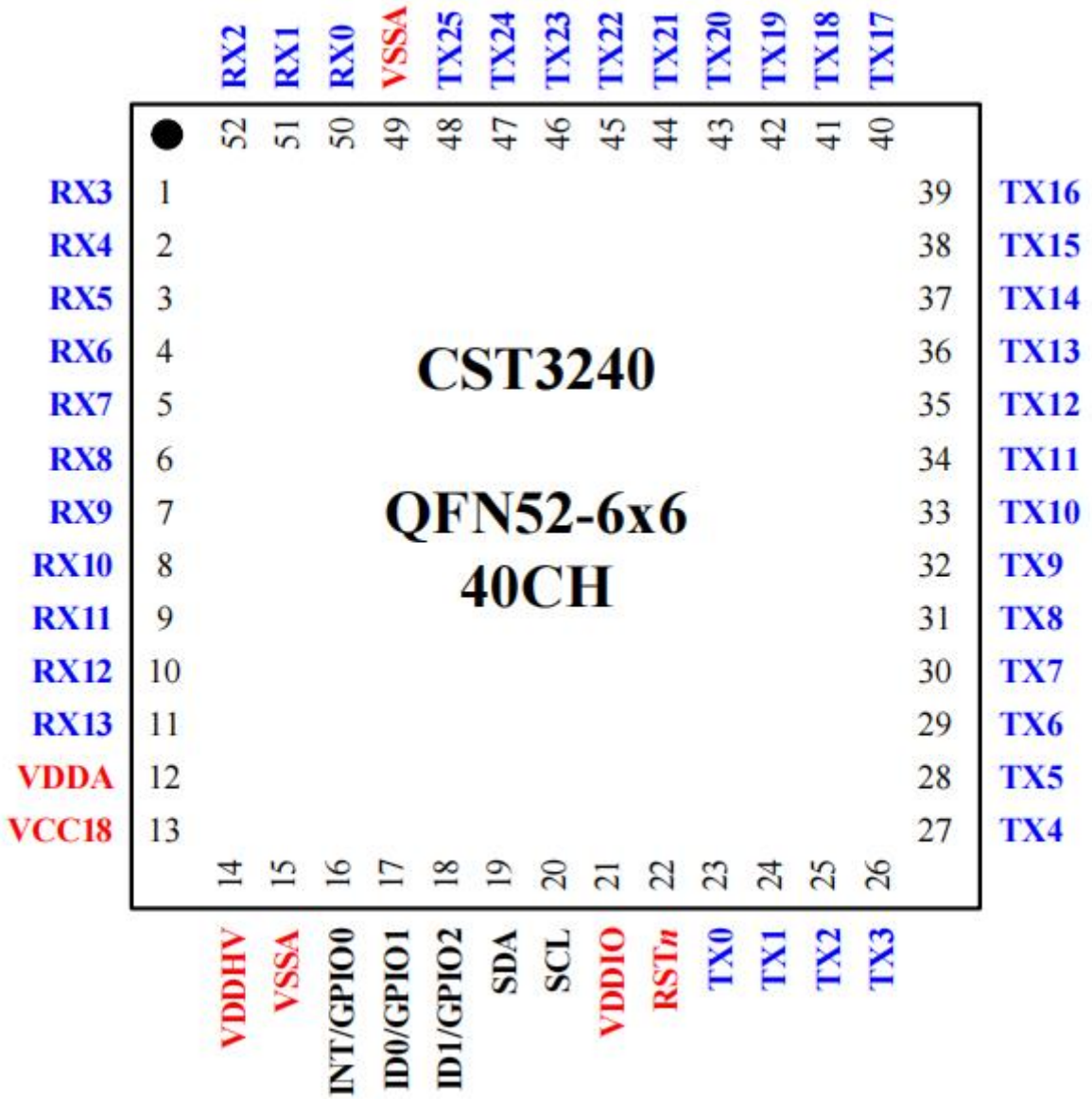
C1: 2.2uF/10V C2:1uF/10V

C3: 100nF/10V C4:1uF/10V

VDDIO: VDDA or VCC 18, determined according to IIC, SPI communication and RSTn voltage. R1 / R2: I2C bus pull resistance, can also be configured with the chip internal 5K pull resistance instead.

GPIO: as INT or SensorID suspended or GND.

5. Pocket arrangement



pin	name	type	functional description	pin	name	type	functional description
1	RX3	I/O	Induction channel	27	TX4	I/O	Drive channel
2	RX4	I/O	Induction channel	28	TX5	I/O	Drive channel
3	RX5	I/O	Induction channel	29	TX6	I/O	Drive channel
4	RX6	I/O	Induction channel	30	TX7	I/O	Drive channel
5	RX7	I/O	Induction channel	31	TX8	I/O	Drive channel

6	RX8	I/O	Induction channel	32	TX9	I/O	Drive channel
7	RX9	I/O	Induction channel	33	TX10	I/O	Drive channel
8	RX10	I/O	Induction channel	34	TX11	I/O	Drive channel
9	RX11	I/O	Induction channel	35	TX12	I/O	Drive channel
10	RX12	I/O	Induction channel	36	TX13	I/O	Drive channel
11	RX13	I/O	Induction channel	37	TX14	I/O	Drive channel

6. Pin Description

12	VDDA	PWR/I	2.8~3.6V，2.2uF	38	TX15	I/O	Drive channel
13	VCC18	PWR/O	1.8V，0.1 uF	39	TX16	I/O	Drive channel
14	VDDHV	PWR/O	Max8V，100nF	40	TX17	I/O	Drive channel
15	VSSA	GND	Simulated to	41	TX18	I/O	Drive channel
16	INT/GPIO0	I/O	Universal digital IO	42	TX19	I/O	Drive channel
17	ID0/GPIO1	I/O	Universal digital IO	43	TX20	I/O	Drive channel
18	ID1/GPIO2	I/O	Universal digital IO	44	TX21	I/O	Drive channel
19	SDA	I/O	The I2C data signal	45	TX22	I/O	Drive channel
20	SCL	I/O	The I2C clock signal	46	TX23	I/O	Drive channel
21	VDDIO	PWR/I	Connect to VDDA / VCC 18	47	TX24	I/O	Drive channel
22	RST n	I	Reset, low and effective	48	TX25	I/O	Drive channel
23	TX0	I/O	Drive channel	49	VSSA	GND	Simulated to
24	TX1	I/O	Drive channel	50	RX0	I/O	Induction channel
25	TX2	I/O	Drive channel	51	RX1	I/O	Induction channel
26	TX3	I/O	Drive channel	52	RX2	I/O	Induction channel

IInput Only Enter only

O OutputOnly Output only

I / O Input And Output input and output

7. Order information

P/N	Package	The surface print	Pack
CST3240	QFN52L6*6	CST3240 XXXXX (Production tracking code)	4000 / plate, compile with shipment

8. Table of limit parameters

Parameter	Symbol	Value min	Value type	Value max	Unit	注释
Operating Voltage VDDA	Vdd	2.8	3.0	3.6	V	
Power Supply Ripple	Vrip	-	-	50	mV	
Analog I/O Withstand Voltage	Vioa	-0.3	-	8	V	
Digital I/O Withstand Voltage	Viod	-0.3	-	3.6	V	
Maximum I/O Current Capacity	Iiom	-10	-	10	mA	
Operating Temperature Range	Topr	-20	+25	+85	℃	
Storage Temperature Range	Tstg	-60	-	+125	℃	
Operating Humidity	Hopr	-	-	95	%	
ESD HBM	ESD	±6000	-	-	V	Human Body Model ESD
ESD CDM	ESD	±2000	-	-	V	Charge Device Model
Latch-up Current	LU	-	-	150	mA	

9. Electrical characteristics

9.1 DC (DC) electrical characteristics

Ambient temperature of 25.C，VDDA=2.8V。

Parameter	Symbol	Value min	Value type	Value max	unit
Low-level output voltage value	Vol	-	-	0.3* VDDIO	V
High-level output voltage value	Voh	0.7*VDDIO	-	-	V
Input the low-level voltage value	Vil	-0.3	-	0.3* VDDIO	V
Input the high-level voltage value	Vih	0.7*VDDIO	-	VDDIO	V
Operating current (dynamic mode)	Iopr	-	10	-	mA
Operating current (monitoring mode)	Imon	-	4 (30Hz)	-	mA
Operating current (sleep mode)	Islp	-	20	-	uA

9.2 AC (AC) electrical characteristics

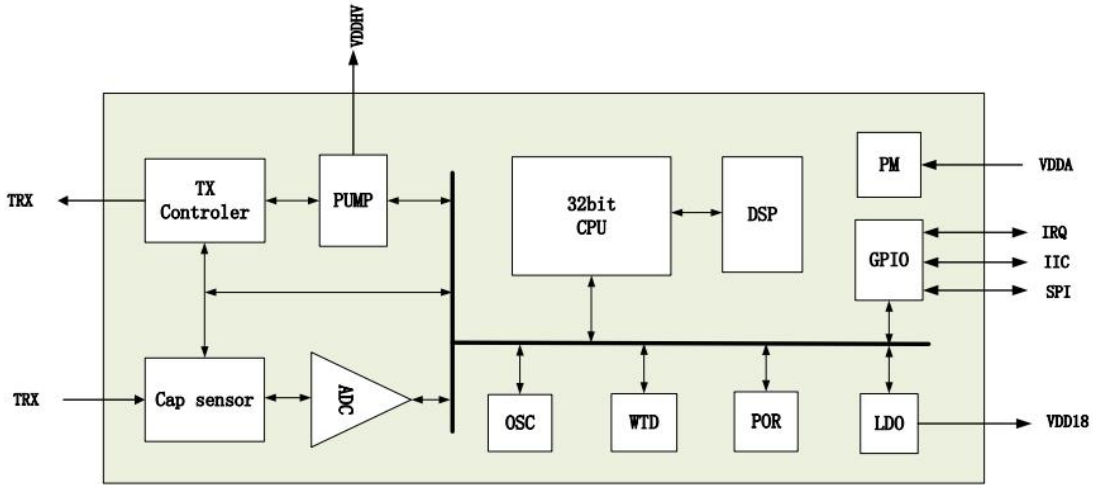
Ambient temperature of 25.C，VDDA=2.8V。

Parameter	Symbol	Min.	Type.	Max	Unit
TX clock frequency	ftx	-	-	300	KHz
TX output voltage	Vtx	-	-	7.5	V
RX input voltage	Vrx	-	1.4	-	V

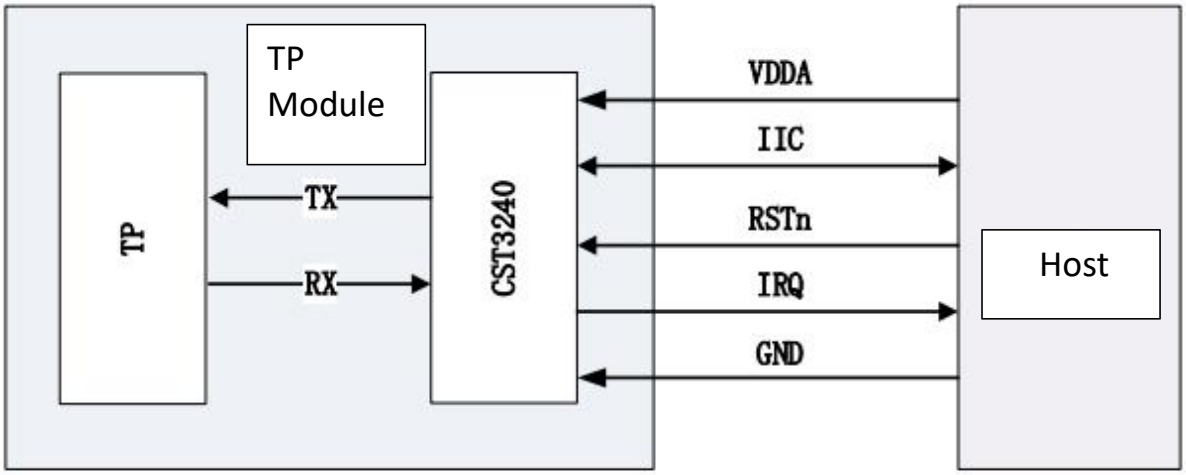
10. Functional description

CST3240 Series of multi-point capacitive touch chip, using high-voltage drive, compared with the traditional low-voltage drive can provide a higher signal-to-noise ratio and anti-noise capability, to achieve ultra-sensitive touch. At the same time, the chip internal self-mutual capacitor induction module, combined with intelligent scanning algorithm, in the realization of rapid response, has extremely excellent noise resistance, waterproof, low power consumption performance.

The overall system block diagram is as follows:



10.1 Host Interface



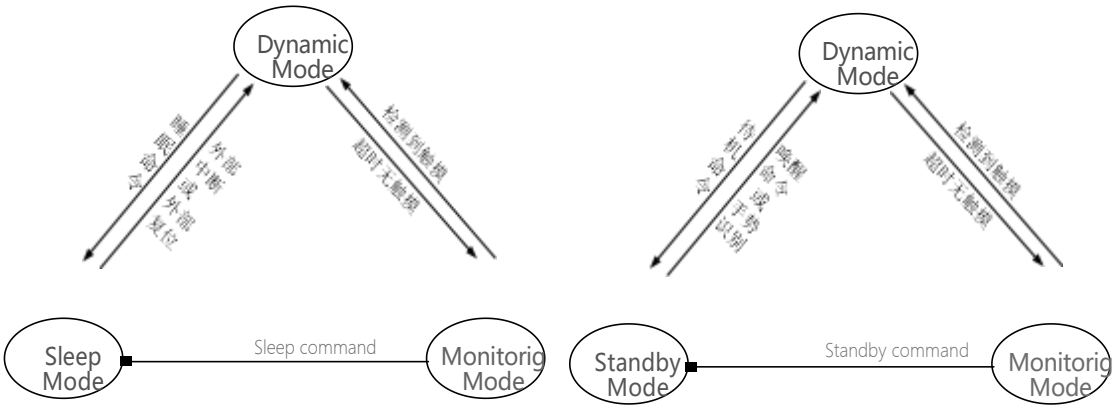
The figure above shows the interface relationship between the host and CST3240, including IIC, IRQ, RSTn and VDDA signals between the host and CST3240, and TX and RX signals between CST3240 and TP.

VDDA: the operating voltage of the CST3240.

SCL and SDA: Serial communication interface, host Master, CST3240 Slave.

IRQ: Interrupt signal, which is the general GPIO interface. When CST3240 prepares the data, it is used to notify the host data to read, such as touch data, gesture data, etc.

10.2 Working mode



Dynamic models

In this mode when touches are frequently touched. In this mode, the touch chip quickly scans the touch screen, detects the touch and reports it to the host.

Monitoring mode

When the touch screen timeout has no touch action, the chip automatically switches to the monitoring mode. In this mode, the touch chip detects possible touch movements by scanning at a lower frequency, and quickly switches to the dynamic mode.

Standby Mode

In this mode when the standby command is received. In this mode, the touch chip scans the touch screen at a low frequency, matches the wake up gesture and enters the dynamic mode. At the same time, the host is woke up through the IRQ pin, and you can switch to the dynamic mode by wake up command.

Sleep Mode

When the sleep command is received, it is in this mode. In this mode, the touch chip is in a deep sleep state to maximize power consumption, and can be awakened by external interruption or external reset.

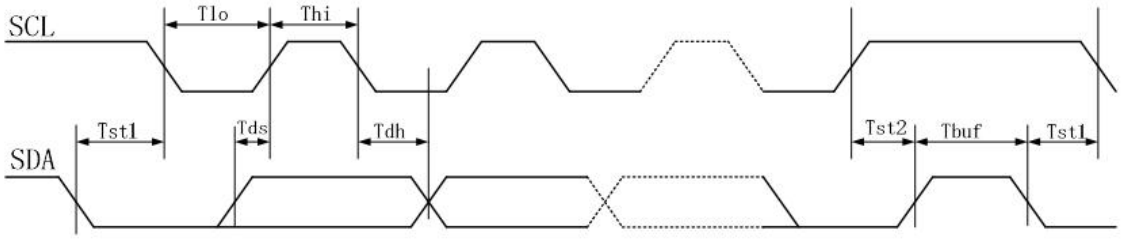
10.3 Channel / node configuration

The CST3240 multitouch chip can provide up to 40 channels, with flexible configuration between drive and sense functions for each channel, and each channel supports both self-capacitance and mutual-capacitance scanning. When allocating drive/sense pins, it is recommended to select pins that are continuously distributed.

The range of mutual capacitance that can be supported per node is: 0.5pF to 20pF (assuming a drive voltage of 7V).

10.4 I2C communication

CST3240 Support standard I2C communication protocol, can realize the compatible communication rate of 50 Kh z ~ 400 Kh z. Two I2C pins SCL and SDA, in addition to support open leakage mode, but also support internal pull-up mode, for flexible choice.



Description	Symbol	Fast Mode		Unit
		Min	Max	
SCL clock frequency	Fscl	0	400	kHz
SCL hold time forSTART condi tion	Tst1	0.6	-	us
LOW periodof SCL	Tlo	1.3	-	us
HIGH periodof SCL	Thi	0.6	-	us
SDA setup time	Tds	0.1	-	us
SDA hold time	Tdh	0	0.9	us
SCL setup time for STOP cond ition	Tst2	0.6	-	us
Ready time between STOP and START	Tbuf	20	-	us

CST3240 Always as a slave, the startup is actively established by the host. During the clock line SCL maintaining a high level, the level on the data line SDA is pulled down (i. e. negative jump), defined as the start signal of the I2C bus bus.

CST3240 The 8-bit address sent after detecting the start signal on the bus (the address can be customized in the chip, the default is 0x34 / 0x35). In the 9th clock cycle, change the data line SDA to the output port and pull down as the response signal. The data line SDA will send 9 bits of data in series in 9 clock cycles, 8 bits of valid data plus a response signal ACK or non-response signal NACK sent by 1 bit receiver.

The stop signal is also actively established by the host after the communication ends. The stop signal is when the clock line SCL maintains high level, the data line SDA is released so that the SDA returns to high level (i. e., positive jump). It marks the termination of a single data transfer.

A. The host writes the data to the CST3240. Data transfer format is shown in Fig:

S	Slave Address[7bit]	W[1bit]	ACK	DATA[8bit]	ACK	...	DATA[8bit]	ACK/ NACK	P

B. Host reads data from CST3240. Data transfer format is shown in Fig:

S	Slave Address[7bit]	R[1bit]	ACK	DATA[8bit]	ACK	...	DATA[8bit]	NACK	P

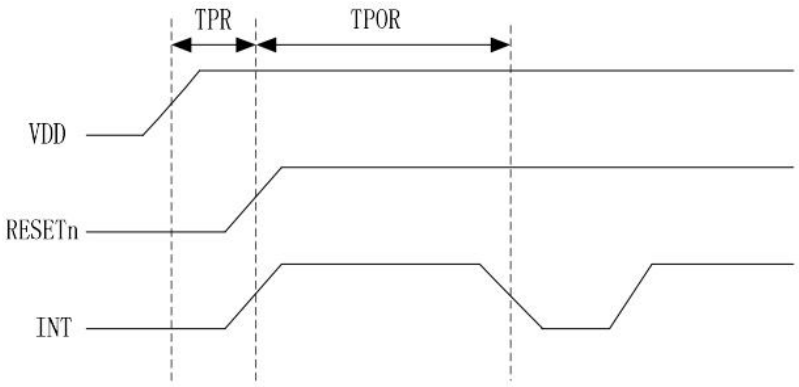
C. The host writes data into the CST3240 and then starts the starting condition, then reads the data from the CST3240; or the main device reads data from the CST3240 and then starts the starting condition, immediately after the main device writes the data into the CST3240. Data transfer format is shown in Fig:

S	Slave Address[7bit]	W[1bit]	ACK	DATA[8bit]	ACK	...	DATA[8bit]	ACK/ NACK	
RS	Slave Address[7bit]	R[1bit]	ACK	DATA[8bit]	ACK	...	DATA[8bit]	NACK	P

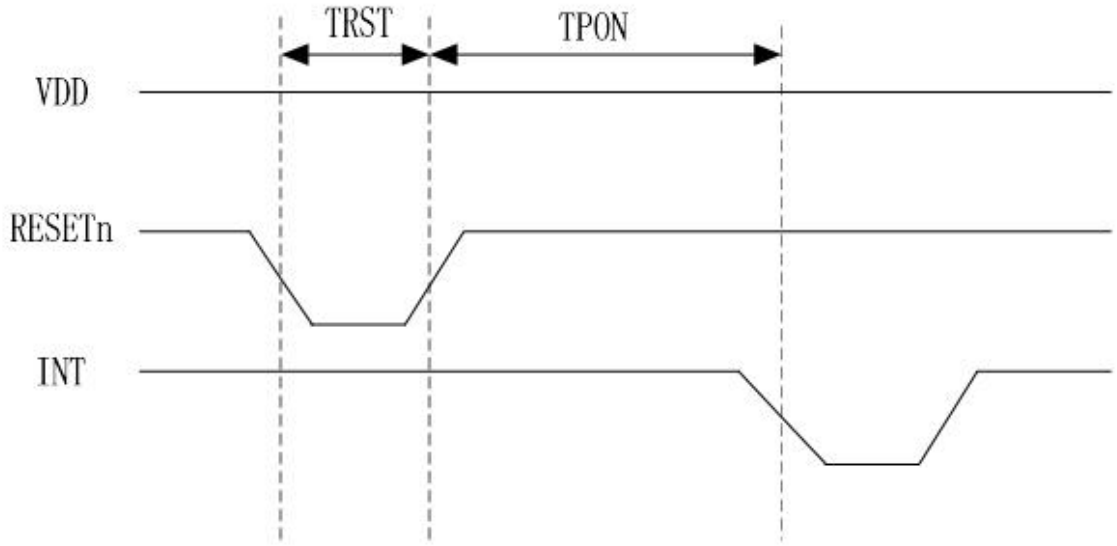
10.5 Power on / reset

Built-in electric reset module will keep the chip in the reset state until the voltage is normal, when the voltage is below a threshold, the chip will be reset, when the external reset pin RSTn is low will reset the whole chip, the pin built-in pull resistance and RC filter, external can be the pin, the chip built-in watchdog to ensure that when abnormal situation occurs, the chip can still return to normal working state within the specified time.

The timing of the power reset is shown in the figure below:



The electric timing



External reset timing

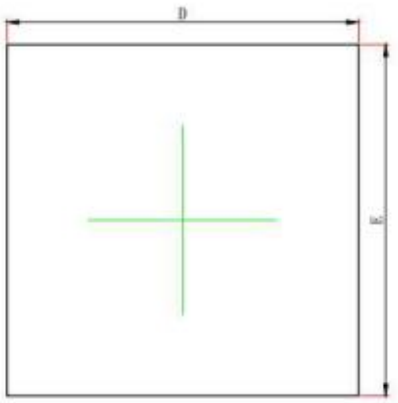
Symbol	Dscription	Type Value	Unit
TPOR	Time of chip initialization after power-on	400	mS
TPR	RST pin delay pull time	1	mS
TRON	Chip re-initialization time after reset	400	mS
TRST	Reset the pulse time	0.1	mS

10.6 Interrupt mode

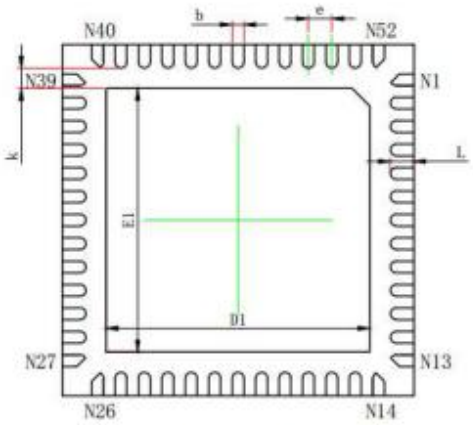
Touch chip only when detected effective touch, and need to report to the host, through the IRQ pin notification host read effective data, to improve the efficiency, reduce the CPU burden, interrupt edge can be configured to rise along or down along effective, when under the standby mode match predefined gestures, IRQ pin is also used to wake up the host.

11. Product packaging

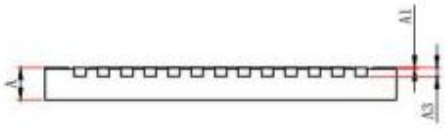
QFN52L 6*6



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152REF.		0.006REF.	
D	5.924	6.076	0.233	0.239
E	5.924	6.076	0.233	0.239
D1	4.400	4.600	0.173	0.181
E1	4.400	4.600	0.173	0.181
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
k	0.200MIN.		0.008MIN.	
L	0.324	0.476	0.013	0.019

12. Version record

Documentation Edition	Revise	Time
V1.0	The initial version	2022-2-16